Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 9, No. 2, September : 2023

EFFICIENT LOSSLESS IMAGE COMPRESSION FOR BUFFERLESSVIDEO STREAMING USING FUZZY-BASED MODIFIED GOLOMB RICE ENCODING

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Abstract

This paper unveils a unique approach VLSI-based image compression algorithm tailored for wireless sensor net- works. The algorithm integrates fuzzy decision, variable-size block partition, and coding for BTC (block truncation coding) method. Huffman coding is employed for eight block types, enhancing compression ratio. To achieve and improve the low cost and power attributes, an iterative BTC training module is introduced, along with predictive and modified Golomb-Rice coding modules. The proposed design, implement in UMC 0.18 μm CMOS process, boasts 6.4 k gate counts, 60, 000μm core area, 100 MHz operating frequency, and 3.11 mW power consumption. This design surpasses prior Joint Photographic Experts Group (JPEG), Joint Photographic Experts Group Lossless (JPEG-LS) and Near Lossless, and the fixed-size of block truncation coding designs, achieving a 20.9 percentage reduction in the gate count and utilizing a one-line-buffer memory, eliminating the need fora frame-buffer memory.

Index Terms—Block Truncation Coding, Branch Metric Unit, Redundant Data, Human Visual System, Discrete Cosine Trans- formation, PSNR (Peak Signal Noise Ratio), VQ (Vector Quantization), WSN (Wireless Sensor Networks).

I. INTRODUCTION

The time has progressed, more and more data has been created by humans via actions like typing, recording, photographing, scanning, etc. Human limitations in focus, precision, and speed make it impractical to constantly capture a large quantity of data. Using sensors to gather information on human existence in place of humans is one approach to the challenge.

Instead of basing choices off of simply one piece of in- formation, a computer or server may do so with the help of data analyzed from several sensors. People are paying more attention to wireless sensor networks (WSNs) due to the fast progress of sensor technology and wireless communication methods. Each node in a WSN is a sensor node equippedwith one or more physical phenomenon detectors like light, temperature, pressure, etc.

As the Rendering data is so much greater than any other kind of data in WSNs, the quantity of imagery and video data in WSNs increases in proportion to the number the wireless camera nodes. How to efficiently store and transmit photoswhile minimizing losses in quality due to the constraints of storage and mobile bandwidth is a pressing issue. Compressinga picture is a useful technique for lowering its data size before being stored or sent. The joint photo experts' team (JPEG) standard is the most widely used format for compressing still photographs. By using a mathematical procedure known as discrete cosine transform, JPEG is able to transform images from the frequency domain to the spatial domain (DCT).

To reduce file size, JPEG discards high-frequency information, which the human visual system does not need to detect subtle changes in. After that, a Huffman coding method isused

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 9, No. 2, September : 2023

to encode the data and further improve compressionrates. Nevertheless, the hardware cost and the energy usageof JPEG decoder design make it inappropriate for the WSN because of the way it compresses pictures using DCT, which demands significant computational complexity. In an effortto move away from the DCT-based JPEG standard, the joint photographic specialist's group also created JPEG 2000.

For even greater compression ratio improvement over JPEG,The JPEG 2000 uses the more complex entropy encodingalgorithm. Because of the enormity of the wavelet transform, the JPEG 2000 based approaches cannot be implemented in hardware. For image compression, JPEG-LS relied on apredictive system that took into account the positions of a picture's three closest neighbor's and an entropy coding.

JPEG-LS is a common choice for compressing medicalimages since it is lossless and does not rely on any transforms to achieve its compression. As JPEG-LS doesn't need any transformative mathematical operations, it compresses more quicker and has less computing complexity than jpg and JPEG2000. Yet, the compressors the JPEG-LS substantially smallercompared to those of JPEG and JEPG 2000. Hence, owing to the constraints of wireless.

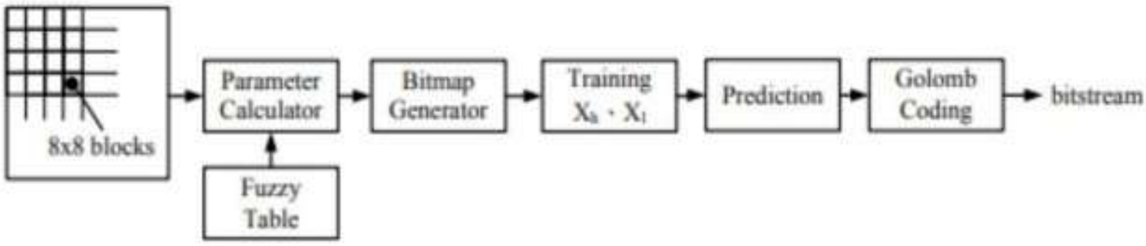

Fig. 1. Architecture of BTC

It is challenging to locate a candidate with low complexity and good cylinder pressure for the WSNs after analyzing JPEG, Jpg 2000, and JPEG-LS. With CMOS image sensors, picture compression was achieved by the use of delta modulators and delta sigma modulators, with pixel values being selected for input to the respective modulators.

Random selection of collected pixel values from a CMOS picture led to the creation of a single-shot compressive sensingsystem for CMOS image sensors. The implementation of a CMOS image sensor using block-based compressive sensing saved money. It was suggested that audio and image processing make use of an adapted non-uniform sample delta modulation (ANS-DM) method. To accomplish picture compression, the CMOS image sensor's output data was efficiently reducedusing delta modulation and sigma modulation dependent com-pression algorithms.

A system that uses the block truncation coding (BTC) it's seen as a possible solution. The source encoding of BTCoutput, with VQ; encrypting the raster image within a lookup table based on the Vector Quantization encoder, and it's getting through portrayal level based on binary search; that reducing the coding price with Hyping code and difference pulse code modulation; these are just a few of the methods recently proposed to continue improving the rendering quality,compression ratios of block truncation coding (DPCM).Since then, a Bitcoin-based picture compression scheme has been created because to its low production costs.

Even though the hardware's price and performance are well-suited to WSNs, the compression ratios were constrained by the fixed size of the block. Thus, it is important to createa WSN-friendly image compressor architecture that is both versatile and efficient.

II. ENCODING FOR COMPRESSION OF VISUAL CONTENT THROUGH BLOCK TRUNCATION

A. DIGITAL IMAGE FUNDAMENTALS

The basics of Block Truncation Coding (BTC) for compression techniques and the encoding of digital picture signals are discussed in this chapter. While looking at a digital image, imagine a frame as a series of horizontal lines, each linecontaining a group of picture components (pixels), and each group of lines being layered on top of the other. Instead,you might think of it as a grid of squares. A picture with the dimensions 512 x 512 contains, for instance, 512 horizontal lines, each of which is 512 pixels in size. Eachpixel in a picture has its own independent colour (hue) and brightness unit (intensity of light). Luminance refers to light intensity, whereas chrominance describes colour chroma). The three main colors--red, green, and blue—form the basis forall other colours.

B. NEED FOR IMAGE COMPRESSION

For various uses, digital pictures are first stored in memory before being preprocessed, transferred, and finally reprocessed.An image processor must process a massive amount of binary data. In the case of a monochrome picture with a 256 × 256 frame, the no.of bits required for represent the images pixels is 524288. Five minutes of video at 25 fps would need roughly40 million bits. It makes sense to cut down on the numberofbits before sending if doing so won't compromise the picture quality too much. The term Lossy Picture Compressiondescribes this technique. As a result, less bandwidth and less memory will be used during transmission.

But, with the right coding methods, photos may be compressed without losing quality. These so-called Lossless Image Compression techniques [9] are inherently less compressive than Lossy techniques.

C. TRADITIONAL BLOCK TRUNCATION CODING

In 1979, Delp and Mitchell unveiled Block Truncation Coding (BTC). The picture is divided into uniform, non- overlapping chunks for this encoding method. In analog signalprocessors, a picture is split into the smaller chunks of 'kxk' pixel for the processing. In this way, the frame with a resolution of the 512×512 may be broken up into 8 x 8 sections. Micro-blocks of 2x2 pixels, 4x4 pixels, 16x16 pixels, and32x32 pixels are often utilized as well. Here a mean brightnessvalue and b depending on a cutoff intensity-value. The averagerate pixel brightness in the region defines this cutoff. A 'bit plane' is generated by encoding the 'a' property pixel by the '0's and 'a' and the value pixel by '1's.

$$a = \bar{x} - \sigma\sqrt{\frac{q}{m-q}}$$

$$b = \bar{x} + \sigma\sqrt{\frac{m-q}{q}}$$

D. PARAMETERS FOR COMPRESSION, INCLUDING CR,BR, RMSE, PSNR, AND C

Image compression can be assessed through various metrics, including CR, RMSE, BR, and PSNR. These metrics are employed to evaluate the level of error introduced duringthe process of image compression. The visual quality of a picture may be quantified using a metric called contrast

(C). Compression ratio (CR) is the comparison of uncompressed image bit depth to compressed image bit depth. Hence, the formula for the compression ratio (CR) is: CR = (8 m) / (m + 16) and Bit Rate (BR) is a measure of how quickly data canbe sent. The original picture had 8 bits per pixel, hence the Bit Rate (BR) = (m + 16) / m.

E. VISUAL DEMONSTRATION OF BLOCK TRUNCATIONCODING APPLIED TO A RANDOM 4X4 BLOCK

The initial block is truncated to a height of 2 gray-scale levels. Every of the image's blocks undergo this Blocks Truncation Coding process. After estimated block a,b values are from the block co-ordinates x,y are used [6]in Equations, the decoder reconstructs the shortened form of every block in the original picture. The 8-bit pixel intensity is encoded by a sub- string in a 4x4 block. The x and y values of a block also needa coding size of 8 bits.

Comparisons are made between the original pictures and their measurements of contrast. In this section, we will examine these figures to those of the Classical BTC. Contrast values for the four examples photos are listed in Table 1.

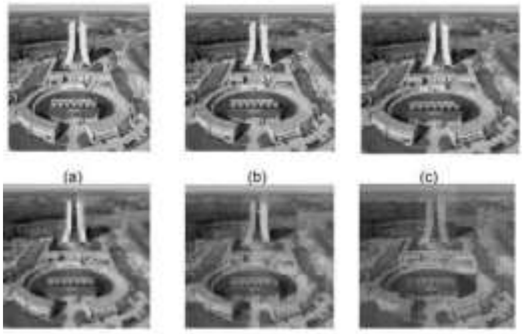

Fig. 2. (a) Here's the Original picture city.jpg, and the (b)-(f) The traditionalBTC for the block size 4*4, 8*8, 16*16, 32*32 and 64*64 for city.jpg

F. COMPUTATIONAL TIME FOR IMAGE PROCESSING

The amount of time required to process a picture is another critical factor. As the Bitcoin algorithm is rather straight forward, it requires less time to run. In addition, as block size grows, so does the amount of time needed to analyze thecomplete picture[5].Time spent by a computer's central processing unit (CPU) carrying out the instructions of a program or operatingsystem is referred to as CPU time, also known as process time. Time spent in low-power (idle) mode or waiting for I/O activities accounts for the majority of the elapsed time.

Block Size	Elapsed Time (in Seconds)	CPU Time (in Seconds)
4x4	7.7197	3.0888
8x8	5.0510	1.1544
16x16	4.5638	0.6708
32x32	4.0711	0.6084
64x64	3.8789	0.4056

Table.1. Here's the elapsed time of CPU for the various block in size of the traditional BTC in city and coypa.jpg

Industrial Engineering Journal
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G. COMPRESSION TECHNIQUES

Compression methods are divided into the lossless and lossy categories according on whether or not the original,undistorted data can be reconstructed [1].

1) *Lossless compression:* With lossless compression, the encoded version of a picture faithfully reproduces the original.Under this method, every piece of data is considered vital.In fields like medical imaging where every bit of information must be preserved, a lossless compression strategy is employedto save images.

2) *Lossy compression:* By eliminating even more redundancies, lossy compression may achieve even higher compressionratios. Most applications, such as web surfing and video processing, make heavy use of lossy algorithms since they are efficient and the quality of the rebuilt picture is not critical. This is not an instance when it would be ideal to restore the picture to its original state.

3) *Entropy:* Identifying differences in the image's entropy is crucial for classifying different compression techniques.Any compression method will result in a smaller file size fora picture that has a low frequency, strong correlation, and low entropy. The effectiveness of a compression method optimizedfor one use case may suffer in another.

III. PROPOSED DESIGN VLSI ARCHITECTURE

The implementation of vlsi, suggested image compressor concept. It has predictor, and a modified Golomb Rice Encoder, a training module, a bitmap generator, and a parameter calculator. Because of the strong relationships between the three colour planes, the parameter calculator and the image generator has been developed to handle the green-coloured layer as the most representational of an RGB picture. To further enhance compression efficiency, the image generator only creates bitmaps for the green layer. The parameter converter not only gives you the bitmap generator's thresholds, but also the information you need to search up the fuzzytable that will tell you what kind of block your sub imagewill be. After a choice has been chosen, it stays that wayuntil the following sub-image arrives. The representative levelsthat are most faithful to the original picture are identified by the training module. The training module additionally supplies2-level numbers (xh and xl) for the predictor, and for theGolomb-Rice encoder for each sub-block so that the packer may create bit streams.

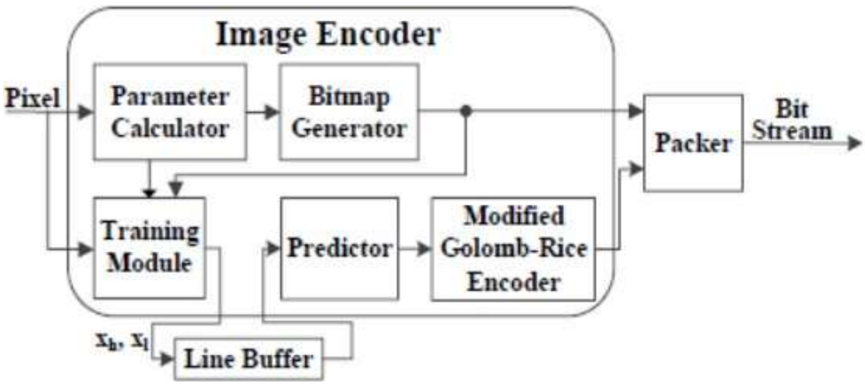

Fig. 3. The proposed hardware architecture of compressor block diagram

A one-line buffer and a predictor work together in the suggested picture compressor. The prediction error is providedto the Golomb-Rice encoder through this single-line buffer, which also stores the representative levels. Lastly, a packer module was introduced to separate block-type, bitmap, and Trade - off between risk coding because the length of code corresponding to given location memory that is 16 bits. Packerparallel produces a 16-bit signal when the length is more than 16.

The parameter calculator determines the average, maximum,and lowest values for each 4x4 grid cell of the sub image. Aftercompleting the calculations for the third 44 block, the results for the fourth block were stored in the registers tempMean, tempMax, and tempMin. After processing all 4x4 blocks inthe sub image, the parameters were prepared to begin the computation using the approach given in educated fuzzy table,to identify a block kind. When the sub-image is divided up, the average, maximum, and minimum values will be adjusted. In the case of the mean, four 4x4 blocks would stand forfour different averages. If the chunk G is used, then newMean 1 or Newman 2 are both the same as the mean ofthe two subsets, mean1 and mean2. Both the newMean3 and newMean4 sum to zero, just as the mean3 and mean4 do. Figure depicts the VLSI layout for the planned BTC training module. To determine acceptable sample levels xh and xl, it is utilized to calculate the minimal value of MSE and in order to save money on hardware, it is possible to traintwo representative levels, xh and xl, at separate times usingthe same training module. Also, hardware sharing technology decreased the amount of memory needed to compute MSE. Equation was first used to teach the xl. When the current bitof the bitmap was 0, the accumulation for MSE was consideredsince xl substituted 0 to rebuild the picture. After varying 2 between 0 and 1, the training session returned xl, the valuethat minimized the mean squared error. The xh was then taughtthe same techniques. Moreover, most functions were designedusing the adders, shifters to lower the hardware cost. Because MSE determined the representative levels, the BTC training module simply required a single multiplier. To reduce the costof the hardware is to be suggested compressor design, the proposed algorithm may be implemented using the hardware sharing, adders, multiplexers, shifters.

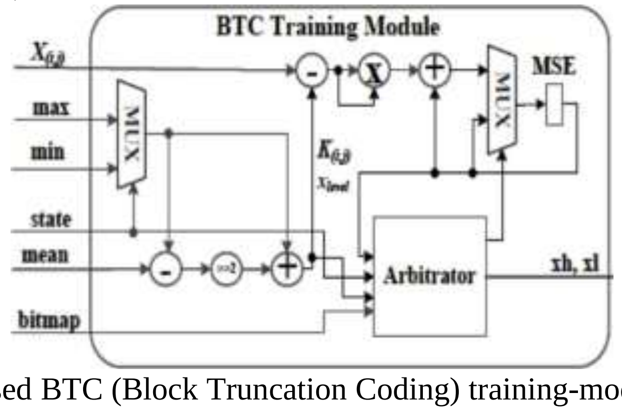

Fig. 4. The Proposed BTC (Block Truncation Coding) training-module blockdiagram

IV. VLSI ARCHITECTURE FOR IMAGECOMPRESSION

A. Symmetric filtering-based VLSI architecture for image compression:

Instrumentation for symmetric filtering picture compressionis supplied. The hardware consists of an N-element shift circuits with an equivalent number of shifting blocks (SB)for storing and rearranging data. Each piece of information stands in for a single picture pixel. A first set of adder circuits is included to aggregate information from a set of N SB pairs. Further to the first set of adder circuits, a second set of adder circuits is provided for combining information from a differentset of N SB pairs. The equipment also has a first multiplicity ofmultiplier circuits, which are responsible for multiplying the sums produced by the adder circuits by the relevant low pass coefficients. The second set of adder circuits performs adds, and the second set of multiplier circuits takes those

Industrial Engineering Journal
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numbers and multiplies them by the relevant high pass coefficients.

B. Description:

1) *Field:* This innovation is about processing signals and images. In particular, the current invention is related to the compression of images.

2) *Background Information:* Every signal may be thought of as a collection of sinusoidal waveforms at different frequency when analyzed using standard Fourier transformations. To successfully approximate signals with severe discontinuities, such as the edge characteristics of pictures or signals codedfor digital communications, Fourier transforms are not as well suited to be used for signals with repetitive behavior, such as voice signals.

Images may be represented in the frequencies and spatial domains using wavelets. As a result of quantization effects, wavelets create less undesired visual effects than a block-baseddiscrete cosine transformation (DCT). In order to describe signals with discontinuous characteristics, the Wavelet analysis- based Wavelet Transform (DWT) was created as an alternativeto the Fourier transform. To get an approximation of a signal, the DWT uses discrete samples rather than continuous ones, making it a discrete technique. Given the discrete nature ofthe transform, digital logics like Very Wide Scale Integrated (VLSI) circuitry may be used to implement the DWT. Hence, DWT might be built onto a chip alongside other digital element. The core idea of DWT is to split a signal up into many frequency bands. An appropriate encoding scheme might be applied independently to each of these sub-bands. It is possibleto further subdivide each sub-band into even more specific sub-bands if necessary. When calculated on a general-purpose computer, DWT takes a very long time because of its high computational complexity. A dedicated bespoke VLSI device might be utilized for DWT, capitalizing on the inherent data parallelism to achieve a high throughput and, by extension,a high data rate, making it suited for real-time applications. There are several suggested VLSI designs for DWT.

Unfortunately, these intricate layouts often need a lot of physical space on the computer’s part and result in hardware usage rates that are far below 100 percentage. It would be helpful to have a new DWT design for image compressionthat uses fewer components.

V. SUMMARY

To sum up, one application of the present invention offers a device for carrying out symmetric filtering picture compression. The hardware consists of an N-element shift circuits with an equivalent number of shifting blocks (SB) for storing and rearranging data. Each piece of information stands in for a single picture pixel. A first set of adder circuits is includedto aggregate information from a set of N SB pairs. Further to the first set of adder circuits, a second set of adder circuitsis provided for combining information from a different setof N SB pairs. The equipment also has a first multiplicity of multiplier circuits, which are responsible for multiplying the sums produced by the adder circuits by the relevant low pass coefficients. The second set of adder circuits performs adds, and the second set of multiplier circuits takes those numbers and multiplies them by the relevant high pass coefficients.

A. VLSI Architecture of Fuzzy Logic Hardware Implementation

This work contributes to the literature by presenting the results of research into the VLSI architectures of various fuzz processor and controllers tailored to different uses. In orderto provide minimal silicon area, high operation speed, and flexibility across multiple application domains, the research investigates the VLSI design of fuzzy logic hardware. In this work, we take a look at the fuzzifiers, de-fuzzifiers, inference, and rule bases that make up fuzzy processors, as well as their circuit or architecture level designs. The efficiency of these various parts has been compared.

It has been noted that these fuzzy processors have room to grow in terms of power consumption, processing speed, foot- print, and reliability. Based on the research results, it is clear that due to the complexity of the calculations they manage, more attention should be placed throughout the design processon the performance of inference engines and defuzzification units. A substantial performance boost is realized across the board as a consequence of the optimization work done on thesesubsystems. About 30 years have passed since Lotfi Zadeh [1- 6] first proposed the concept of fuzzy logic, and in that time, the theory has seen widespread implementation across many industries. Control system, consumer electronics, household appliances, data analysis, decision making analysis, intelligentagents, computer vision, signal processing, and many more areas have all found uses for fuzzy logic. Moreover, fuzzy logic is a great tool for modelling human behavior.

B. Fuzzification

In the theory of fuzzy logic, fuzzification plays a crucial role. The operation of smoothing out a sharp number. Fuzziness, uncertainty, vagueness, or ambiguity are introducedinto the sharp number during the conversion. While they may seem precise, numbers in the actual world sometimes conceal significant degrees of ambiguity or vagueness. A

membership function may be used for representation of thedegree of uncertainty, ambiguity, or imprecision associated with fuzzy number.

C. Defuzzification

1) Real-time applications need less-fuzzy data, thus theresults of the fuzzification process must be crisped up before they can be used. Defuzzification, often some- times referred to as rounding off, is the process by which fuzzy data is transformed into a more preciseformat. As a result, the whole set of membership value values may be summarized into a single number. Several techniques for removing uncertainty from data that havebeen presented in the literature.
2) Maximum membership theory 1.
3) The Centroid Formula 2.
4) A third option is the weighted average technique.
5) Membership in the mean-max club, number four.
6) Fifth, the midpoint of the totals.
7) The sixth place, the biggest area’s center.
8) Which comes first, the maximum or the minimum.

D. IMAGE DATA COMPRESSION

Throughout the last decade, picture data compression has emerged as a popular study topic in the field of image processing. Information may be compressed to take up less space on a storage medium by using a more efficient encodingscheme. If you do this, you can reduce the number of bits and bytes needed to hold the same amount of data. In practice, less bandwidth is needed for transmission, and less space is neededfor storage. This study looks at the feasibility of using low-power VLSI technology to construct an image compression algorithms approach that may be employed in real-world coding systems. In real life, an image is often specified at its inception over a huge matrix of picture components (pixels), for each pixel typically representing a grayscale value with 8 or 16 bits of precision. This depiction may be too big to easily save or send. Compressing a picture allows us to store more information in a smaller file while still maintaining much of the original’s quality. The

Coding and decoding methods are based on discrete cosine transform (DCT) are widely usedin Realtime settings. VLSI DCT processing chips have now become crucial in real time coding systems. Still photos with continuous tonal ranges may now be coded and compressedto an international standard thanks to JPEG. It is popularly known as that of the JPEG standard. In order to facilitate VLSI implementation of information compression, the JPEG standard's principal goal is to offer a general, application- independent picture compression algorithm. Because of its increasing importance, the DCT core in image compression systems warrants in-depth research into its efficiency and practicality. The design focuses primarily on meeting the needs of the intended use. Data transmission methods have come a long way in the last decade, and the explosion of the Internet has led to a rise in the demand for their use, particularly inthe realm of multimedia. Transferring uncompressed audio andvideo data requires a massive data transmission bandwidth.

The Discrete Cosine Transform (DCT) and its inverse (IDCT) are two of the many methods that have developed to compressmultimedia streams. In the realm of digital technology, thestudy of image compression is an important one. Bitmaps usedto store digital images may sometimes include hundreds of megabytes of information, which places a heavy burden onthe system in terms of both processing time and CPU use.Data samples that are highly correlated include a great deal of unnecessary detail, while a small number of uncorrelated data points may more accurately portray the same facts. Data compression relies on the identification of redundancies, such as coding redundancy, inter-pixel duplication, and psycho- visual redundancy. When there is a need to represent the sourceinformation with less data, we have a data redundancy. Whena number of these redundancies are eliminated, compressionis accomplished.

Intuitively, reducing the amount of data by excluding irrelevant details should have no negative effects on any relevant details. But, visual redundancy in the mind does not workthis way. Lessening redundant coding is the most direct path to better compression. Using more data than required to communicate the intended meaning is increasing the image's entropy. Entropy coding describes a class of lossless redundancy reduction compression methods. Inter-pixel redundancyelimination is a further method of compression. Due to the strong correlation between neighboring pixels, just a small portion of each pixel's value has to be sent when transmitted inplace of the whole value. The same holds true for neighboringblocks, but not to the pixel level.

It is advised that only encoding redundancy be minimizedor removed in order to generate loss less compression. Inother words, the decompressed version of the picture will bea perfect match for the original. Since the precise pixel value may be retrieved using differential coding or run length coding,interpixel errors can also be eliminated. The term psycho-visual redundancy describes how the visual system of humans interprets an image in such a manner that removing this redundancy results in an image that is practically unrecognizableby human viewers.

1. ***Principle behind the compression:***

i. Cutting down on redundant data in a picture reduces the number of bits needed to describe the image's content.In general, redundancies may be divided into three categories: Images have three types of redundancy with the goal of decreasing the number of bits neededto describe a picture, researchers in the field of image compression attempt to do away with as much redundantinformation as they can in terms of both the image's spatial and spectral components.

ii. There are three potential outcomes here i.es., n1=n2, therefore CR=1 and RD=0, indicating the original picture which have no redundant pixels.

Coding redundancies, inter-pixel (spatial) redundancy, and psyche visual redundancy are all explored in image compression and coding methods. Reduced redundancies allow for compression.

2. Coding Redundancy:

Image entropy, in the sense that more information is stored than is strictly required, is increased. This problem may be solved by using codes of varying lengths. Huffman codes and the arithmetic codingmethod are two examples of picture coding techniques that investigate coding redundancy.

3. **Inter-pixel Redundancy:** Redundancy in space, in between frames, or in geometry. It takes use of the fact that pictures often.

VI. EXPERIMENTAL RESULT

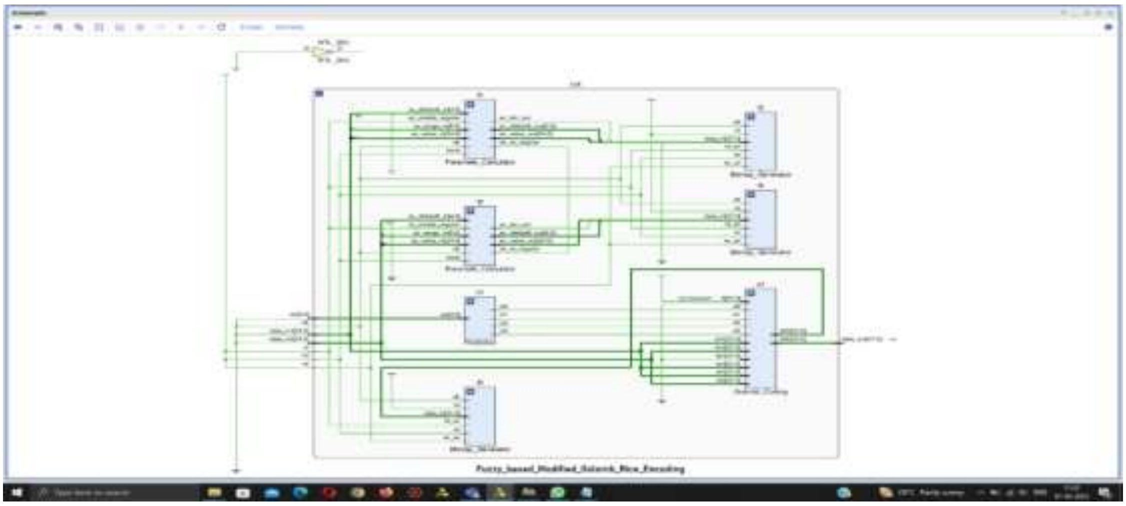

Fig. 5. Fuzzy based modified golomb rice encoding internal

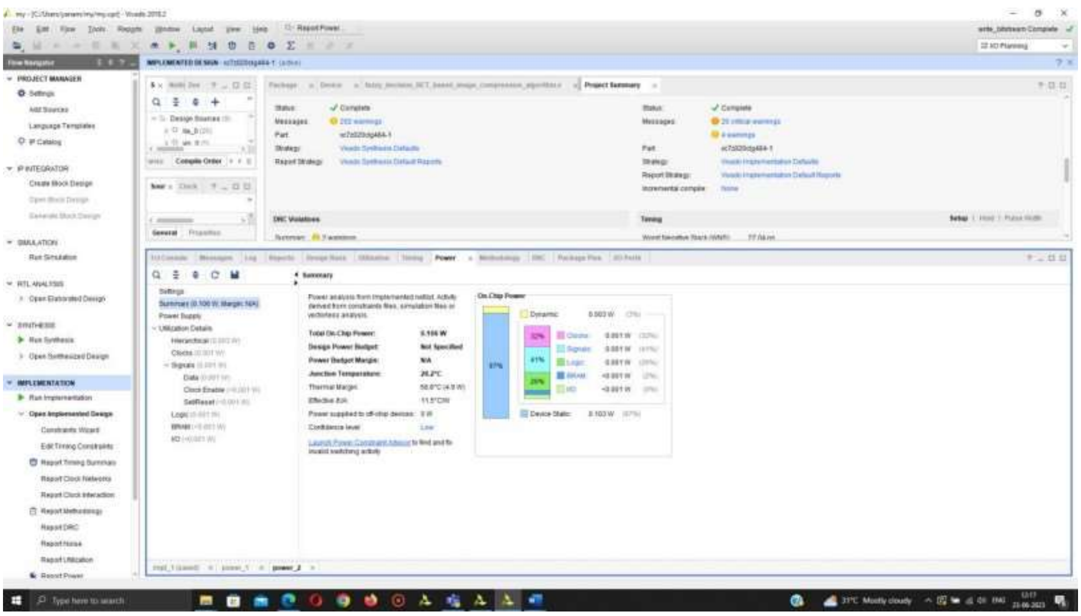

Fig. 6. Power

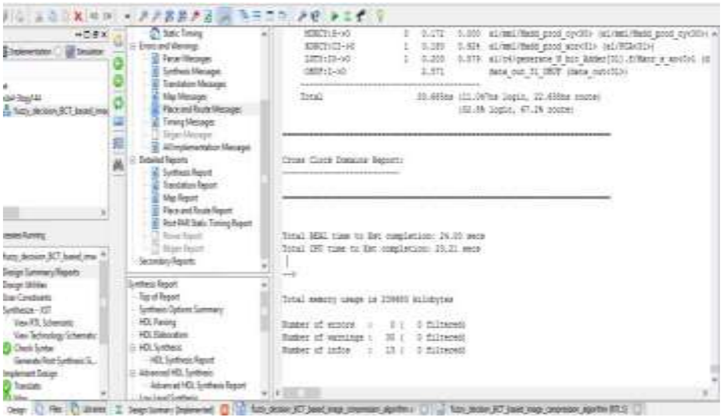

Fig. 7. Delay

VII. COMPARISON

	[3]	[4]	[5]	[6]	[2]	This work
Algorithm	JEPG	JEPG	JEPG-LS	JEPG-LS	4X4 BTC	Halfton & BTC
PSNR	35.53	35.53	45.53	45.53	31.02	28.33
Compression Ratio	12.41	12.41	1.94	1.94	7.14	14.58
Process	TSMC 0.6um	TSMC 0.13um	FPGA	UMC 0.18um	TSMC 0.18um	FPGA
Operating Frequency	40 MHz	100 MHz	21 MHz	40 MHz	100 MHz	100 MHz
Power	310	260	N/A	8.2	2.91	3.11
Delay	123.364ns	165.35ns	N/A	82.95ns	65ns	33.685ns
Core area(um2)	288 k	283 k	N/A	12.6 M	81 k	60 k
Memory	1 frame	1 frame	1 frame	1 frame	1 frame	1 frame

Table.2. comparison between binary-weighted dac and proposed design.

VIII. CONCLUSION

In conclusion, this paper introduces an innovative picture compression algorithm that leverages digital half-toning, block truncation coding, fuzzy judgement, and block partition approaches. The algorithm is designed with a strong focus on hardware efficiency, boasting low complexity and memory requirements. By introducing novel techniques such as variable size blocks and fuzzy judgement algorithms for block truncation coding, this study successfully enhances both picture quality and compression ratios. The integration of Huffman encoding further contributes to improved compression ratios. Additionally, the development of an advanced entropy encoder plays a crucial role in achieving even higher compression efficiencies. Notably, this research surpasses previous image compression methods in terms of gate count reduction, with a minimum reduction of 20.9 percentage, and in the evaluation of the Figure of Merit (FOM) value. These achievements collectively mark a significant advancement of image compression, offering a valuable contribution to both hardware oriented and quality-driven approaches.

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