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DESIGN FAULT TOLERANT BIST USING WEIGHTED TRUE RANDOM NUMBER GENERATOR DEVICES

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ABSTRACT

A built-in self-test's fault coverage can be decreased by weighting the pseudorandom test pattern that a test pattern generator generates. The primary aim of this study is to introduce a novel weighted Transition Probability Graph (TPG) for a Built-In Self-Test (BIST) architecture that relies on scan chains. This research aims to produce efficient weighted motifs that will enable scan chains to be constructed with reduced power and space requirements. In addition, the TPG pseudo-primary seed is optimised so that the weighted pseudorandom designs have a substantial length. The implementation of maximum-length weighted patterns is achieved by utilising a weight-enabled clock to assign distinct weights to the different scan chains. This approach effectively mitigates power consumption and minimises hardware overhead. Furthermore, the proposed weighted Transition Probability Graph (TPG) demonstrates a high level of accuracy when implemented on two separate test-per-scan Built-In Self-Test (BIST) architectures. The simulation results are examined using a Xilinx platform. To achieve the performance goals, it is also necessary to alter the suggested weighted TPG to a higher bit TPG and compare the results.

Keywords: weighted TPG, BIST architecture and Verilog HDL.

1. INTRODUCTION

Low-power systems for high-speed designs in very-large-scale integration (VLSI) technology have been emphasised recently. Several design solutions have been used to balance performance, power, and space. Some BIST systems prioritise low power usage

during regular operation over when performing a test. BIST test mode execution requires scan chain switching and the right test pattern generator (TPG) for test data compression. In addition, it is imperative to conduct thorough testing in semiconductor designs with a focus on achieving optimal reliability and sensitivity. Figure 1 depicts a typical Wu-Shiung Feng functioned as the assistant editor who oversaw the evaluation of this submission and granted final clearance for publication.

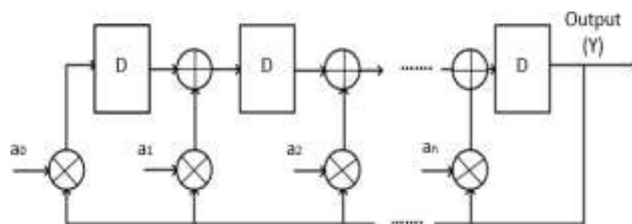
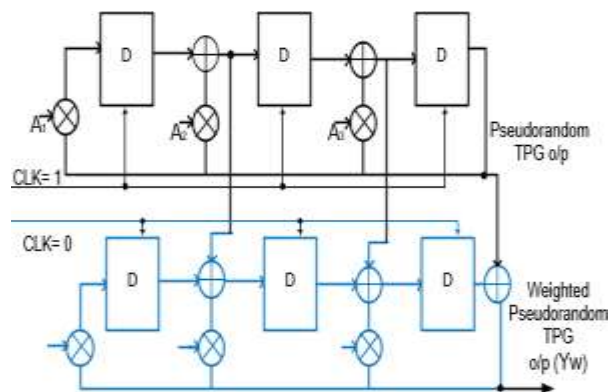


Fig 1. An example of a conventional pseudorandom TPG

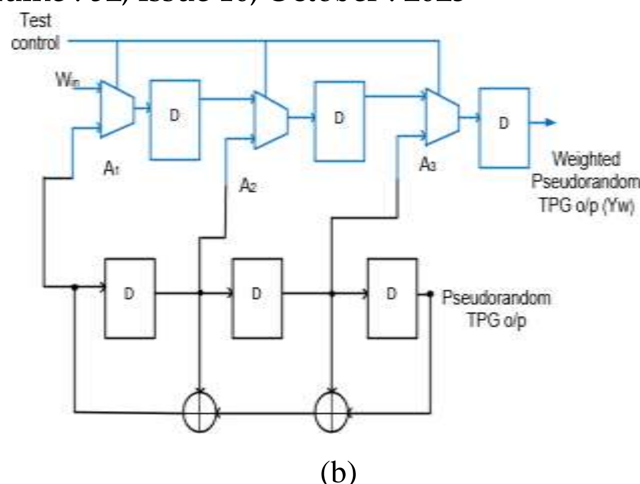
The True Pseudo-Random Generator does pseudo-random things. Seed bits (a0, a1, a2,..., an) are fed into the TPG's (Test Pattern Generator's) n shift registers. Based on the shift register's (n 1)-th bit, the i-th clock cycle constantly modifies the (i-1)th clock cycle. TPGs use parallelism in many practical applications to meet high-yield requirementsThe linear function of TPG is implemented with the help of the output feedback signal and the input seed bits.The linear features of this system find applications in aerospace, instrumentation, medicine, communications, entertainment, and energy production and distribution.

The outputs generated by a TPG exhibit characteristics such as exhaustiveness, determinism, pseudo randomness, pseudorandom-weightedness, and mixed-mode behaviour. A number of Built-In Self-Test (BIST) architectures utilise output weighting based on pseudorandom patterns to enhance the detection of defects. The weighted pseudorandom test pattern generator (TPG) demonstrates both actual randomization and the presence of recurring patterns within each clock cycle. Regarding test-per-scan Most Built-In Self-Test (BIST) uses a single seed bit to generate a test pattern during each scanning phase cycle. In this case, n signifies scan chain length. Recent research shows

that scan shift cycles reduce switching activity. To reduce power usage, the TPG automates weighted parameter determination. Weighted pseudorandom test pattern generation (TPG) reduces switching transitions. However, the solutions required more power and space due to supplemental XOR transitions between shift registers. The proposed approach successfully mitigates the inherent problems. The prioritisation of fault coverage, weighted switching activity, power consumption, and area overhead should be considered while establishing the BIST criterion. Two methods can be used to fulfil these needs. One is to change the weighted TPG's circuit layout. The alternative is to upgrade the weighted TPG with new hardware. So, using additional hardware, a novel pseudorandom-weighted TPG is built in this research. Additionally, greater fault coverage is attained by using test-point insertion to obviate transition delay problems. A phase shifter is used in the proposed method to transfer weighted test patterns to the scan chains.



(a)



(b)

Fig 2. An example of an existing 3-bit weighted pseudorandom TPG: (a) redundant TPG; and (b) TPG;

This scenario is similar to exchanging weighted patterns used to choose scan chains in front of those with the smallest area. Consequently, all scan chains in the BIST design employ weighted patterns. This improves fault coverage and eliminates defects at a specified output. The TPG effectively improves switching activity and decreases average power consumption for scanning and recording during BIST test-per-scan, owing to its selection of weighted patterns.

Logic gates are used in the TPG's implementation. The technology was put through its paces on a Mentor Graphics IC station and tested with a 0.13 m submicron SilTerra process. The article's remaining sections will follow this format: In Section II, we go over the details of the current weighted pseudorandom TPG. Our original weighted pseudorandom TPG proposal can be seen in Section III. The TPG is mathematically analysed to show how a set of pseudo-primary seeds can simultaneously reach their maximum-length weighted patterns.

2. LITERATURE SURVEY

J. Zhou, Z. Cao, X. Dong, and A. V. Vasilakos, "Security and privacy for cloud-based IoT: Challenges," The Internet of Things (IoT) represents the forthcoming paradigm shift inside the realm of the Internet. The technology facilitates the connection and communication of a vast number of gadgets, enabling them to exchange data and augment

our everyday lives. In contrast, cloud computing facilitates the seamless integration of data from diverse sources by offering flexible and scalable access to computing resources, allowing for on-demand network connectivity and resource sharing. Both cloud and Internet of Things (IoT) installations encounter several challenges that impede their progress. The Cloud has the potential to transcend its existing restrictions related to physical items in a more dynamic and distributed manner, thanks to the abundance of Cloud-based resources that can be accessed through the Internet of Things. This article presents a comprehensive examination of the integration between the Cloud and the Internet of Things (IoT), focusing on the advantages and obstacles encountered during the integration process. This paper will also discuss the architecture and distinctive application scenarios of the resulting cloud-based Internet of Things (IoT) paradigm. In conclusion, this study highlights the presence of unresolved inquiries and prospective avenues for further investigation.

3. APPLICATION OF PROPOSED WEIGHTED TPG IN TEST-PER-SCAN BIST ARCHITECTURE

WEIGHTED PSEUDORANDOM TPG USING THE GALOIS OPERATION WITH A PHASE SHIFTER

The weighted TPG that is being presented exhibits various advantages in comparison to existing approaches. These advantages include a reduction in switching transitions as a result of the utilisation of certain weighted patterns, as well as a decrease in power consumption due to the architecture's reduced number of hardware components. This reduces hardware overhead and improves Built-In Self-Test (BIST) fault coverage. The suggested TPG approach is depicted in Figure 1 and makes use of Galois operations and weighted pattern hardware. The black dashed line in the proposed TPG denotes the Galois operation. This operation simplifies constant pseudo-primary seed use (A, X). The same subset of primary seeds can be used to increase persistent seed bits. The employment of seed subsets enables the achievement of a higher degree of weighted patterns while minimising the occurrence of switching activity. The blue line in the diagram illustrates the inclusion of supplementary hardware that effectively produces A weighted

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pseudorandom TPG output while minimising the number of components required.

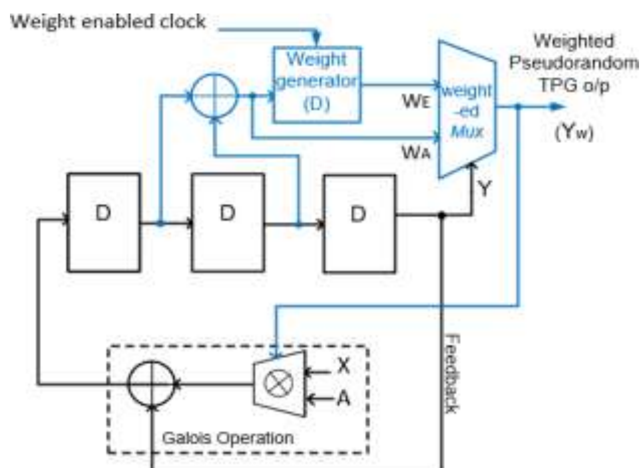

Fig 3. Proposed 3-bit weighted pseudorandom TPG.

Additionally, a weighted algorithm is incorporated into the auxiliary hardware layout. Consequently, the m-bit Test Pattern Generator (TPG) is implemented by employing shift registers that operate with asynchronous timings. The pseudo-primary seed bit, A, is continually multiplied by X. The product, Z, is then added to the test vectors. Additionally, the registers are configured to execute many TPG layers simultaneously. Therefore, the arrangement of the feedback loop is employed to define the state that follows the i-th state, denoted as the (i+1)-th state. The proposed TPG design makes advantage of the Galois operation, which strengthens the constant pseudo-primary seeds even further. The expansion of this concept can be achieved by the utilisation of Galois field Lemma 1, which enables the identification of subsets pertaining to first pseudo-primary seeds.

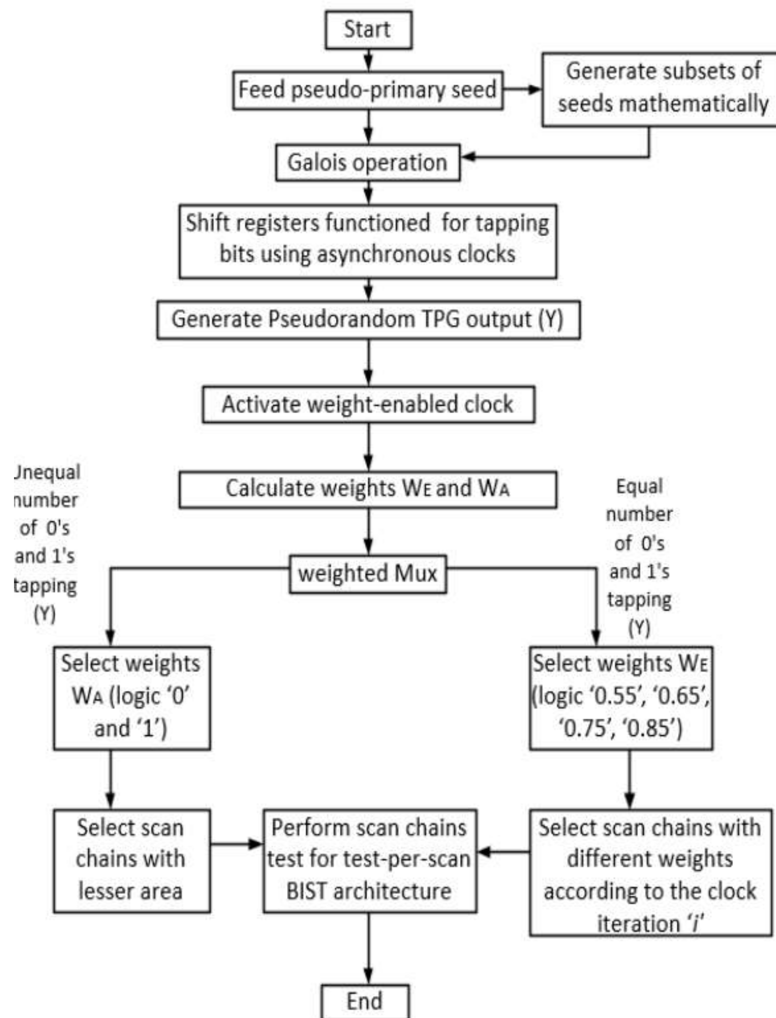

Fig 4. Flowchart of the proposed weighted pseudorandom TPG operation

1) The weighted patterns WA created with probability of assigning a '0' or '1' to specific scan chains take up less space. The weighted Mux's output is dependent on the seed inputs' crucial attribute of pseudorandomness. Suppose the recommended 3-bit TPG's Galois operation (Z) value swaps Y0 with Y1, Y2, and so on till Yn. In this case, Y2 is the Mux's selection input. The weighted pattern is established by this. As a result, it is possible to reduce switching transitions overall by 25% in the scan chain's major inputs.

2) Upon cycling through the shift registers, the weighted multiplexer (Mux) is responsible for selecting the weighted patterns WE. The number of '0' and '1' values in the pseudorandom output (Y) must be equal for this choice to be valid. The probability is 0.55

when the two inputs to the i-th scan cell are close. There is a 0.75 percent chance that the two scan chain cells will be joined.Scanning chains with the same input vectors and transition probabilities are all given the same stochastic value of 0.65. The probability of the remaining scan chain cells is 0.85.

WEIGHTED TPG IN TEST-PER-SCAN BIST ARCHITECTURE

Typical elements of a BIST architecture include

- TPG - Test Pattern Generator
- TRA – Test Response Analyzer
- Control Unit

TEST PATTERN GENERATOR (TPG)

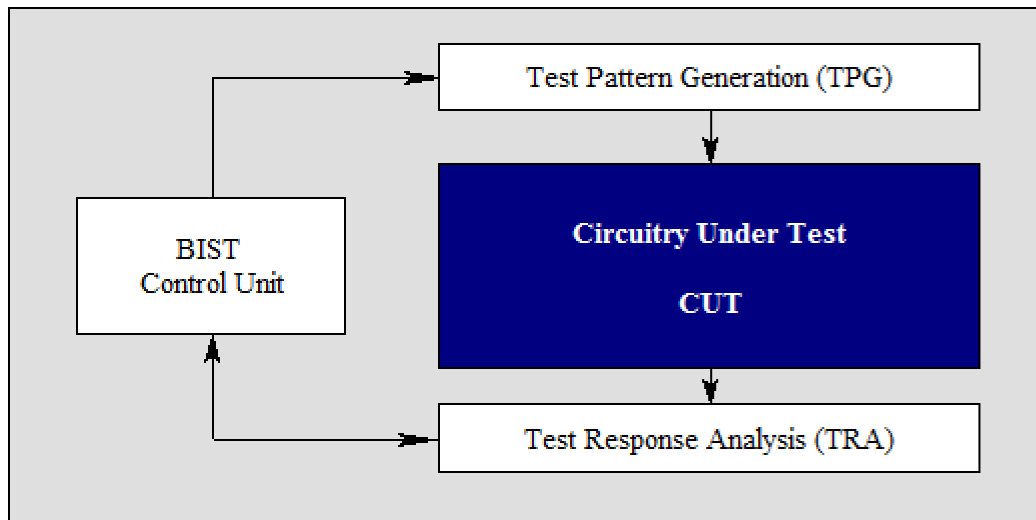

Fig 5. BIST architecture

For CUT, it generates test patterns. It will either be a microprocessor or a specialised circuit. predetermined sequence or pseudo-random numbers may be used to generate the pattern. Here, the random number is generated using a weighted pseudorandom TPG.

TEST RESPONSE ANALYZER (TRA)

When TRA examines the MISR output and compares it to the weighted pseudorandom TPG input, it determines if the result is incorrect or not.

BIST CONTROL UNIT

All processes are controlled by a control unit. The control unit's primary functions are to configure the CUT in test or regular mode, to feed seed data to the weighted pseudorandom TPG, and to control MISR and TRA. An interrupt will be generated if an error occurs. The interrupt_clear_i signal can be used to clear interrupts.

CIRCUIT UNDER TEST (CUT)

The component referred to as CUT, which may be a circuit or chip, will be utilised for the application of Built-In Self-Test (BIST) techniques in order to detect mistakes that are consistently fixed at either zero or one.

4. RESULTS

RTL SCHEMATIC: RTL, or register transfer level, is an acronym for the architecture's blueprint. It is used to contrast the designed architecture with the yet-to-be-developed ideal architecture. Using the coding language known as verilog or vhdl, the hdl language is used to transform an architecture's description or summary into a working summary. Internal connection blocks are also defined in the RTL schematic for convenience of study.The following image depicts the RTL schematic diagram of the proposed architecture.

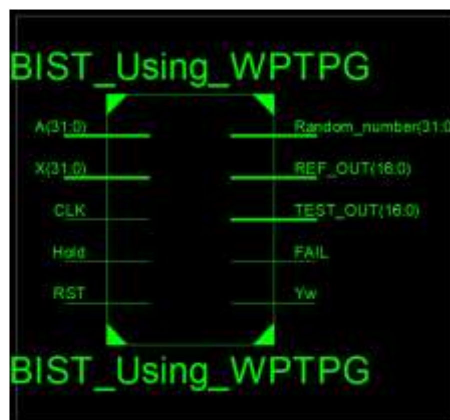

Fig 6. RTL Schematic view of TPG based BIST

TECHNOLOGY SCHEMATIC: The technological schematic produces a visual representation of the architecture in Look-Up Table (LUT) format, which serves as an area parameter in Very Large Scale Integration (VLSI) for estimating the design of the architecture.The memory allocation of the code in the Field-Programmable Gate Array's (FPGA) Look-Up Tables (LUTs) is visually represented as a square unit.

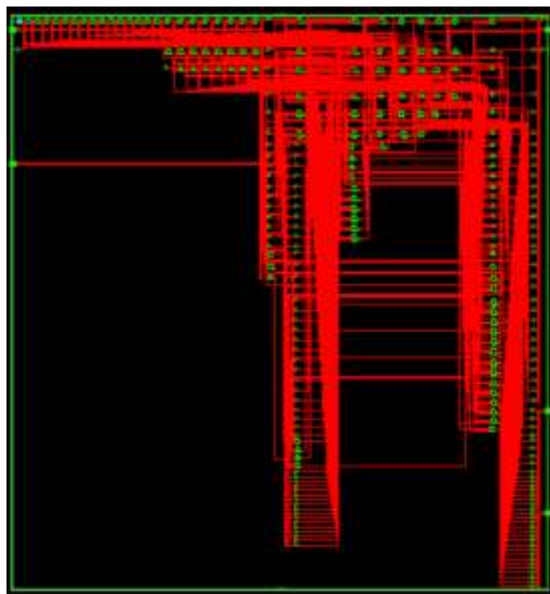

Fig 7. View technology Schematic of TPG based BIST

SIMULATION: The simulation is the process, while the schematic evaluates the connections and construction components. The tool's home screen changes from implementation to simulation when the simulation window is accessed, and the simulation window restricts output to wave shapes. In this instance, it is versatile enough to support multiple radix number systems.

Fig 8. simulated wave form of TPG based BIST

PARAMETERS: Area, delay, frequency, and power are four variables that are considered in VLSI; using these variables, one can compare one architecture to another. Here, area and power consumptions are taken into account. Verilog language HDL and the tool

XILINX 14.7 are used to acquire the parameters.Any design that has higher frequency will progress more quickly.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	35	93120	0%
Number of Slice LUTs	63	46560	0%
Number of fully used LUT-FF pairs	19	79	24%
Number of bonded IOBs	134	240	55%
Number of BUFG/BUFGCTRLs	1	32	3%

Table1. device utilization summery

Minimum period: 1.052ns (Maximum Frequency: 950.570MHz)

Minimum input arrival time before clock: 2.542ns

Maximum output required time after clock: 4.986ns

Delay 4.986ns

CONCLUSION

In this research, we present a unique low-power weighted test pattern generator (TPG) for producing weighted patterns efficiently. Patterns of maximum length and minimum transition weights are generated by applying the Galois operation to a subset of the initial pseudo-primary seed bits. The weighted multiplexer (Mux) in the design is used as a phase shifter to control the rate of switching between scans in the test. The proposed weighted TPG now employs a 32-bit TPG, guaranteeing efficient use of power throughout all clock cycles and cutting down on unnecessary storage requirements. The research found that fault coverage was enhanced when the architecture included Built-In Self-Test (BIST). In addition to sequential, redundant, scanning, and recording phase transition, and stuck-open faults, this investigation can also contain stuck-open faults. Built-In Self-Test (BIST) scan-forest architectures are also amenable to this method.

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