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OPTIMIZING NETWORK ON-CHIP COMMUNICATION WITH AND OPERATION-BASED STANDARD BASIC CODE ENCODING/DECODING

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Abstract:
In recent times, the code division multiple access (CDMA) technique has emerged as a highly efficient on-chip communication method for networks on chip (NOCs). To further enhance the performance and cost-effectiveness of CDMA NOCs in terms of area and delay, we introduce a novel encoding/decoding approach based on standard-basis principles. In our transmitter module, data from various senders undergo individual encoding using orthogonal codes from a standard basis. These encoded data are then combined through an XOR operation, resulting in the transmission of the combined data to their respective destinations via the on-chip communication infrastructure. Upon reception, the receiver module retrieves a sequence of chips by performing an AND operation between the combined data and the corresponding orthogonal code. A simple accumulation of these chips enables the reconstruction of the original data. To demonstrate the effectiveness of our method, we implemented the encoding/decoding technique in a CDMA NOC with a star topology. Comparative analysis with the state-of-the-art Walsh-code-based (WB) encoding/decoding technique revealed that our approach not only saves area but also reduces encoding/decoding latency. Furthermore, when applied to CDMA NOCs of different sizes, our encoding/decoding method demonstrates area savings and substantial improvements in maximal throughput compared to the WB CDMA NOC. The proposed architecture presented in this paper underwent rigorous analysis of logic size and area using Xilinx 14.6, providing additional evidence of its efficiency and practicality.
Keywords: smart farming, Artificial intelligence, Internet of Things, sensors.

I. Introduction

Over the last decade, network-on-chip (NoC) has emerged as a better communication infrastructure compared with bus-based communication network for complex chip designs overcoming the difficulties related to bandwidth, signal integrity, and having more Delay [1]. A significant amount of area of the NoC data transport medium is occupied by routers, which is predominantly occupied by FIFO buffers and routing logic. Accordingly, the probabilities of run-time faults or defects occurring in buffers and logic are significantly higher compared with the other components of the CDMA based NoC. With the rapid growth of the computational complexity more and more processing elements (PEs) are integrated onto a single chip and network on chip (NoC) has been proposed to address the versatility throughput and unwavering quality issues of on-chip communication. However ordinary packet switched NoCs experience the ill effects of nondeterministic transmission idleness and constrained open doors for parallel information exchange, since different streams can't overcome a connection in the meantime. To determine these issues the CDMA system as a compelling technique for actualizing elite on-chip communication was connected to NoCs. The beforehand proposed CDMA NoCs depend on a computerized encoding and translating technique requiring that the spreading codes have both orthogonal and adjusted properties. To this end the Walsh code is ordinarily utilized. However, the Walsh-code-based (WB) encoding and translating strategy has inalienable deficiencies which are given as takes after.

1)Design Complexity: In the encoding strategy, a math expression logic unit, whose logic overhead increments with the quantity of senders, is utilized to combine coded information. In the interpreting strategy a key demux accumulation contrast unit is utilized with recover the source information from blended information chips (in this short each piece of a spreading code is known as a chip and hence

the encoded information is called information chips). This unit is in any case, zone expending.
2)Low Code Utilization: In a S-chip Walsh code set S must be equivalent to 2N, where N is a characteristic number, and at most S − 1sequences can be utilized to encode the first information. This outcomes in a misuse of arrangements in the code set. For instance, a 16-hub organize needs a 32-chip Walsh code set on the grounds that a 16-chip Walsh code set can just give 15 arrangements to information encoding and it in this manner can't fulfill the necessity of 16 successions one for every hub.
To address the previously mentioned shortcomings, we propose another standard basic Based (SB) encoding/translating technique, which beats the WB encoding/deciphering strategy. The SB encoding/interpreting strategy can be connected to any CDMA NoCs to enhance their execution. The CDMA technique is becoming extremely popular in interconnecting mechanism of IP core for its efficient utilization of the data transfer among the IPs, to achieve higher throughput and less latency currently silicon chips that contain more and more number of transistors with 45nm feature size are available in the market, according to the report, the International Technology Road map for Semiconductors (IRTS), a single semiconductor chip will contain multi-billion transistors with a feature size around 22nm and clock frequency of nearly 35 GHz by the year of 2016.This growing manufacture capacity and demanding applications continuously increase the complexity of an System-on-Chip (SoC) to a higher degree in terms of number of system components and functionalities. Currently used bus architectures like Core connect for data transfer in an on-chip system have several disadvantages, bus arbitration and bandwidth limitations. To overcome the disadvantages of bus structure, the concept of Network-on-Chip (NoC) has been proposed as a solution to interconnect variable IP Core in system architecture.
The early design of NoC has emerged from SoC where the router is considered as a software running on to perform routing. The space and cost of SoC systems have motivated the researchers to find an alternate medium for performing the specified task with least cost and maintenance. The NoC is a combination of various components like buffer, processing unit and scheduling program are encoded with the design. The NoC systems replaced SoC systems based on the cost and maintenance. The purpose of NoC routers is to perform routing of the packet between various nodes of the network which are raised from various processes.

2.General working principle of CDMA
The general working of CDMA technology has two stages namely encoding and decoding as shown in Fig 1. The source node encodes the message utilizing the key selected, which is performed based on the orthogonal spreading codes. The orthogonal spreading codes maintain the uniqueness of the signature which will be distinct to each process and could be decoded by the pair of processes.

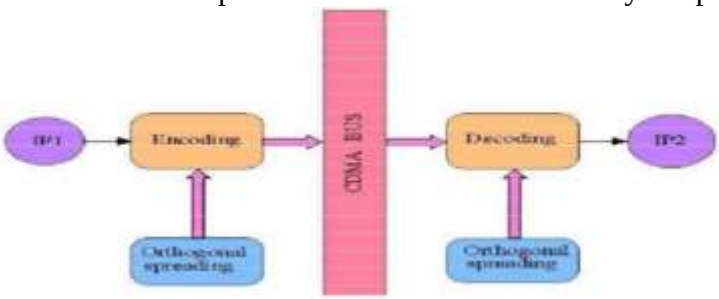

Fig: 1.The general working of CDMA technology
The processes use the code to encode the message and each process uses a different code which is visible for the subsequent pair of process. The messages or packets which are transmitted in the same channel will not feed the process and mesh up. At the sending end, the information from various senders are encoded utilizing an arrangement of orthogonal spreading codes. The encoded information from various senders are included for transmission without meddling with each other as a result of the orthogonal property of spreading codes.

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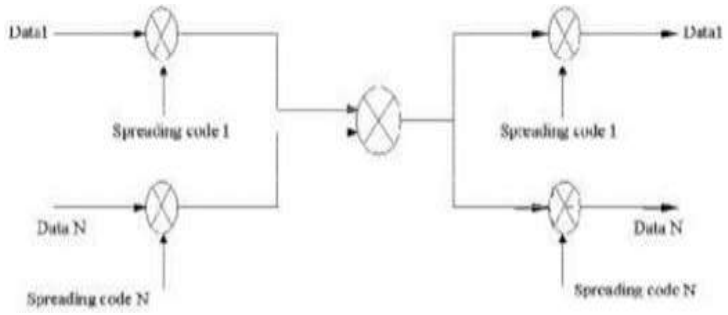

Fig: 2 Working principle of CDMA

Considering the orthogonal property, at the less than desirable end, the information can be decoded from the gotten whole flags by duplicating the got signals with the spreading code that are utilized for encoding. In the encoding plan, information from various senders are sustained into the encoder a little bit at a time. Every datum bit will be spread into S bits by XOR logic operations with an exceptional S-bit spreading code as shown in Figure 2. Each piece of the S-bit encoded information produced by XOR operations is known as an information chip. At that point the information chips which originate from various Senders are included mathematically as per their bit positions in the S-bit successions. All the main information chips from various senders are included and all the second information chips from various senders are included together thus.

Therefore, after the add operations, we will get S sum values of S bit encoded data. Then the binary equivalents of each sum value will be transferred to the receiving end. The scheme of applying the CDMA technique into on-chip communications has already been - proposed in several works. These works concern analog circuits to implement the CDMA technique, the representation of encoded data is in the form of continuous voltage or capacitance value of the circuits.

However, the data transfers through the analog circuits are challenged - in terms of coupling noise, clock skew problems and the variation of capacitance caused by manufacturing processes. Hence, a method of applying digital CDMA technique is proposed in this work. Figure 2.3 shows the general working principle of CDMA technique where the input data is encoded with the spreading code selected and forwarded to the receiving side. The received data will be decoded with the same on the other side.

3.CDMA Encoder

The WB unraveling plan is introduced in Fig. 4(a). As indicated by the chip estimation of Walsh code, the multibit entireties are amassed into positive part (if the chip esteem is 0) or negative part (if the chip esteem is 1). Thus, the two aggregators in the WB decoder independently contain a multibit viper to gather the coming chips and a gathering of registers to hold the amassed esteem. Through the examination module after the two collectors the first information is reproduced. If the estimation of positive part is substantial, the first information is 1. Generally, the first information is 0.

The SB unraveling plan is appeared in Fig. 4(b). At the point when the double aggregate flag touches base at recipients, an AND operation is taken between the twofold entirety and the relating orthogonal code in chip-by chip way. At that point the outcome chips are sent to an aggregator. After m-chips are collected (m is the length of the orthogonal code) the yield estimation of the aggregator will be the relating unique information. Note that there is constantly just a single chip equivalent to 1 and every other chip is equivalent to 0 for an orthogonal code in standard premise.

Consequently, the maximum collected an incentive in the SB aggregator is 1 and it can be put away in a 1-bit enlist. Along these lines, in the SB translating module just a single AND entryway and a gatherer with one 1-bit enroll are utilized bringing about less logical assets.

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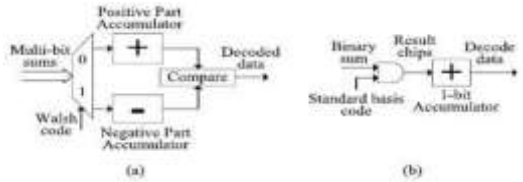

Fig: 4. Block diagram of decoding scheme (a) WB encoder. (b) SB encoder

4. Simulation Results

The simulation results for the comparison of Standard basis encoding and decoding with AND gate implemented in Xilinx ISE Simulator as shown in below figures. Area, delay is analyzed, and maximum throughput measured using Xilinx 14.6. A network is implemented in Verilog with 6,8 and 16 nodes.

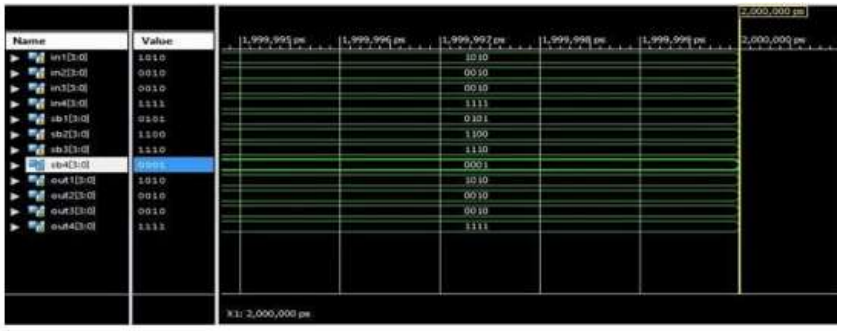

Fig.5. Simulation Results

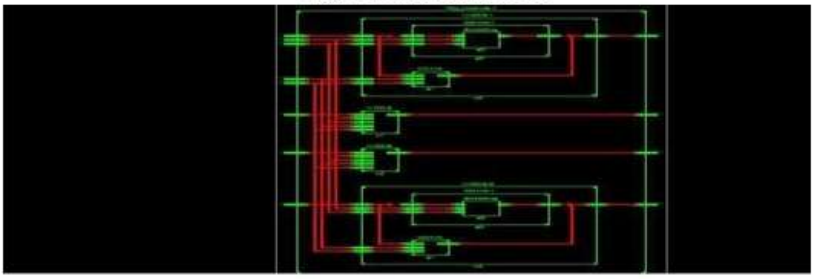

Fig.6. RTL Diagram for FIFO Buffers of CDMA based NOC Routers

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	1	4,800	0%	
Number of Slice LUTs	1	2,400	0%	
Number of occupied Slices	1	600	0%	
Number of MUXCYs used	1	1,200	0%	
Number of LUT Flip Flop pairs used	1			
Number of bonded IOBs	32	102	31%	
Number of RAMB18WERs	1	12	0%	
Number of RAMB8WERs	1	24	0%	
Number of BUFIO2/BUFIO2_2CLKs	1	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	1	32	0%	
Number of BUFG/BUFGMUXs	1	16	0%	
Number of DCM_ADVs	1	4	0%	
Number of ILOGIC2/ISERDES2s	1	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	1	200	0%	
Number of OLOGIC2/OSERDES2s	1	200	0%	
Number of BSCANs	1	4	0%	
Number of BUFHs	1	128	0%	
Number of BUFPLLs	1	8	0%	
Number of BUFPLL_MCBs	1	4	0%	
Number of DSP48As	1	8	0%	
Number of ICAPs	1	1	0%	
Number of PCILOGICSEs	1	2	0%	
Number of PLL_ADVs	1	2	0%	
Number of PMVs	1	1	0%	
Number of STARTUPs	1	1	0%	
Number of SUSPEND_SYNCs	1	1	0%	
Average Fanout of Non-Clock Nets	1.03			

Fig: 7 Device utilization Summary in Xilinx

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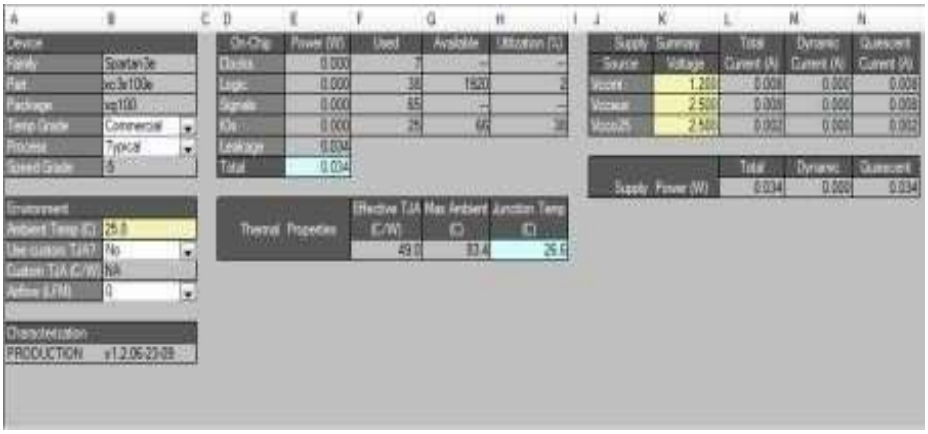

Fig: 8 Power Report of NOC

Power value =Maximum power achieves from both decoder and encoder of existing method – and proposed method Should be equal. By using twoencoding/decoding schemes we have compared the performance of CDMA Network on Chips. Besides the decoder module and encoder module, other on- chip modules, such as parallel-to-serial modules, serial-to-parallel modules and network scheduler areall included in the Network on Chips. Since both NoCs contain the parallel-to-serial module, scheduler module, and serial-to-parallel module, the percentage of power should equal of both Existing method and proposed method and area saving of the new code division multiple access, is as much as the previously calculated Standard basic code. However,the SB CDMA NoC reduces up to 50% of area saving in the form of average fanout of non-clocked nets.

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Timing Details:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 16 / 16
-------------------------------------------------------------------------
Delay:               4.372ns (Levels of Logic = 2)
  Source:            in1<3> (PAD)
  Destination:       out1<3> (PAD)

  Data Path: in1<3> to out1<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.579  in1_3_IBUF (in1_3_IBUF)
     OBUF:I->O                 2.571          out1_3_OBUF (out1<3>)
    ----------------------------------------
    Total                      4.372ns (3.793ns logic, 0.579ns route)
                                       (86.8% logic, 13.2% route)
```

Fig: 9 Timing delay of New CDMA Comparison

Technique	Area(µm)	Power Consumption	TIMING REPORT (Delay)
Existing Method (walsh based code)	2.00	0.014W	4.409ns
Proposed Method (Standard basic code)	1.00	0.014W	4.372ns

Table:1 Comparison of both existing and proposed methods.

The standard basis code with multiplexer using AND operation achieves low delay when compared to

Walsh basis code Encoding/decoding method. By using two different encoding/decoding methods we have compared the performance of Code Division Multiple Access Network on Chip. Delay value = Maximum Delay achieves from the both decoder and encoder of existing method - Maximum delay achieves from both decoder and encoder of proposed method /Maximum delayachieved.

CONCLUSION

In this paper Standard Basis Code Multiplexer with an operation for an on-chip interconnection network has been presented. Standard basis codes are used to modulate the packet data to handle many parallel data transfers. Compared to the existing Walsh basis code method, the proposed standard basis code of CDMA approach provides reduction in delay, and area and achieves maximum throughput. In the proposed method a lower number of gates is used than the existing method. So, it occupies less area than the existing one. Normally multiplexers are used in many areas for data transferring. Multiplexer sends digital or analog signals at higher speed on a single line in one shared device.

FUTURE SCOPE

Future work includes Design of Low Power & Reliable Networks on Chip through Joint Crosstalk Avoidance and Multiple Error Correction Coding.

REFFERENCES

[1] D. Sigüenza-Tortosa, T. Ahonen, and J. Nurmi, “Issues in the development of a practical NoC: The Proteo concept,” Integr., VLSI J., vol. 38, no. 1, pp. 95–105, 2004.
[2] A. J. Viterbi, CDMA: Principles of SpreadSpectrum Communication. Reading, MA, USA:Addison-Wesley, 1995.
[3] S. Shimizu, T. Matsuoka, and K. Taniguchi, “Parallel bus systems using code-division multiple access technique,” in Proc. Int. Symp. Circuits Syst., May 2003, pp. II-240–II-243.
[4] D. Kim, M. Kim, and G. E. Sobelman, “CDMA- based network-on-chip architecture,” in Proc. IEEEAsia-Pacific Conf. Circuits Syst., Dec. 2004, pp.137–140.
[5] X. Wang and J. Nurmi, “An on-chip CDMA communication network,” in Proc. Int. Symp. Syst.- Chip, Nov. 2005, pp. 155–160.
[6] E. H. Dinan and B. Jabbari, “Spreading codes for direct sequence CDMA and wideband CDMA cellular networks,” IEEE Commun. Mag., vol. 36, no. 9, pp. 48–54, Sep. 1998.
[7] M. Kim, D. Kim, and G. E. Sobelman, “MPEG-4 performance analysis for a CDMA network-on- chip,” in Proc. Int. Conf. Commun., Circuits, Syst., May 2005, pp. 493–496.
[8] X. Wang, T. Ahonen, and J. Nurmi, “Applying CDMA technique to network-on-chip,” IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 15, no.10, pp. 1091–1100, Oct. 2007.
[9] W. Lee and G. E. Sobelman, “Mesh-star hybrid NoC architecture with CDMA switch,” in Proc.IEEE Int. Symp. Circuits Syst., May 2009, pp. 1349–1352.