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A Novel Dual Output Schmitt Trigger Using Single Current Amplifier

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Abstract—**Schmitt trigger circuit utilizing a single second-generation Current Controlled Conveyor (CCCII) is proposed. The proposed configuration achieves a simple circuit with minimal components, requiring only one CCCII and two external resistors. Despite its simplicity, the design offers square wave outputs and has advantage of large bandwidth. Schmitt trigger circuits find the applications in the field of Biomedical applications, analog signal processing, communication systems, waveform generators, pulse width modulators, multi vibrators, flip-flops and in many other amplifier circuits. The proposed design leverages the inherent properties of CCCII to achieve sharp switching behavior, a key characteristic of Schmitt trigger. Cadence Virtuoso software with GPDK45nm technology files are used to test the topology, allowing for performance evaluation and verification. The design exhibits hysteresis, a crucial feature in Schmitt triggers that defines different switching thresholds for rising and falling input signals. This characteristic provides noise immunity and ensures clean switching behavior.**

Keywords— Schmitt Trigger, Current Controlled Conveyor (CCCII), Hysteresis, GPDK45, Cadence Virtuoso

I. INTRODUCTION

Schmitt trigger is a fundamental building block in analog and mixed-signal circuits, performing level shifting and noise shaping functions [1]. A conventional Schmitt trigger design typically utilizes operational amplifiers (op-amps) and passive components like resistors and capacitors. However, op-amp-based designs can be area-consuming and potentially power-hungry, especially in deep-submicron technologies like GPDK45.This paper presents a novel Schmitt trigger design that leverages the unique properties of a single second-generation current controlled conveyor (CCCII) to achieve efficient hysteresis behavior. CCCIIs offer controlled current transfer between different terminals, making them attractive alternative to op-amps in specific applications. The proposed design utilizes a single CCCII along with minimal passive components, resulting in a compact and potentially lower power alternative to conventional Schmitt triggers [2].

This paper presents a Schmitt trigger involving a single Current Amplifier (CA) to achieve a square-wave output. The following section highlights the fundamental advantages of the CA [3].

The manuscript introduces a new type of dual-output Schmitt trigger that uses just one second-generation current-controlled conveyor (CCCII), along with two resistances and a capacitor. This setup makes it suitable for integration into circuits. By adjusting the bias current, which affects the circuit's resistance, the high-impedance voltage input allows precise control over oscillation frequency across a wide range. Using the CCCII brings advantages like wider bandwidth, faster response time, better accuracy, and broader dynamic range, even at lower voltages. This design not only upgrades the Schmitt trigger but also opens up possibilities for applications in various fields where accurate signal processing is needed, like sensor technology, communication systems, and instrumentation circuits. Current sense amplifiers can handle a wider range of input voltages compared to op-amps. This makes them suitable for applications with high common-mode voltages, such as measuring currents in power supplies or motor drives [4]. The built-in amplifier in a current sense amplifier typically has a very small offset voltage. This minimizes errors in the output signal, which is crucial for precise current measurements. Current sense amplifiers are designed to maintain consistent performance over a wide range of temperatures. This ensures reliable operation in environments where temperature fluctuations can occur for amplifying high-frequency signals [5]. A high bandwidth is provided by some current amplifiers, such as current feedback amplifiers, which makes them appropriate. CCCII can be utilized as a current amplifier by controlling the input current to generate a proportional output current. This capability is particularly useful in applications where precise

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control and amplification of current signals are required, such as in sensor interfacing, current-mode signal processing, or current-controlled oscillators [6].

II. SECOND GENERATION CURRENT CONTROLLED CONVEYOR

A current conveyor is a basic structural module that possesses both negative and positive feedbacks, offers more flexibility and can then stimulate negative resistance. The Current Controlled Conveyor (CCC) is an alternate versatile CM dynamic structure that has intrinsic resistance (Rx) between input ports X and Y which can be constrained by the bias current [4-5]. The presence of intrinsic resistance, is the prime difference between CCII and CCCII that avoids the use of external resistance and hence reduces the circuit complexity and suitable for IC fabrication [5-10].

The block level illustration of CCCII is given in Fig.1

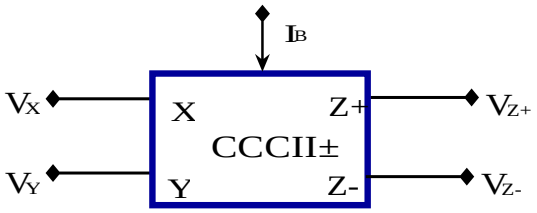

Fig.1. The structure of CCCII with input and output ports.

Dual output CCCII is basically a four terminal device, has two input ports *X*&*Y* and an output port *Z* that delivers a current at Z+ node and its replica at Z- node. CCCII has an infinite input impedance at terminals *Y* and *Z*, whereas, the input port *X* has internal resistance R_X that is tuned by the bias current I_B which is given as:

$$R_X = \frac{1}{g_{m2}+g_{m4}} \quad (1)$$

In (1) g_{mi} is the MOS transistor transconductance, assuming that both the transistors M_2 and $M_4$are matched, $g_{m2}=g_{m4}$. This leads to:

$$R_X = \frac{1}{\sqrt{8\mu Cox\left(\frac{W}{L}\right)I_B}} \quad (2)$$

In (2) μ indicates the surface mobility, oxide capacitance is C_{OX}, channel width is *W* and channel length is *L*. The internal structure of CCCII involves the MOS transistors, as presented in Fig. 2. The translinear loop consist the transistors M_1- M_4, and is DC biased with current mirrors M_6&M_7 and M_8&M_9. The input port current I_X is replicated to I_{Z+} and I_{Z-} by the translinear loops. The current is also replicated using additional current mirrors M_{10}-M_{13}, M_{14}-M_{16} and M_{17}-M_{19} [11-15].The aspect ratios of transistors of Fig. 2 are exhibited in Table I. If $I_Z = +I_X$, the module is termed as positive current conveyor and for $I_Z = -I_X$ it is called negative current conveyor [1]**.** CCC works based on the principle of controlling the output current or voltage based on the input current.

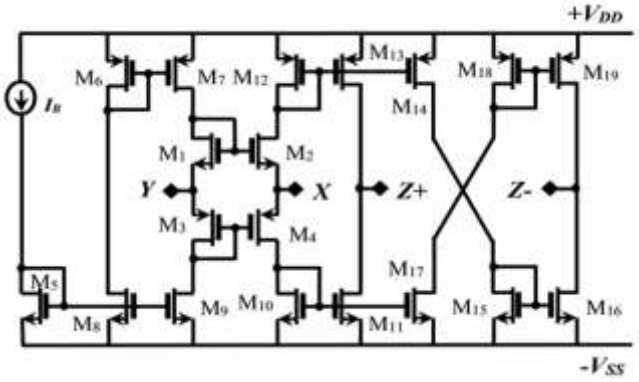

Fig. 2. CCCII structure using MOS.

In a CCCII, CMOS transistors are arranged in a looped configuration, this looped arrangement ensures that the output of one transistor affects the input of another transistor, creating a feedback loop. The CCCII working is based on the principle of translinear circuits, where the relationship between the currents and voltages across the transistors is linear. By applying input currents to the terminals of CCCII, that can control the currents and voltages within the looped arrangement. When an input is applied, it controls the flow of current through the looped arrangement of transistors. The interconnected transistors create a feedback mechanism where the output voltage depends on both the current input and the previous state of the output. This feedback loop, along with the linear relationship between currents and voltages, generates a hysteresis effect. The hysteresis effect ensures that the output voltage switches between high and low states at specific threshold level of the input current, resulting in a stable and clear square wave output.

Input stage (M_1, M_2, M_3, M_4): This stage amplifies the input current (I_B) using a differential pair (M_1, M_2) and a current mirror (M_3, M_4).

Current mirror (M_5-M_{10}): This stage copies the amplified input current to the output terminal (Z+).

Transistor	**Width (nm)**	**Length (nm)**
M_3, M_4, M_6, M_7, M_{12}, M_{13}, M_{14},M_{18}, M_{19}	120nm	45nm
M_1, M_2, M_5, M_8, M_9, M_{10}, M_{11}, M_{15}, M_{16}, M_{17}	120nm	45nm

Output stage (M_{11}-M_{19}): This stage provides a low impedance output at terminal Z+. M_{13}-M_{16} acts as a current mirror, while M_{17}-M_{19} act as a buffer. One of the features of the proposed design is, it can produce frequencies up to 1 MHz, also offers low power dissipation and low supply voltage requirement [11-16].

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TABLE I. ASPECT RATIOS OF FIGURE 2. TRANSISTORS

Section III discusses about the proposed Schmitt Trigger and its working. Section IV includes the simulation results of the proposed topology. The paper is concluded in section V.

III. PROPOSED SCHMITT TRIGGER USING CCCII

The proposed topology comprises of a single CCCII, two resistors and a grounded capacitor. To achieve a Schmitt trigger output using Cadence virtuoso simulator tool, CCCII is configured as a comparator with hysteresis. By applying a sinusoidal input signal to the CCCII, it compares the input voltage with a reference voltage set by biasing resistors. The feedback network connected from the output terminal back to the inverting input terminal provides hysteresis, ensuring that the output switches cleanly between high and low states. This hysteresis prevents the output from oscillating around the threshold voltage, resulting in a stable square wave output. Through simulation and analysis, the CCCII effectively generates the desired Schmitt trigger output, providing a reliable digital signal from the input sinusoidal waveform. A fraction β, of the output is fed back to the positive input port X,

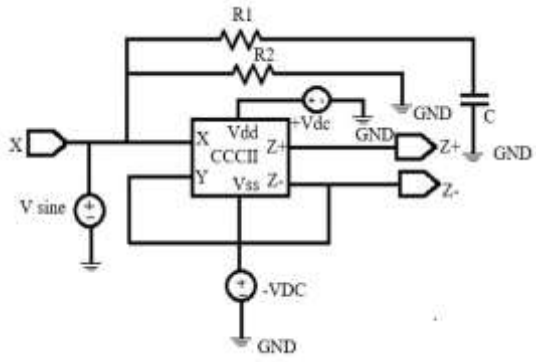

Fig. 3.Proposed Schmitt Trigger using CCCII.

The fraction β that is fed back to the input is expressed as given below,

$$\beta = \frac{(R_1 - R_2 - R_B)}{(R_1 + R_2 + R_B)} \quad (1)$$

The lower threshold and upper threshold voltages for the proposed topology are expressed as given in equations (2) and (3)

$$V_{LT} = \frac{R_2}{R_2 - (R_1 + R_B)}(-V_{sat}) \quad (2)$$

$$V_{UT} = \frac{R_2}{R_2 - (R_1 + R_B)}(+V_{sat}) \quad (3)$$

A Schmitt trigger is a comparator circuit with hysteresis. This means that it has two different threshold voltages, one for switching the output high (UT) and another for switching the output low (LT). The input voltage is applied to the input terminal (X) of the CCCII. The current coming out of terminal X is mirrored by the CCCII to its output terminal (Z). The mirrored current passes through resistor R_1, which causes a voltage drop across it. This voltage is compared to a reference voltage (V_{dc}) at the other input terminal (Y) of the CCCII.

When the input voltage is high enough to make the voltage drop across R_1 greater than the reference voltage, the output voltage (Z+) goes high. When the input voltage falls below a certain level, the voltage drop across R_1 becomes lower than the reference voltage, and the output voltage (Z+) goes low. The resistors R_1 and R_2 along with capacitor C sets the frequency of operation for the design proposed.

IV. SIMULATION RESULTS

Using Cadence virtuoso simulator tool of 45 nm GPDK technology files, the topology shown in Fig.3 is simulated. The supply voltage is fixed at +900 mV and -900 mV, the bias current I_B is set at 50µA, and the passive elements are chosen as $R_1 = 20K\Omega$, $R_2 = 1K\Omega$ and C=280nF. The simulated output waveforms are shown with respect to time period in Fig.4, where the $T_{Simulated}$=1ms. The peak-to-peak value reaches ±0.9 V when the power supply rail is ±0.9 V. The frequency of the produced waveform can be varied by tuning the bias current which indicates the maximum frequency can reach up to 1 MHz. I_B is ranged from 10 µA to 120 µA by keeping the passive component values R_1=20 kΩ, R_2=1 kΩ and C = 280 nF constant. The variation of the time period with bias current is plotted in Fig. 5. The capacitance is varied from 3 nF to 50 nF for selected values of R_1=1 kΩ, R_2=1.5 kΩ and bias current of 100 µA. Schmitt trigger circuit uses voltage levels to produce a square wave output from an analog input signal. This functionality relies on hysteresis, achieved through two threshold voltages: V_{IH} (upper threshold) and V_{IL} (lower threshold). When the input voltage (Vin) rises above V_{IH}, the output abruptly jumps to a high level (near to the supply voltage, Vcc). Conversely, when Vin falls below V_{IL}, the output switches back to a low level (around ground voltage, 0V). The hysteresis voltage (V_{HYS}), is the difference between V_{UT} and V_{LT}, creates a "dead zone" that prevents the output from switching due to minor input fluctuations or noise. This ensures a clear transition between high and low states in the resulting square wave output. While the specific voltage values depend on the circuit design and components, the output typically reaches voltages close to Vcc for the high state and near 0V for the low state, with practical limitations due to transistor saturation and

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component voltage drops. Fig 4 shows the simulation results of Schmitt trigger using single current amplifier. Fig 5 shows the Proposed Schmitt trigger produce frequencies up to 1 MHz. Fig 6 shows the AC response for the proposed topology and Fig. 7 shows the Transient response for the Schmitt trigger topology. The layout diagram of CCCII model is displayed in Fig.8. The layout of the CCCII occupies 15.39 mm chip area. Cadence layout design tools have been used for producing the CCCII layout. The delay produced by the topology is 0.69 ms and the power dissipation is 0.71 mW which are quite low and is suitable for integrated circuit fabrication.

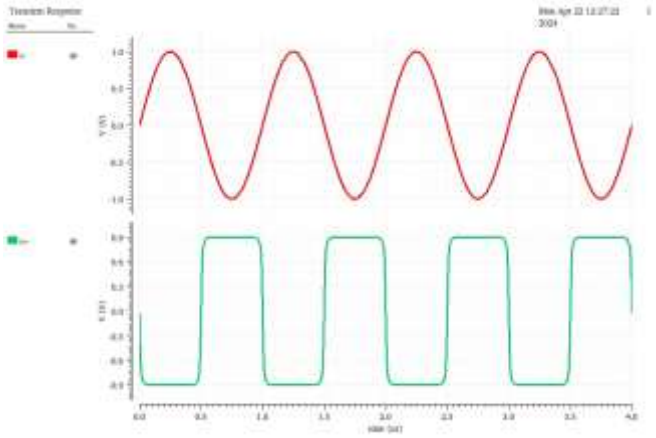

Fig.4. Simulation results of Schmitt trigger using single current amplifier

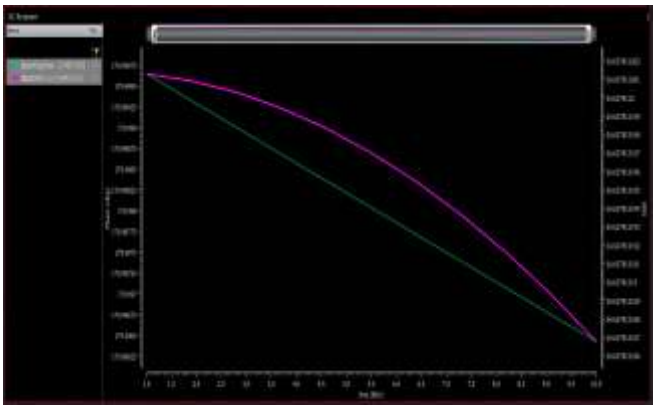

Fig. 5. AC response for the proposed topology

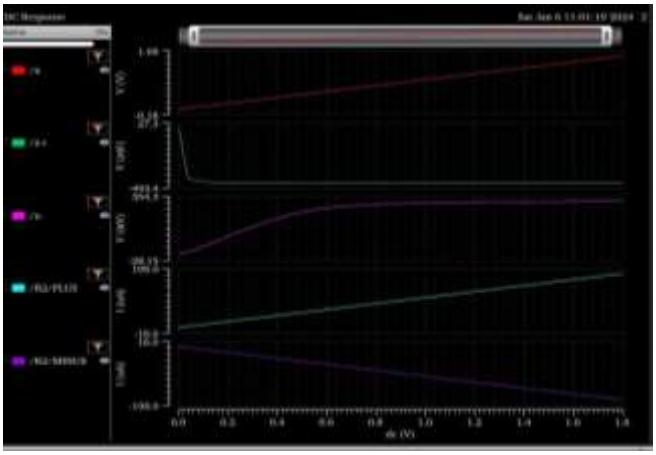

Fig. 6. DC Response for the proposed topology

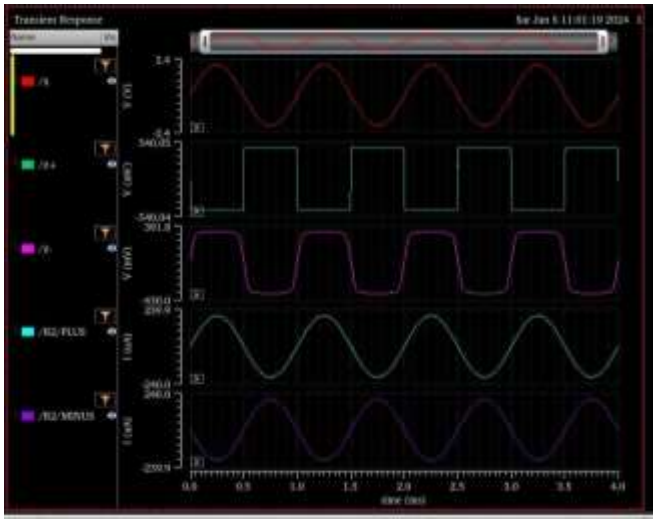

Fig.7.Transient Response of proposed topology

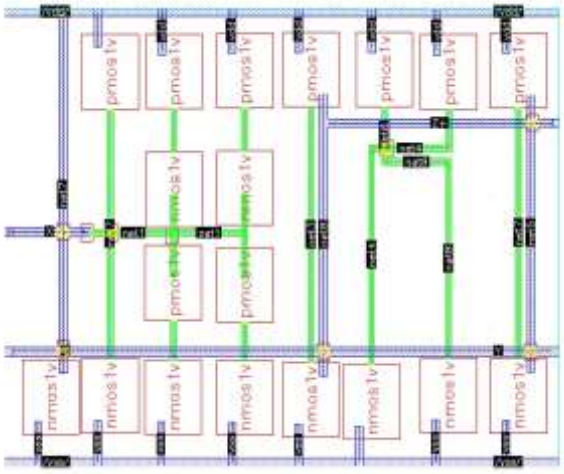

Fig.8. Layout of the CMOS based CCCII circuit

V. CONCLUSION

A CCCII centred Schmitt trigger has been proposed in this work. The design has been realized using single CCCII, two resistors and a grounded capacitor. The topology enjoys electronic tunability and produced maximum frequency of 1 MHz. The delay and power dissipation for the proposed topology are 0.69 ms and 0.71 mW respectively. Thus the proposed design is suitable for implementation in monolithic IC, usable for low power applications particularly in communication and bio medical applications as a versatile building block.

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