Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 5, May : 2024

A NOVEL ARCHITECTURE IMPLEMENTATION OF ARITHMETIC AND LOGICAL UNIT (ALU) WITH QUANTUM DOT METHOD

Pitta Deepthi M-Tech (VLSI Design) Student, Department of ECE Avanthi Institute of Engg& Tech
deepthideepunaidu20@gmail.com
E. Govinda, Professor,Department of ECE, Avanthi Institute of Engg& Tech
ennamgovinda19@gmail.com
T. Pattalu Naidu, Assistant Professor**,** Department of ECE**,** Avanthi Institute of Engg& Tech
naidu.tamarana1@gmail.com

ABSTRACT: Quantum-dot cellular automata (QCA) presents a novel approach for nano-scale digital circuit design. In this realm, an innovative 8-bit QCA-based Reconfigurable Arithmetic Logic Unit (ALU) has been introduced, employing clock zone based crossover (CZBCO) methodology. This ALU unit is engineered to execute fundamental arithmetic and logical operations, including binary addition, logical AND, OR, and EXOR. Notably, the utilization of Multi-Gate (MG) structures for the EXOR operation is optimized, with MGs repurposed for logical AND and OR operations. This strategic reuse effectively reduces the required number of MGs in a 1-bit ALU design. In comparative analysis, the proposed 1-bit ALU demonstrates a substantial decrease in energy dissipation by 54.5% and a notable reduction in QCA cell utilization by 43.5% when juxtaposed with existing methodologies. Consequently, the proposed 8-bit reconfigurable ALU streamlines design complexity by nullifying 16-MGs and achieves implementation on a single layer using CZBCO. As a result, the proposed reconfigurable ALU offers a significant reduction in cell count and power dissipation compared to prior works.

Keywords: Quantum-dot cellular automata, Arithmetic Logic Unit, Multi-Gate (MG), clock zone based crossover.

I. INTRODUCTION

Quantum-dot cellular automata (QCA) represent a promising emerging technology for crafting densely-packed, energy-efficient, and high-performing digital circuits. QCA employs an array of interconnected quantum dots to execute Boolean logic functions. Its appeal stems from the remarkable potential for compactness, simplified interconnections, and minimal power-delay product. A fundamental QCA unit comprises four quantum dots arranged in a square formation, linked by tunnel barriers. Electrons within the cell can tunnel between dots but are confined within it. When two excess electrons occupy the cell, Coulomb repulsion compels them to opposite corners, resulting in two energetically equivalent ground state polarizations, denoted as logic "0" and "1". QCA's foundational components encompass AND, OR, and NOT gates. Implementing Majority gates aids in reducing delay by managing propagation and generational carries efficiently.

Quantum dots, characterized as semiconductors confined in all three spatial dimensions, serve as simple charge containers. Alternatively, they can be described as being three-dimensionally constrained. Quantum dot cellular automata (QCA) presents a promising departure from the conventional CMOS paradigm, employing binary charge configurations, denoted as M' and O', to represent information. The theoretical framework for QCA was introduced by C. S. Lent et al. in 1993, followed by an experimental approach utilizing GaAs described in early 1999. The dynamic behavior of QCA has been explored through the Hartree approximation, with quantum mechanics playing a role in determining the cell size and dot radius of individual QCA cells.

Therefore, QCA has garnered significant research interest as a robust alternative to CMOS. Over the past few decades, amidst the nanotechnology revolution, extensive research has been conducted in this field. QCA, however, remains in its nascent stage and necessitates thorough exploration, particularly in the realm of QCA logic circuit design. Key areas of focus include low-power

reversible logic circuit design, tile-based logic circuit design, and defect analysis. Ternary computing poses a particularly challenging task within this domain, as notable advancements have yet to be observed. Multivalued computing, particularly ternary computing, emerges as a burgeoning area of research, offering potential benefits such as enhanced data storage capacity, accelerated arithmetic operations, improved support for numerical analysis, the application of non-deterministic and heuristic techniques, communication protocol development, and effective solutions for non-binary problems. Nano-scale logic circuit fabrication is susceptible to defects that can arise during the fabrication process. Notably, QCA fabrication is particularly prone to a high probability of defects, as highlighted in various studies. These defects are primarily associated with the deposition phase, where chemically synthesized QCA cells are deposited onto the substrate.

Three common defects have been identified during this phase:

a) Excessive cell deposition, where more QCA cells are deposited than required for the intended cell arrangement,
b) Missing or un-deposited cells, where QCA cells are not deposited according to the original design specifications, and
c) Displaced or misaligned cell deposition, where QCA cells are positioned incorrectly.

These defects can lead to significant errors in QCA manufacturing, potentially rendering devices or gates non-functional. Designing devices or gates using QCA necessitates establishing permissible defect tolerances for the aforementioned issues to ensure that the device retains its operational characteristics. Consequently, defect analysis emerges as a pivotal domain within QCA research. The below figure shows the QCA cell polarization in figure 1.

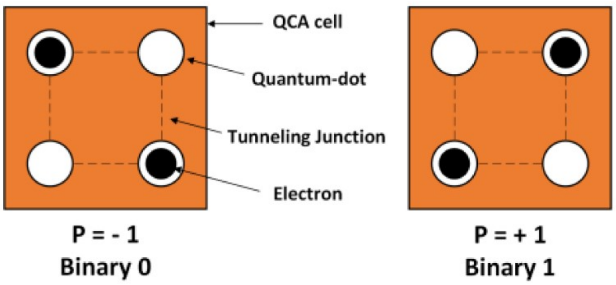

Fig 1: QCA cell polarization

II. LITERATURE WORK

Novel applications and architectures leveraging the distinctive functionality of room temperature operating Single Electron Transistor (SET) circuits have emerged, particularly through the monolithic integration of SETs with FET circuits to complement conventional Si CMOS performance. Illustrative examples encompass SET/CMOS hybrid multi-value logic circuits, multiband filtering circuits, analog pattern matching circuits, associative recognition tasks, and others, wherein characteristic Coulomb blockade oscillations of SETs are commonly exploited to minimize device count. Notably, certain aspects of circuit performance, particularly room temperature operation, already surpass the theoretical assessment of logic gate parameters for 2-nm SETs. Theoretically estimated maximum operation parameters for these devices include temperature (T~20 K), integration density (n~10^11 cm^-2), and speed on the order of 1 GHz. However, significant threshold voltage variation persists, hindering the realization of large-scale SET circuits and impeding direct competition with CMOS devices in implementing Boolean logic operations. Overcoming size and background charge fluctuations is imperative to mitigate threshold voltage variations.Single-electron approaches, which represent a bit by a Single-electron ("bit state logic") and utilize a single electron for random number generation, have been primarily confined to

laboratory demonstrations. The limited fanout issue inherent in truly Single-electron devices, stemming from the use of only a single electron, may be addressed through innovative circuit designs like the binary decision-diagram. Consequently, the drawbacks of CMOS have spurred significant endeavors to identify suitable alternatives, with nano-scale technologies such as Tunneling Phase Logic (TPL), Single Electron Tunneling (SET), and Quantum-dot Cellular Automata (QCA) garnering considerable attention. Recent research has proposed possible implementations of Quantum-dot cells for Quantum-dot Cellular Automata (QCA), as demonstrated. An adiabatic switching paradigm has been developed for clock-controlled pipelined QCA architectures, where binary information is stored as electronic charge, resulting in reduced computing requirements. Furthermore, researchers have expanded the theoretical analysis of QCA arrays. Tonamoto et al. have suggested alternative methods of assembling QCA cells into practical devices. Lusth and Jackson have employed graph theoretic analysis in QCA design, while Chen and Porodhave devised sophisticated finite element models for gate-depleted Quantum-dots in semiconductors, which can correlate Dot occupancy with specific bias conditions.

In [6], authors have introduced a straightforward clocked molecular QCA cell. These molecules exhibit intrinsic bistability due to dipole charge configuration, which strongly interacts with neighboring molecules. Although this study is preliminary and indicative of the potential use of molecular QCA, it underscores the exploration of molecular-scale QCA implementation. A review of the feasibility of implementing QCA on a molecular scale or using nano-magnets has been conducted [64]. Numerous molecular structures for QCA have been proposed, with one such 2-Dot QCA already implemented. It is anticipated that the full potential of QCA will emerge from the integration of existing technologies with advanced nanotechnology.An experimental realization of Quantum-dot Cellular Automata (QCA) within Nano-scale Metal-dot structures defined by tunnel barriers has been documented in [6]. In this work, the authors showcase controlled polarization of QCA cell switching, consistent with theoretical predictions. The operation of clocked QCA is demonstrated through a two-cell shift register example. Another study [7] introduces fan-outs.

Research concerning the switching speed and temperature dependency of QCA has been outlined in [7]. Traditional Coulomb blockade and master equation dynamic approaches have been considered for the design of a semi-infinite shift register. The pivotal role of power gain as a function of temperature has been elucidated. However, the behavior of such circuits with respect to clock speed and temperature remains incompletely explained [5]. It has been observed that circuit speed is constrained by the RC-time constant, allowing Majority Voters to operate up to 450 Kelvin, while QCA wires can function up to room temperatures.

QCA's physical design challenges have been addressed within the context of VLSI physical design issues in [4]. A comparison between ILP formulation and heuristic solutions for QCA partitioning, placement, and routing has been presented, revealing that the heuristic approach yields the most optimized results. The issues of unidirectionality and metastability within QCA wires have been investigated, prompting the proposal of a 3D architecture as an alternative to asymmetric spacing.The classical analysis conducted herein has indicated that a 3D configuration could serve as a solution to overcome metastability issues. While H-memory is a design specifically tailored for QCA, authors in [7] propose a novel execution model that integrates with H-memory to distribute CPU functionality throughout memory structures.

Present-day QCA designs typically consist of four-dot cells. However, reports in existing methods hasalso documented designs featuring five-dot and even six-dot configurations. Current research endeavors are primarily focused on developing low-power devices. Compared to counterpart designs, the proposed Full-Adder cell exhibits the lowest energy dissipation. From the perspectives of complexity, latency, and area, the proposed adder structures outperform all counterparts with significant superiority.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 5, May : 2024

Given the utilization of both gate-level and a new explicit interaction approach in designing QCA combinational circuits in this study, we anticipate that the findings presented herein will be of significant interest for future computational endeavors.

III. PROPOSED METHODOLOGY

The operations of the Arithmetic Logic Unit (ALU) are typically categorized into two main groups: Arithmetic operations and Logical operations. Arithmetic tasks such as Addition, Subtraction, Increment, Decrement, and others are carried out by the Arithmetic unit, while the Logical unit handles operations like AND, OR, XOR, complement, rotate, shift, and so forth. Multiplexers and de-multiplexers play critical roles in selecting the appropriate results produced by the ALU.Microcontrollers must manage individual port lines, necessitating bit handling instructions. Consequently, an ALU within a Microcontroller must accommodate both bitwise and byte-wise Logical operations, arithmetic computations, and data transfers. Despite encompassing all ALU functionalities, the primary challenge remains in optimizing the chip's area utilization.

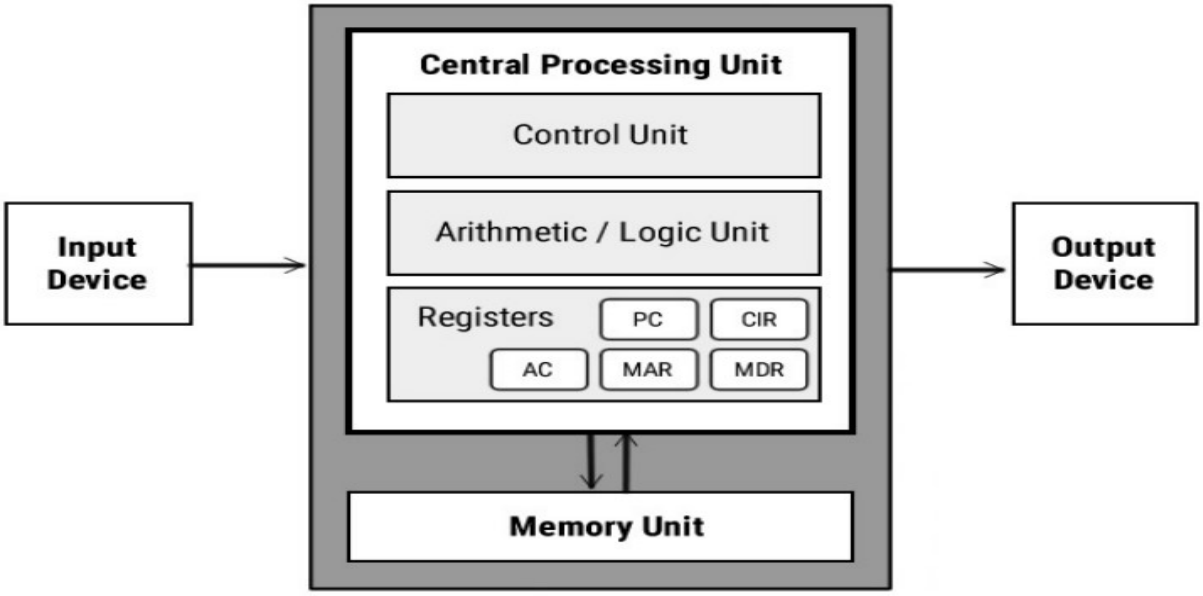

Fig.2: A typical depiction of proposed ALU architecture

The fundamental component in designing an arithmetic unit is the full adder circuit. Various types of adders, such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), and Carry Select Adder (CSeA), are designed in multiple ways. The selection of a specific adder depends on the parameter to be minimized. For instance, if minimizing delay is the priority, then CSeA is preferable, although it comes with a larger chip area and higher power consumption. On the other hand, CLA, while slower than CSeA, occupies significantly less area. CSA becomes the preferred choice when the number of bits to be added increases, particularly in the case of multipliers. RCA occupies the smallest area but becomes slower as the number of bits to be added increases.

The suggested structure prioritizes area optimization, thus opting for RCA throughout the design. The ALU is intended for integration into a Microcontroller alongside a barrel shifter to expedite logical operations. Given the targeted clock frequency of 20MHz for the microcontroller, operational speed wasn't a primary concern. The entire instruction set for the ALU has been meticulously crafted.The main limitation observed in the cited literature is the significant area consumption, leading to higher power usage. They utilized multiple majority gates, including two 3-input and two 5-input majority gates, along with four inverter gates, to construct full adders and subtractors. To

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 5, May : 2024

address this, a novel design has been developed capable of performing both full addition and subtraction simultaneously.

A Quantum-dot Cellular Automata (QCA) is a nanostructure consisting of square cells, each containing four quantum dots charged with two free electrons capable of tunneling through the dots. Due to Coulombic repulsion, these electrons tend to occupy opposite corners, representing binary states 1 and 0 based on their positions within the cell.

Although neighboring cells interact via electrostatic forces and tend to align their polarizations, QCA cells lack inherent data flow directionality. To establish controlled data flow directions, cells within a QCA design are divided into clock zones, each associated with a clock signal phase-shifted by 90°. This clocking scheme, known as the zone clocking scheme, inherently pipelines QCA designs, with each clock zone functioning akin to a D-latch..

QCA cells serve both as logic elements and interconnections, utilizing either the coplanar cross or bridge technique. In QCA technology, the fundamental logic gates are the inverter and the Majority Gate (MG). The MG, with three inputs (a, b, and c), performs the logic function described in equation (1) when all input cells share the same clock signal clkx (where x varies from 0 to 3), while the remaining cells of the MG are linked to the clock signal clkx+1:

$$M(abc) = a \cdot b + a \cdot c + b \cdot c.$$

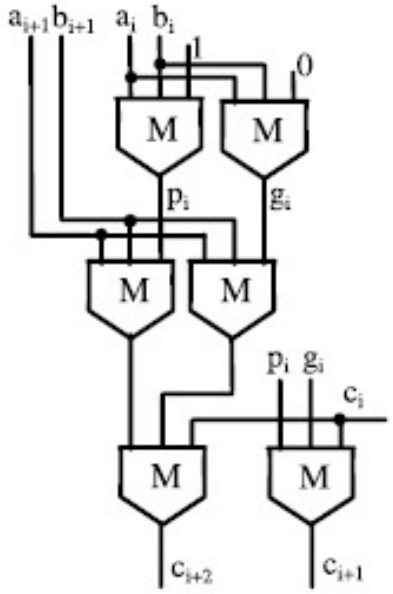

Fig. 3: Novel 2-bit basic module.

Various QCA adder designs are documented. The Ripple Carry Adder (RCA) and the Carry-lookahead Adder (CFA) process n-bit operands by chaining n full-adders (FAs). Despite using different FA topologies, both addition circuits feature a carry-in to carry-out path comprising one MG, and a carry-in to sum bit path consisting of two MGs plus one inverter. Consequently, the worst-case computational paths for n-bit RCA and n-bit CFA involve (n+2) MGs and one inverter.A CLA architecture formed by 4-bit slices was also presented. In particular, the auxiliary propagate and generate signals, namely $pi = ai + bi$ and $gi = ai \cdot bi$, are computed for each bit of the operands and then they are grouped four by four. Such a designed *n*-bit CLA has a computational path composed of $7 + 4 \times (\log 4\ n)$ cascaded MGs and one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which only one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path. In addition, to compute the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that, to process *n*-bit addends, log4 *n* levels of CLA

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 5, May : 2024

logic are required, each contributing to the computational path with four cascaded MGs. Finally, the computation of sum bits introduces two further cascaded MGs and one inverter.

The parallel-prefix Binary Kogge-Stone Adder (BKA) showcased in this study leverages more efficient basic Carry Lookahead Adder (CLA) logic structures. Its primary advantage over previously discussed adders lies in its ability to achieve a lower computational delay. When processing n-bit operands, the BKA's worst-case computational path comprises $4 \times log2\, n - 3$ cascaded Majority Gates (MGs) and one inverter. Apart from the level necessary for computing propagate and generate signals, the prefix tree consists of $2 \times log2n - 2$ stages. Analyzing the logic equations provided reveals that the first stage of the tree introduces just one MG into the computational path, while the last stage contributes only one MG. In contrast, the intermediate stages introduce two cascaded MGs each into the critical path. Finally, for computing the sum bits, an additional two cascaded MGs and one inverter are incorporated.

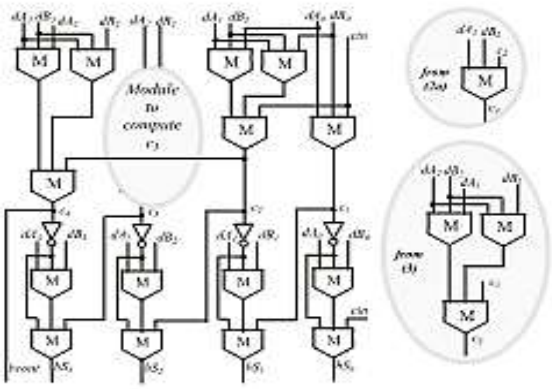

Fig 4: New ADD1 module

With the primary aim of balancing area and delay considerations, the hybrid adder (HYBA) introduced in this context combines a parallel-prefix adder with the Ripple Carry Adder (RCA). For n-bit operands, this architecture exhibits a worst-case computational path comprising 2×log2 n +2 cascaded Majority Gates (MGs) and one inverter.Utilizing the methodology recently proposed, the worst-case path of the Carry Lookahead Adder (CLA) is reduced to 4 × log4 n + 2 × log4 n − 1 MGs and one inverter. This approach can also be employed to design the Binary Kogge-Stone Adder (BKA), leading to reduced overall area while maintaining the same computational path.By applying the decomposition method illustrated, the computational paths of the CLA and the Carry Skip Adder (CFA) are reduced to 7 + 2×log2(n/8) MGs and one inverter and to (n/2) + 3 MGs and one inverter, respectively.

IV. RESULTS & DISCUSSION

The proposed methodology is implemented using Xilinx VivadoSoftware tool. Xilinx Vivado is a suite of software tools developed by Xilinx, an American technology company specializing in the development of programmable logic devices (PLDs), particularly field-programmable gate arrays (FPGAs) and adaptive compute acceleration platforms (ACAPs). Vivado is primarily used for designing, verifying, synthesizing, and implementing digital circuits on Xilinx FPGAs and ACAPsThe simulation results are shown in the following figures. The proposed reconfigurable Arithmetic & Logical Unit (ALU) is implemented with Quantum Dot Automata and the corresponding simulation results are shown in the below figures with different combinations of control signals CS[2:0]. Figure 5 shows these results with all the 8 possibilities of control signals i.e., from “000” to “111”. The performance of the proposed ALU gives an excellent results.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 5, May : 2024

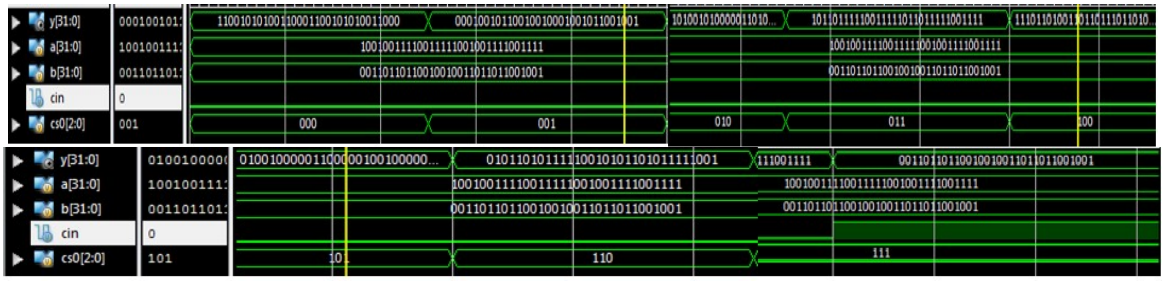

Fig 5: Simulation result of proposed ALU.

V. CONCLUSION

This study introduces novel designs for N-bit adders, subtractors, and multipliers based on Quantum-dot Cellular Automata (QCA) to facilitate arithmetic and logical operations. Simulation results validate that the proposed operations require fewer cells, occupy less area, and exhibit lower latency. Furthermore, to streamline the complexity associated with addition-related operations, an efficient adder-subtractor hybrid has been proposed.

REFERENCES

[1]. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," *Nanotechnology*, vol. 4, no. 1, pp. 49–57, 1993.

[2]. M. T. Niemer and P. M. Kogge, "Problems in designing with QCAs Layout = Timing," *Int. J. Circuit Theory Appl.*, vol. 29, no. 1,pp. 49–62, 2001.

[3]. J. Huang and F. Lombardi, *Design and Test of Digital Circuits by Quantum-Dot Cellular Automata*. Norwood, MA, USA: Artech House,2007.

[4]. W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, Jr., "Design rules for quantum-dot cellular automata," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2011, pp. 2361–2364.

[5]. K. Kim, K. Wu, and R. Karri, "Toward designing robust QCA architectures in the presence of sneak noise paths," in *Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit.*, Mar. 2005, pp. 1214–1219.

[6]. K. Kong, Y. Shang, and R. Lu, "An optimized majority logic synthesis methology for quantum-dot cellular automata," *IEEE Trans. Nanotechnology.*vol. 9, no. 2, pp. 170–183, Mar. 2010.

[7]. K. Walus, G. A. Jullien, and V. S. Dimitrov, "Computer arithmetic structures for quantum cellular automata," in *Proc. AsilomarConf.Sygnals, Syst. Comput.*, Nov. 2003, pp. 1435–1439.

[8]. M. BagherianKhosroshahy, M. H. Moaiyeri, S. Angizi, N. Bagherzadeh and K. Navi, "Quantum-Dot Cellular Automata Circuits with Reduced External Fixed Inputs", Microprocessors and Microsystems, Vol. 50, pp. 154-163, 2017 (ISI).

[9]. BikashDebnath, Jadav Chandra Das, Debashis De, "Reversible logic-based image steganography using quantum dot cellular automata for secure nanocommunication", IET Circuits, Devices & Systems pp. 58–67, Vol. 11, Iss. 1, year 2017.

[10]. K.Walus, T.J Dysart and G.A Jullien, "QCADesigner: A Rapid design and simulation tool for Quantum-dot cellular automata", IEEE Transaction on Nanotechnology vol.3, pp: 26-31, 30th march 2004.

[11]. S. Srivastava, A. Asthana, S. Bhanja, and S. Sarkar, "QCAPro an error-power estimation tool for QCA circuit design, Circuits and Systems (ISCAS)", IEEE International Symposium, pp: 2377- 2380, 2011.

[12]. Saket Srivastava, Sudeep Sarkar and SanjuktaBhanja,"Estimation of Upper Bound of Power Dissipation in QCA Circuits", IEEE Transactions On Nanotechnology, Vol. 8, No. 1, pp:116-127, Jan 2009.