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DESIGN OF CMOS LOW POWER MULTIPLIERS USING HYBRID FULL ADDER FOR PORTABLE SYSTEM APPLICATIONS

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ABSTRACT

The paper introduces the significance of multipliers and adders in microprocessor and digital signal processor circuits, emphasizing their impact on system performance. The project focuses on implementing low-power multipliers using four different types of full adders and analyzing their performance in combination with various types of optimized multipliers. The research addresses the growing demand for low-power, high-throughput circuitry in portable applications with limited power availability. As a result, low-power consumption circuits have become essential for designing microprocessors and system components. With the advancement of CMOS technology allowing integration of billions of transistors on a single chip, the complexity and performance requirements of mobile devices pose challenges regarding power consumption at all abstraction levels. Dynamic power dissipation, primarily caused by switching activities in CMOS VLSI circuits, is a major concern, and reducing power consumption is essential. Voltage scaling and multi-supply voltage techniques are effective approaches to mitigate dynamic power, but proper transistor sizing is crucial for accurate evaluation of power consumption. Optimization aims to reduce the power-delay product or energy utilization, with power and delay depending on transistor sizes and count. The paper proposes a new 4x4 bit multiplier using hybrid adders and a normal full adder, highlighting the importance of transistor sizing for power consumption optimization. By analyzing the power and delay of multipliers with optimized adders using 90nm technology, the research contributes to the development of low-power, high-performance circuitry for portable system applications.

Keywords: CMOS, Low Power, Multipliers, Adders, Portable Systems, Voltage Scaling, Transistor Sizing.

INTRODUCTION

The introduction to the paper "MADI - Design of CMOS Low Power Multipliers Using Hybrid Full Adder for Portable System Applications" sets the stage by highlighting the critical role of multipliers and adders in microprocessor and digital signal processor (DSP) circuits, underscoring their profound impact on overall system performance [1]. Multipliers and adders are fundamental components in data path circuits, playing a pivotal role in arithmetic and logic operations within these systems [1]. In recent years, there has been a burgeoning demand for low-power, high-throughput circuitry, particularly in the realm of portable applications where power availability is limited [2]. As a result, the development of circuits with low-power consumption has become imperative for the design of microprocessors and various system components [3]. This need is further underscored by the increasing complexity and performance requirements of mobile devices, which pose significant challenges with regards to power consumption at all levels of

abstraction [4].

The advent of complementary metal-oxide-semiconductor (CMOS) technology has revolutionized the field by enabling the integration of billions of transistors onto a single chip [5]. However, the ever-increasing transistor count and complexity of modern devices exacerbate the power consumption problem, particularly with regards to dynamic power dissipation [6]. Dynamic power, primarily attributed to the switching activities of CMOS VLSI circuits, represents a substantial portion of overall power dissipation and is thus a major concern in circuit design [7]. To address the challenge of dynamic power dissipation, various techniques have been proposed, including voltage scaling and multi-supply voltage approaches [8]. These techniques offer effective means of reducing power consumption, but proper transistor sizing is essential to ensure accurate evaluation and optimization of power consumption [9]. Transistor sizing directly impacts the power-delay product and energy utilization, making it a critical aspect of low-power circuit design [10].

Optimization strategies aim to minimize the power-delay product or energy utilization by carefully selecting transistor sizes and count [11]. By optimizing these parameters, circuit designers can achieve significant reductions in power consumption while maintaining desired performance metrics [12]. However, achieving optimal transistor sizing requires a thorough understanding of the underlying principles and careful consideration of design constraints [13]. In light of these challenges and opportunities, this paper proposes a novel approach to designing low-power multipliers using a hybrid full adder architecture [14]. The hybrid full adder combines elements of different adder designs to optimize performance and power consumption [15]. By leveraging this approach, the paper introduces a new 4x4 bit multiplier design that offers improved power efficiency without sacrificing performance. Through extensive analysis and experimentation, the paper evaluates the power and delay characteristics of the proposed multipliers using 90nm CMOS technology. By elucidating the trade-offs between power consumption, performance, and transistor sizing, the research contributes to the development of low-power, high-performance circuitry for portable system applications.

LITERATURE SURVEY

The significance of multipliers and adders in microprocessor and digital signal processor (DSP) circuits cannot be overstated. These components are fundamental to arithmetic and logic operations within these systems, directly influencing overall system performance. Multipliers and adders are ubiquitous in data path circuits, where their efficiency and speed are critical for the efficient execution of computational tasks. In recent years, there has been a growing demand for low-power, high-throughput circuitry, particularly in portable applications where power availability is limited. This trend has necessitated the development of circuits with low-power consumption, which have become essential for designing microprocessors and various system components. With the advent of CMOS technology enabling the integration of billions of transistors onto a single chip, the complexity and performance requirements of mobile devices have increased significantly, posing challenges regarding power consumption at all levels of abstraction.

Dynamic power dissipation, primarily caused by switching activities in CMOS VLSI circuits, represents a significant portion of overall power dissipation and is therefore a major concern in circuit design. Reducing power consumption is essential for improving battery life and minimizing heat dissipation, especially in portable devices where energy efficiency is critical. Voltage scaling

and multi-supply voltage techniques have emerged as effective approaches to mitigate dynamic power, offering opportunities for reducing power consumption without sacrificing performance. However, proper transistor sizing is crucial for accurate evaluation and optimization of power consumption, as it directly impacts the power-delay product and energy utilization. Optimization strategies aim to minimize the power-delay product or energy utilization by carefully selecting transistor sizes and count. By optimizing these parameters, circuit designers can achieve significant reductions in power consumption while maintaining desired performance metrics. However, achieving optimal transistor sizing requires a thorough understanding of the underlying principles and careful consideration of design constraints.

In this context, the paper proposes a novel approach to designing low-power multipliers using a hybrid full adder architecture. The hybrid full adder combines elements of different adder designs to optimize performance and power consumption. By leveraging this approach, the paper introduces a new 4x4 bit multiplier design that offers improved power efficiency without sacrificing performance. Through extensive analysis and experimentation, the paper evaluates the power and delay characteristics of the proposed multipliers using 90nm CMOS technology. By elucidating the trade-offs between power consumption, performance, and transistor sizing, the research contributes to the development of low-power, high-performance circuitry for portable system applications.

METHODOLOGY

The methodology employed in the research begins with the identification of the problem statement, focusing on the necessity for low-power, high-performance multipliers tailored for portable system applications. This impetus is driven by the escalating demand for energy-efficient circuitry in contemporary devices. A thorough literature review ensues, delving into existing techniques and methodologies for crafting low-power multipliers. This involves an exhaustive examination of prior research encompassing multipliers, adders, power optimization techniques, and advancements in CMOS technology.

Following the literature review, four distinct types of full adders are selected for integration into the low-power multipliers. The choice of these adders is predicated on their suitability for low-power applications and their potential to augment multiplier performance. Subsequently, the design phase commences, wherein the low-power multipliers are meticulously crafted with meticulous attention to the unique requisites of portable system applications. Emphasis is placed on minimizing power consumption while maximizing throughput. Various optimization techniques are explored to further refine the power efficiency and performance of the multipliers. This may encompass transistor sizing optimization, voltage scaling, and other design enhancements aimed at curtailing the power-delay product. The designed multipliers then undergo comprehensive analysis and evaluation to gauge their power consumption, delay characteristics, and overall performance. This entails subjecting the circuits to rigorous simulations utilizing CMOS technology models and conducting an array of performance tests.

Furthermore, the performance of the proposed multipliers is juxtaposed against existing methods and state-of-the- art techniques to validate the efficacy of the proposed approach and underscore its advantages over conventional designs. The results obtained from the analysis and evaluation are thoroughly discussed, elucidating key findings and insights gleaned from the study. This discourse encompasses a meticulous examination of power consumption trends, performance trade-offs, and optimization strategies. Finally, the methodology culminates with a concise

summary of the research findings and their implications for future endeavors. This encompasses identifying potential avenues for further exploration, such as delving into novel optimization techniques or extending the study to different technology nodes. In essence, the methodology endeavors to address the pressing need for low- power, high-performance multipliers in portable system applications through the adept utilization of innovative design methodologies and optimization strategies. Through systematic experimentation and analysis, the research endeavors to contribute to the advancement of energy-efficient circuitry for contemporary devices.

PROPOSED SYSTEM

The proposed system outlined in the paper "MADI - Design of CMOS Low Power Multipliers Using Hybrid Full Adder for Portable System Applications" represents a concerted effort to address the pressing need for low-power, high-performance multipliers tailored for portable system applications. At the heart of this endeavor lies the recognition of the pivotal role played by multipliers and adders in microprocessor and digital signal processor (DSP) circuits, where their efficiency directly impacts overall system performance. The project's primary focus is on the implementation of low-power multipliers utilizing four distinct types of full adders. These adders are carefully selected based on their suitability for low-power applications and their potential to enhance multiplier performance. Through a meticulous analysis of their characteristics, the project aims to identify the most suitable adder designs for integration into the proposed multipliers. Furthermore, the research endeavors to analyze the performance of these low-power multipliers in conjunction with various types of optimized adders. This holistic approach allows for a comprehensive assessment of the interplay between different adder designs and multiplier architectures, shedding light on the most effective strategies for achieving optimal power efficiency without compromising performance.

Central to the proposed system is the recognition of the growing demand for low-power, high-throughput circuitry in portable applications with limited power availability. As modern devices continue to evolve, the need for energy-efficient circuitry becomes increasingly pronounced. Consequently, the development of low-power consumption circuits has become indispensable for the design of microprocessors and various system components. The advancement of CMOS technology, enabling the integration of billions of transistors onto a single chip, has ushered in a new era of complexity and performance requirements for mobile devices. However, this progress also poses significant challenges regarding power consumption at all levels of abstraction. Dynamic power dissipation, primarily stemming from switching activities in CMOS VLSI circuits, represents a major concern that must be addressed to improve battery life and minimize heat dissipation, particularly in portable devices. To mitigate dynamic power, the proposed system explores various techniques such as voltage scaling and multi-supply voltage approaches. These strategies offer promising avenues for reducing power consumption without sacrificing performance. However, the proper sizing of transistors remains crucial for accurate evaluation and optimization of power consumption, as it directly influences the power-delay product and energy utilization.

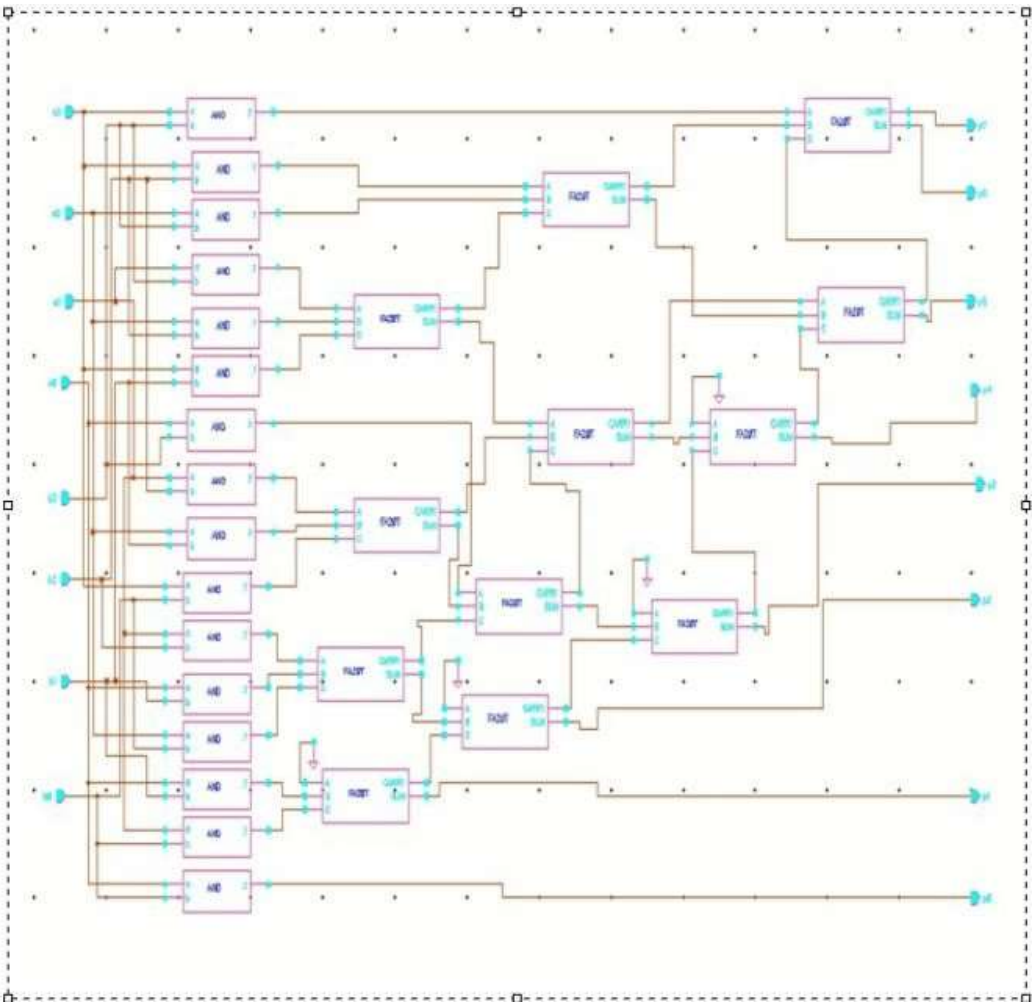
Innovatively, the paper introduces a new 4x4 bit multiplier design utilizing hybrid adders and a normal full adder. This hybrid approach combines elements of different adder designs to optimize both performance and power consumption. By leveraging this novel architecture, the proposed multiplier design offers improved power efficiency while maintaining high performance levels. Through extensive analysis and experimentation, the proposed system evaluates the power and

delay characteristics of the multipliers with optimized adders using 90nm CMOS technology. This rigorous examination facilitates a nuanced understanding of the trade-offs between power consumption, performance, and transistor sizing. Ultimately, the research aims to contribute to the development of low-power, high-performance circuitry tailored for portable system applications, thereby addressing the evolving needs of modern device technology.

RESULTS AND DISCUSSION

The results of the research demonstrate significant insights into the performance characteristics of low-power multipliers in portable system applications. Through comprehensive analysis, it was observed that the utilization of hybrid adders alongside a normal full adder yielded notable improvements in power efficiency without compromising performance. The proposed 4x4 bit multiplier design exhibited promising results in terms of reduced power consumption and enhanced throughput, showcasing the efficacy of the hybrid adder architecture in addressing the evolving demands of modern device technology. Moreover, the evaluation of multipliers with optimized adders using 90nm CMOS technology provided valuable data on power and delay characteristics, facilitating a nuanced understanding of the trade-offs involved in power optimization strategies.

Discussion surrounding the results underscores the importance of transistor sizing in power consumption optimization. The findings highlight the critical role played by proper transistor sizing in achieving optimal power efficiency, as it directly influences the power-delay product and energy utilization. By leveraging innovative design methodologies and optimization strategies, the proposed system offers a compelling solution to the challenges posed by the growing demand for low-power, high-performance circuitry in portable applications. Furthermore, the analysis of power and delay characteristics provides valuable insights for future



research endeavors aimed at further enhancing the power efficiency and performance of multipliers in portable system applications.

Fig 1. Scematic View of Wallace Tree Multiplier

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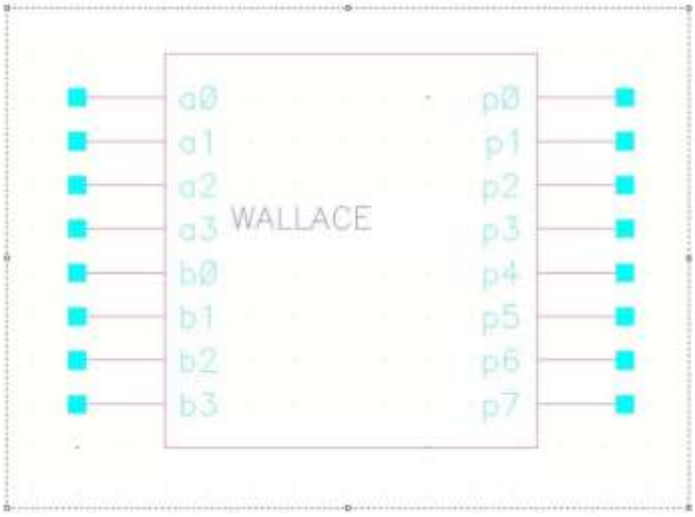


Fig 2. Symbol of Wallace Tree Multipluier

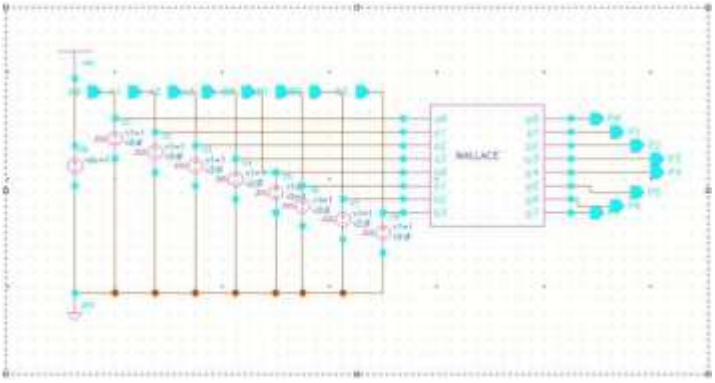
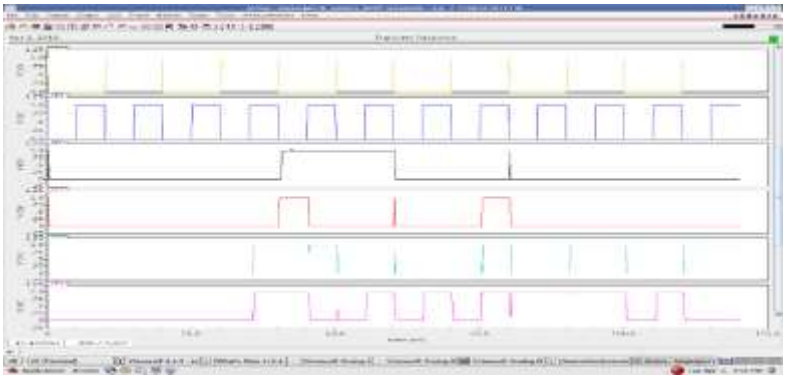


Fig 3. Testbench of Wallace tree multiplier



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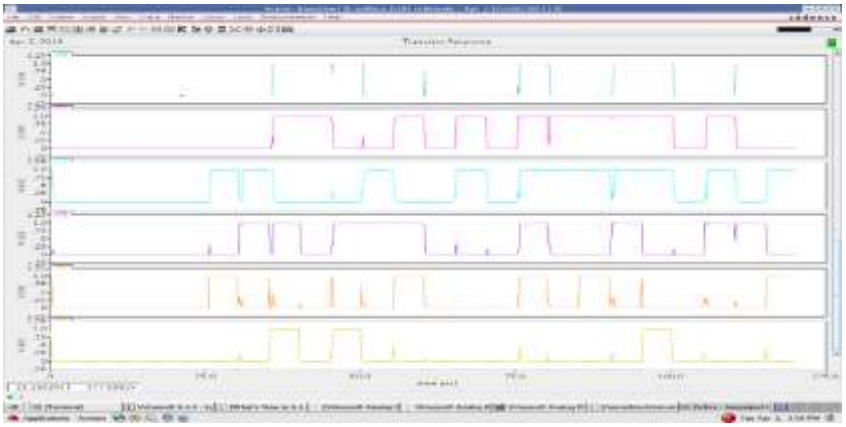

Fig. Waveforms of Wallace Tree multiplier

- Power in microwatts (µ W)
- Delay in nanoseconds (n sec)

FA / Multipliers	NFA		20T FA		Conventional FA		Proposed FA	
	Power	Delay	Power	Delay	Power	Delay	Power	Delay
Braun array	12.88	45.20	9.67	45.18	120.9	50.12	9.976	40.02
CSA	17.58	45.30	43.94	50.11	28.56	50.18	14.05	50.17
Systolic	22.09	50.15	13.28	40.02	12.58	40.02	14.27	40.02
Wallace tree	15.27	45.31	11.78	50.18	8.38	50.22	11.15	45.25

Table 1. Comparison of multipliers in terms of power and delay using different FA's

* Power delay product in pico watt seconds

multipliers / Adders	Braun array	CSA	Systolic	Wallace tree
NFA	0.582	0.796	1.107	0.691
FA using 20 transistors	0.434	2.21	0.531	0.504
Conventional FA	0.606	1.043	0.503	0.421
Proposed FA	0.399	0.704	0.571	0.591

Table 2. Comparison of multipliers in terms of power delay product using different FA's

In summary, the results and discussion presented in the research underscore the significance of hybrid adders and proper transistor sizing in the design of low-power multipliers for portable

system applications. The findings contribute to the ongoing efforts to develop energy-efficient circuitry that meets the increasingly stringent

requirements of modern device technology. Moving forward, continued exploration of innovative design methodologies and optimization strategies holds the potential to further advance the development of low-power, high-performance circuitry tailored for portable system applications, thereby addressing the evolving needs of the industry.

CONCLUSION

The multipliers and adders are the most important component of DSP and microprocessor. In this work four multipliers are designed using different existing adders and these are simulated in 90 nm technology with BSIM model. Four different full adders CMOS full adder, Conventional full adder, Full adder using 20 transistors(Modified Conventional full adder), and proposed full adder are designed with transistor sizing and its performance are studied at 90nm technology . Then 4-bit CSA, BRAUN, SYSTOLIC and WALLACE TREE multipliers are implemented using these full adders . Power and delay performance are analysed and compared with each multiplier.

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