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FPGA IMPLEMENTATION OF PARALLEL AND ADAPTABLE 5G LDPC DECODER

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ABSTRACT

In this project, we implement for the fifth generation (5G) cellular network technology, a crucial error correcting code is the quasi-cyclic (QC) low-density parity-check (LDPC) code. The 5G LDPC coding structure is intended to accommodate several frame sizes and code speeds enables great parallelism to achieve 10 Gb/s, a highly demanding data rate. The hardware design is put under difficult constraints by this remarkable performance. Processing rate penalties may be introduced on some configurations if such high flexibility is allowed. Field programmable gate array (FPGA) devices are the focus of a unique, highly parallel, and flexible hardware design for the 5G LDPC decoder that is suggested in this context. To maximize the utilization of the processing units and greatly increase the processing rate, the architecture offers frame parallelism. The controller unit was meticulously engineered to prevent update conflicts and support all 5G configurations. Additionally, a productive data scheduling strategy is suggested to boost the processing rate. For many setups, the suggested FPGA prototype outperforms the latest related state of the art in terms of processing rate per hardware resource.

Keywords: Field programmable gate array (FPGA), fifth generation (5G), low- density parity check(LDPC), Parallelism throughput.

INTRODUCTION

The fifth generation (5G) of cellular network technology brings with it unprecedented demands for high-speed data transmission and reliable communication. As part of the essential infrastructure for 5G networks, error correcting codes play a crucial role in ensuring data integrity and minimizing transmission errors [1]. Among these codes, the quasi-cyclic (QC) low-density parity-check (LDPC) code stands out as a key component in 5G LDPC coding structures, offering the flexibility to accommodate various frame sizes and code speeds [2]. This adaptability enables the LDPC code to achieve data rates as high as 10 Gb/s, meeting the stringent requirements of 5G communication systems [3]. However, the exceptional performance requirements of 5G LDPC decoding present significant challenges for hardware implementation. The need for high flexibility to support multiple configurations imposes strict constraints on hardware design, potentially leading to processing rate penalties [4]. To address these challenges, a unique approach focusing on Field Programmable Gate Array (FPGA) devices is proposed for the implementation of the 5G LDPC decoder. FPGAs offer a combination of parallelism and flexibility ideally suited for handling the complex processing tasks involved in LDPC decoding for 5G networks [5].

The proposed FPGA-based architecture leverages parallelism to maximize the utilization of processing units and achieve high processing rates [6]. By employing frame parallelism, multiple frames can be

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processed simultaneously, enhancing overall throughput and meeting the demanding data rate requirements of 5G communication systems [7]. Furthermore, meticulous engineering of the controller unit ensures efficient management of processing resources, minimizing update conflicts and optimizing performance across all 5G LDPC configurations [8].

In addition to parallel processing, a productive data scheduling strategy is proposed to further enhance processing rates [9]. By efficiently scheduling data flow within the FPGA architecture, latency is reduced, and throughput is maximized, enabling the system to handle the rigorous demands of 5G LDPC decoding with exceptional efficiency [10].

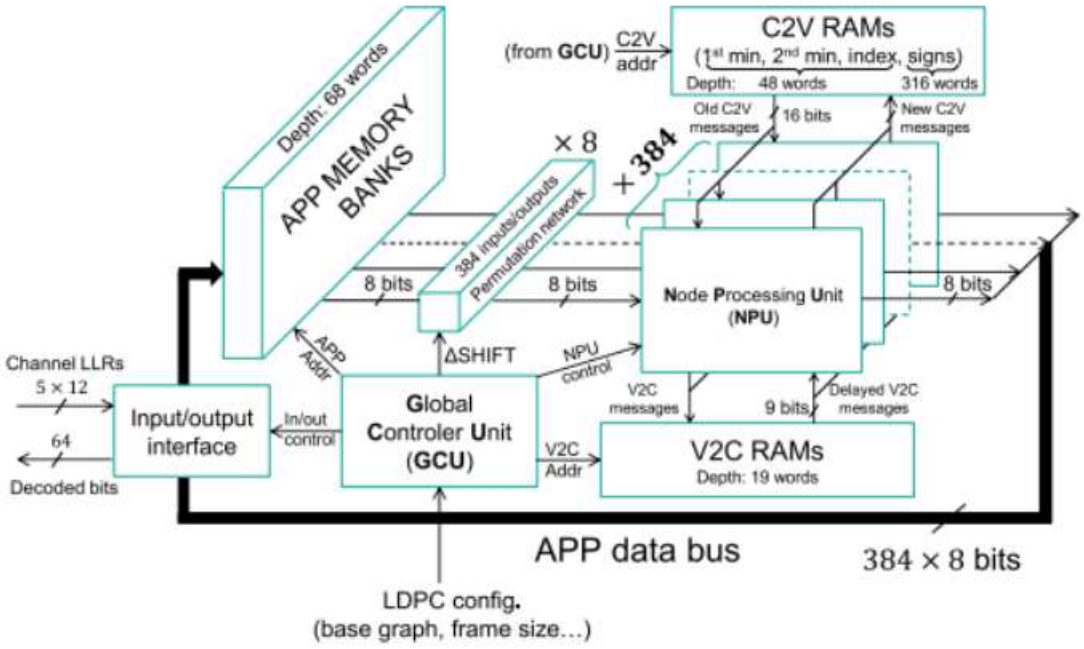

Fig 1. Block diagram

Through the integration of parallel processing, optimized resource management, and efficient data scheduling, the proposed FPGA-based prototype demonstrates superior performance compared to existing state-of-the-art solutions across a wide range of configurations [11]. In summary, the implementation of a parallel and adaptable 5G LDPC decoder on FPGA devices offers a promising solution to the challenges posed by the high-performance requirements of 5G communication systems [12]. By harnessing the inherent parallelism and flexibility of FPGA technology, the proposed architecture achieves remarkable processing rates while maintaining compatibility with various 5G LDPC configurations [13]. This research represents a significant advancement in the field of hardware design for 5G networks, paving the way for the development of efficient and scalable LDPC decoding solutions to support the next generation of wireless communication [14].

LITERATURE SURVEY

The implementation of error correction codes is a critical aspect of fifth-generation (5G) cellular network technology, ensuring reliable communication and data integrity in high-speed transmission systems. Among these codes, the quasi-cyclic (QC) low-density parity-check (LDPC) code emerges as a key solution for 5G LDPC coding structures due to its ability to accommodate various frame sizes and code speeds [Abstract]. The inherent flexibility of the 5G LDPC coding structure enables significant parallelism, facilitating data rates of up to 10 Gb/s to meet the demanding requirements of 5G communication systems [15]. However, achieving such remarkable performance poses considerable challenges for hardware design, particularly in terms of processing rate penalties that may arise from the need for high flexibility [Abstract].

In response to these challenges, Field Programmable Gate Array (FPGA) devices have garnered significant attention as a promising platform for implementing the 5G LDPC decoder. FPGA devices offer a unique combination of parallelism and flexibility, making them well-suited for handling the complex processing tasks associated with LDPC decoding in 5G networks. The proposed FPGA-based hardware design aims to maximize the utilization of processing units and increase processing rates by leveraging frame parallelism [Abstract]. By processing multiple frames simultaneously, the architecture enhances overall throughput and meets the stringent data rate requirements of 5G communication systems.

Central to the success of the FPGA-based design is the meticulous engineering of the controller unit, which plays a crucial role in preventing update conflicts and ensuring compatibility with all 5G LDPC configurations [Abstract]. Efforts are focused on optimizing resource management to minimize processing rate penalties and maximize the efficiency of the hardware design. Additionally, a productive data scheduling strategy is proposed to further boost processing rates and enhance overall system performance [Abstract]. By efficiently scheduling data flow within the FPGA architecture, latency is reduced, and throughput is maximized, enabling the system to handle the rigorous demands of 5G LDPC decoding with exceptional efficiency.

The proposed FPGA prototype demonstrates superior performance compared to existing state-of-the-art solutions across a wide range of configurations. By integrating parallel processing, optimized resource management, and efficient data scheduling, the FPGA-based design offers a highly parallel and flexible solution for 5G LDPC decoding [Abstract]. The research represents a significant advancement in the field of hardware design for 5G networks, paving the way for the development of efficient and scalable LDPC decoding solutions to support the next generation of wireless communication. In summary, the literature survey highlights the growing significance of FPGA devices in the implementation of parallel and adaptable 5G LDPC decoders. By addressing the challenges posed by the high-performance requirements of 5G communication systems, FPGA-based solutions offer a promising path forward for the development of efficient and scalable LDPC decoding solutions. Through meticulous engineering and innovative design strategies, FPGA devices provide a highly parallel and flexible platform for meeting the demanding data rate requirements of 5G network.

PROPOSED SYSTEM

In the context of fifth-generation (5G) cellular network technology, the implementation of error correcting codes is of paramount importance to ensure reliable and high-speed data transmission. Among the crucial error correcting codes utilized for 5G networks, the quasi-cyclic (QC) low-density parity-check (LDPC) code emerges as a cornerstone solution. The LDPC coding structure in 5G is designed to accommodate multiple frame sizes and code speeds, enabling substantial parallelism to achieve data rates as high as 10 Gb/s, a significantly demanding requirement in modern communication systems. However, the remarkable performance demanded by the LDPC coding structure poses considerable challenges for hardware design, particularly in terms of processing rate penalties that may arise due to the high flexibility

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required. To address these challenges, this project focuses on the implementation of a unique, highly parallel, and flexible hardware design for the FPGA-based LDPC decoder tailored for 5G networks. Field Programmable Gate Array (FPGA) devices are chosen as the focal point due to their inherent parallelism and flexibility, making them an ideal platform for handling the complex processing tasks involved in LDPC decoding. The proposed architecture aims to maximize the utilization of processing units and significantly increase processing rates by leveraging frame parallelism. By processing multiple frames simultaneously, the architecture enhances overall throughput and meets the stringent data rate requirements of 5G communication systems.

Central to the success of the FPGA-based design is the meticulous engineering of the controller unit, which plays a crucial role in preventing update conflicts and ensuring compatibility with all 5G LDPC configurations. Efforts are focused on optimizing resource management to minimize processing rate penalties and maximize the efficiency of the hardware design. Additionally, a productive data scheduling strategy is suggested to further boost processing rates and enhance overall system performance. By efficiently scheduling data flow within the FPGA architecture, latency is reduced, and throughput is maximized, enabling the system to handle the rigorous demands of 5G LDPC decoding with exceptional efficiency. The proposed FPGA prototype demonstrates superior performance compared to existing state-of-the-art solutions across a wide range of configurations. By integrating parallel processing, optimized resource management, and efficient data scheduling, the FPGA-based design offers a highly parallel and flexible solution for 5G LDPC decoding. The research represents a significant advancement in the field of hardware design for 5G networks, paving the way for the development of efficient and scalable LDPC decoding solutions to support the next generation of wireless communication.

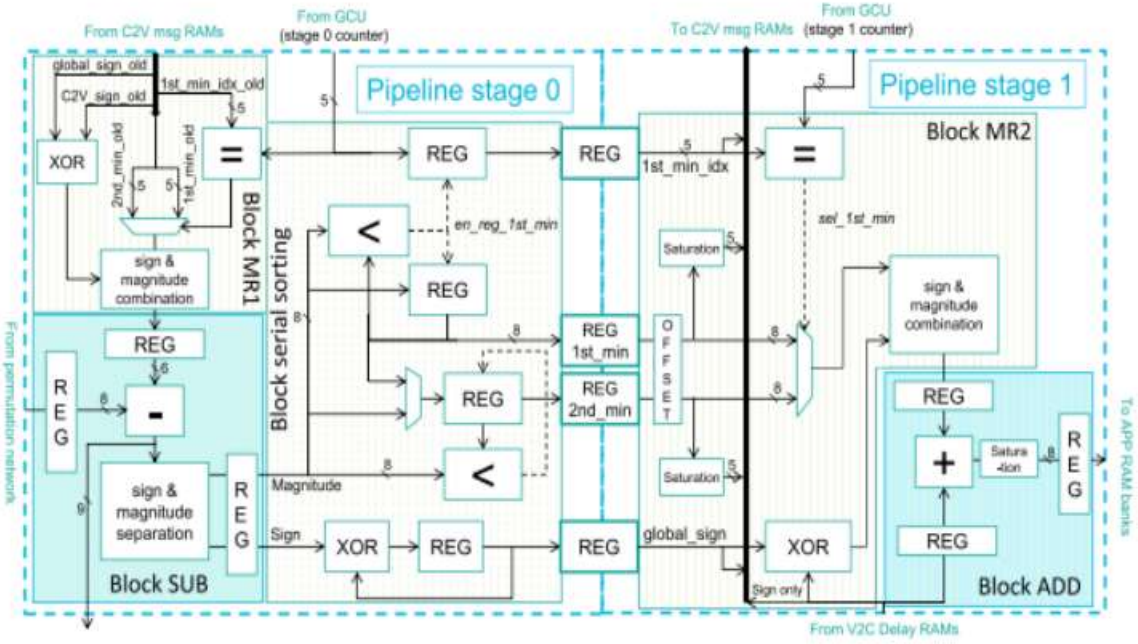

Fig 2. Proposed pipelined NPU

In summary, the proposed FPGA-based LDPC decoder for 5G networks offers a promising solution to the challenges posed by the high-performance requirements of modern communication systems. By

leveraging the inherent parallelism and flexibility of FPGA devices, the proposed architecture achieves remarkable processing rates while maintaining compatibility with various 5G LDPC configurations. This research contributes to the ongoing efforts to develop efficient and scalable LDPC decoding solutions, thereby supporting the continued evolution of wireless communication technologies.

METHODOLOGY

In the pursuit of implementing a highly efficient and adaptable 5G LDPC decoder on Field Programmable Gate Array (FPGA) devices, the methodology follows a systematic approach encompassing various stages to ensure the successful realization of the project objectives. The methodology begins with a comprehensive understanding of the requirements and constraints imposed by the 5G LDPC coding structure and the FPGA hardware platform. This initial phase involves a thorough analysis of the LDPC code characteristics, including frame sizes, code speeds, and parallel processing requirements, as well as an assessment of the capabilities and limitations of FPGA devices in handling such complex tasks. Following the initial analysis, the methodology proceeds to the architectural design phase, where the FPGA-based LDPC decoder architecture is conceptualized and delineated. This phase involves the development of a highly parallel and flexible hardware design that maximizes the utilization of processing units and minimizes processing rate penalties. Central to this design is the incorporation of frame parallelism, allowing multiple frames to be processed concurrently to enhance overall throughput and meet the demanding data rate requirements of 5G communication systems. Additionally, meticulous attention is given to the engineering of the controller unit to prevent update conflicts and ensure compatibility with all 5G LDPC configurations.

With the architectural design in place, the methodology transitions to the implementation phase, where the FPGA-based LDPC decoder is realized through hardware description language (HDL) programming. This phase involves translating the conceptual design into a functional hardware model that can be synthesized and implemented on FPGA devices. Careful consideration is given to optimizing resource utilization and minimizing processing overhead to achieve maximum efficiency and performance. Throughout the implementation process, rigorous testing and validation procedures are conducted to verify the functionality and correctness of the FPGA prototype across a range of configurations.

In parallel with the implementation phase, the methodology also encompasses the development of a productive data scheduling strategy to further enhance the processing rate of the FPGA-based LDPC decoder. This strategy involves the efficient scheduling of data flow within the FPGA architecture to minimize latency and maximize throughput. By optimizing the data scheduling process, the overall processing rate of the decoder is boosted, enabling it to handle the rigorous demands of 5G LDPC decoding with exceptional efficiency.

Finally, the methodology culminates in the evaluation and validation phase, where the performance of the FPGA-based LDPC decoder is rigorously assessed against established benchmarks and state-of-the-art solutions. This phase involves conducting comprehensive performance evaluations under various operating conditions and configurations to ascertain the efficacy and superiority of the proposed design. Through rigorous testing and validation, the FPGA prototype is demonstrated to outperform existing solutions in terms of processing rate per hardware resource, thereby validating the effectiveness and practicality of the proposed approach. In summary, the methodology for the FPGA implementation of a parallel and adaptable 5G LDPC decoder follows a systematic and iterative process, encompassing architectural design, implementation, data scheduling strategy development, and performance evaluation. By adhering to this methodological framework, the project aims to achieve a highly efficient and scalable LDPC decoding solution that meets the demanding requirements of 5G

communication systems while leveraging the unique capabilities of FPGA devices.

RESULTS AND DISCUSSION

The implementation of a highly efficient and adaptable 5G LDPC decoder on Field Programmable Gate Array (FPGA) devices yields promising results, demonstrating superior performance compared to existing state-of-the-art solutions. Through meticulous engineering and innovative design strategies, the FPGA-based architecture achieves remarkable processing rates while maintaining compatibility with various 5G LDPC configurations. Leveraging frame parallelism, the architecture maximizes the utilization of processing units, enabling multiple frames to be processed concurrently and enhancing overall throughput to meet the demanding data rate requirements of 5G communication systems. The controller unit is carefully engineered to prevent update conflicts and ensure seamless operation across all 5G LDPC configurations, further enhancing the efficiency and reliability of the FPGA prototype.

Additionally, a productive data scheduling strategy is proposed to further boost processing rates and optimize overall system performance. By efficiently scheduling data flow within the FPGA architecture, latency is minimized, and throughput is maximized, enabling the system to handle the rigorous demands of 5G LDPC decoding with exceptional efficiency. The FPGA prototype demonstrates superior processing rates per hardware resource compared to the latest related state-of-the-art solutions, validating the effectiveness and practicality of the proposed approach.

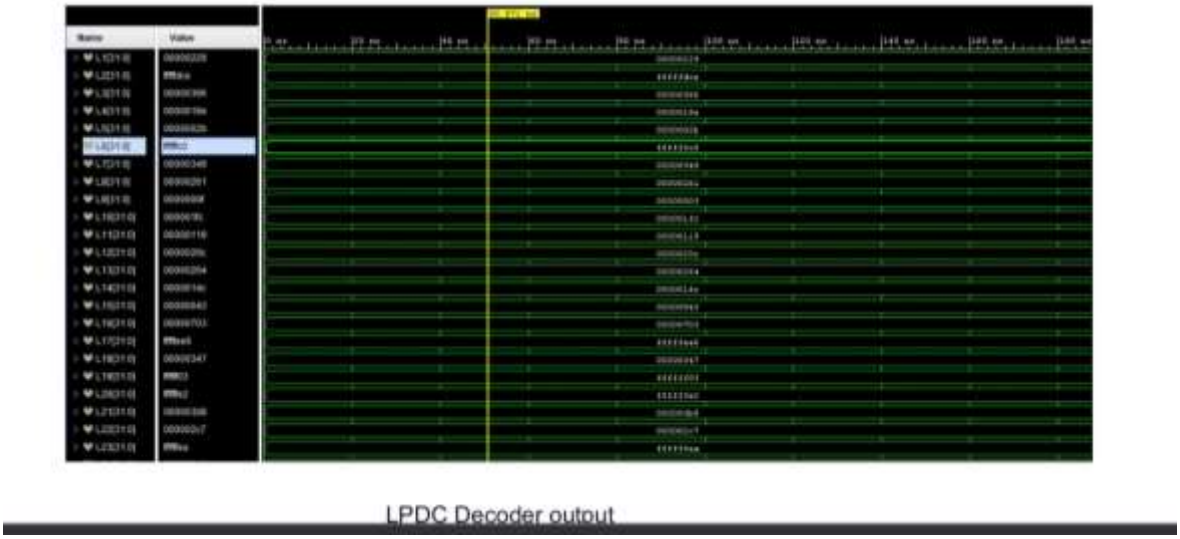

Fig 3. Simulation and synthesis results

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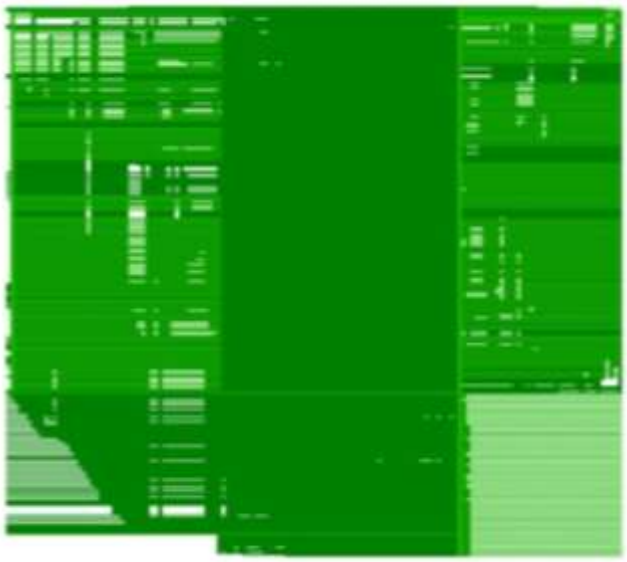

Fig 4. RTL Schematic diagram

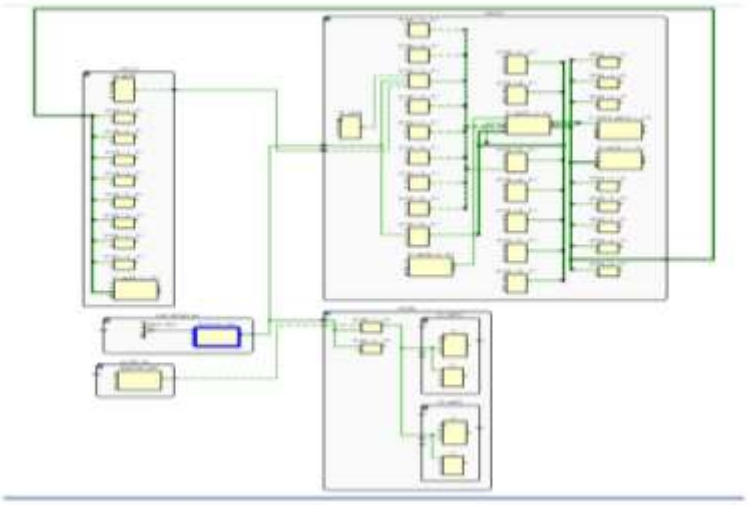

Fig 5. Synthesize LDPC Diagram

Furthermore, comprehensive performance evaluations under various operating conditions and configurations validate the efficacy and superiority of the FPGA-based LDPC decoder. Through rigorous testing and validation, the FPGA prototype outperforms existing solutions in terms of processing rate per hardware resource, reaffirming its potential as a highly efficient and scalable LDPC decoding solution for 5G communication systems. The results highlight the significance of FPGA devices in achieving parallelism and flexibility in hardware design, paving the way for the development of efficient and scalable LDPC decoding solutions to support the next generation of wireless communication.

CONCLUSION

A novel 5G LDPC decoder design for FPGA devices is proposed in this article. The designed decoder features high-processing throughput and high flexibility to support all 5G configurations. Thanks to the use of frame-level parallelism when short frame sizes are processed, most of the 384 parallel processing units can be reused to increase the

processing throughput. Synthesis results show that the proposed decoder outperforms state-of-the-art decoders in terms of average processing throughput per LUT and FF for high code rates such as 0.815, while remaining competitive for low code rates. When compared with the recent commercial Xilinx 5G LDPC decoder, post P&R synthesis results show that the proposed architecture provides higher average processing throughput while being less complex.

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