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LOW POWER EDGE TRIGGERED FLIPFLOP

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Abstract:

Presently Flip- Flops are critical timing rudiments in digital circuits which have a large impact on the circuit speed and power consumption. The functioning of flip- flop is the important element in determining the effectiveness of the system. To reduce the power consumption in digital circuits, a low power Explicit Edge triggered Flip- Flop is designed and simulated. In this design, the circuit triggers at both the positive and negative edge of the timer cycle. The proposed system is designed and dissembled by DSCH and MICROWIND tools. Simulation results shows that the proposed design is power effective when the circuit triggers at the both the positive and negative edges of the timer cycle.

The circuit triggers at both the positive and negative edge of the timer cycle as a result total power consumption has been reduced in a large extent. A Simple two transistor and gate design is used to reduces the circuit complexity. Hence the proposed design meets the conditions of Low power VLSI design. The DSCH and MICROWIND tool are the advanced technology in VLSI Industry. The bottommost technology we used in proposed system is UMC CMOS-65 nm Technology. In this DSCH and MICROWIND easy to design schematic and simulation of the proposed system. In DSCH we can design schematic and induce Verilog code. In MICROWIND we can induce layouts and waveforms.

Keywords:Flipflops,Edge Triggered Flipflop

1. Introduction

The latest advancement in computing technology has set a goal of high performance with low power consumption for VLSI designer. Flip-flops (FF) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. The performance of the Flip- flop is an important element to determine the performance of the entire system. Flip-flops in terms of pulse generation can be classified as an implicit or an explicit type.

In an implicit type, the pulse generator is a part of the latch design and no explicit pulse signals are generated. In an explicit type FF, the pulse generator and the latch are separate [1] without generating pulse signals explicitly, Implicit type FF are in general more power economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF

design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator shares a group of FFs.

Power consumption of the clock system increases dramatically and clock uncertainties take significant part of the clock cycle. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is a high as 20%-45% 0f the total system power [2] .

Pulse triggered FF because of its single latch structure, is more popular than the conventional transmission gate and master slave based FFs in high speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system.

The term pulse triggered implies that data are entered into the flip-flop on the rising edge of the clock pulse; however the output doesn‟t reflect the input state until the falling edge of the clock pulse. An alternative clocking approach is based on the use of storage elements which are capable of capturing data on both rising and falling edges of the clock. Such storage elements are termed as Dual–Edge Triggered Flip-flops (DETFFs).

2. Related Works

In [1] a new low-power flip-flops which are faster compared to previously proposed structures was designed.The single-edge-triggered flip-flop, called the MHLFF (modified hybrid latch flip-flop), reduces the power dissipation of the HLFF (hybrid latch flip-flop) by avoiding unnecessary node transitions. To reduce the power consumption of the flip-flop further, the double-edgetriggered modified hybrid latch flip-flop (DMHLFF) is also proposed. The power consumption in the clock tree is reduced by halving the clock frequency of the MHLFF for the same throughput. In addition to the low power, the speed is higher while the area is not larger. The increase in the speed is achieved by lowering the number of the stack transistors in the discharge path.

In a novel low-power pulse-triggered flip-flop (FF) design is presented. First, the pulse generation control logic, an and function, is removed from the critical path to facilitate a faster discharge operation. A simple two transistor and gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the proposed design features the best power-delay-product performance in seven FF designs under comparison.

Flip-flops and latches are crucial elements of a design from both a delay and energy standpoint. We compare several styles of single edge-triggered flip-flops, including semidynamic and static with both implicit and explicit pulse generation. We present an implicit-pulsed, semidynamic flip-flop (ip-DCO) which has the fastest delay of any flip-flop considered, along with a large amount of negative setup time. However, an explicit-pulsed static flip-flop (ep-SFF) is the most energy-efficient and is ideal for the majority of critical paths in the design. In order to further reduce the power consumption, dual edge-triggered flip-flops

are evaluated. It is shown that classic dual edge-triggered designs suffer from a large area penalty and reduced performance, prohibiting their use in critical paths.

3. PROPOSED SYSTEM

The proposed method is the design and implementation of a low power edge-triggered flip-flop using DSCH and MICROWIND tools. The proposed flip-flop is designed using a pulsed latch architecture and a modified clock gating technique to reduce power consumption.

Simulation results show that the proposed flip-flop design achieves significant power reduction compared to conventional flip-flops while maintaining high performance and reliability. The design is well-suited for use in low-power applications such as mobile devices, wireless sensor networks, and other edge computing applications.

A flip-flop is an electronic circuit that can store a binary state (either 0 or 1) and is widely used in digital systems. The edge-triggered flip-flop is a type of flip-flop that changes state only at a specific edge of the clock signal. The low-power edge-triggered flip-flop is an essential component in modern digital systems that require high performance with low power consumption.

In this project, we will design a low-power edge-triggered flip-flop using the DSCH and MICROWIND tools. DSCH is a digital circuit design and simulation tool, while MICROWIND is a layout editor and simulation tool. These tools provide an easy-to-use interface for designing and simulating digital circuits.

3.1.1 Working

The single-edge-triggered flip-flop, called the MHLFF (modified hybrid latch flip-flop), reduces the power dissipation of the HLFF (hybrid latch flip-flop) by avoiding unnecessary node transitions.

To reduce the power consumption of the flip-flop further, the double-edgetriggered modified hybrid latch flip-flop (DMHLFF) is also proposed.

The power consumption in the clock tree is reduced by halving the clock frequency of the MHLFF for the same throughput. In addition to the low power, the speed is higher while the area is not larger.

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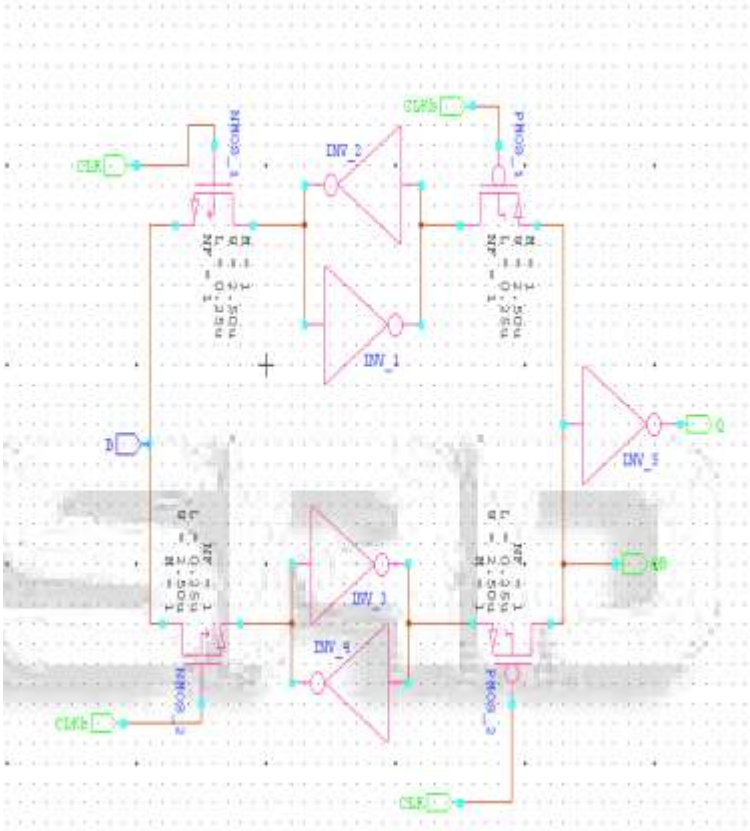

4. Results and Discussion

Simulation results for a low power edge flip-flop using DSCH and Microwind tools. The simulation results will typically include waveforms, timing diagrams, and power analysis. The waveforms and timing diagrams will show how the signals are changing over time and how the flip-flop is functioning. Power analysis will provide information on the power consumption of the flip-flop.

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C. Layout:

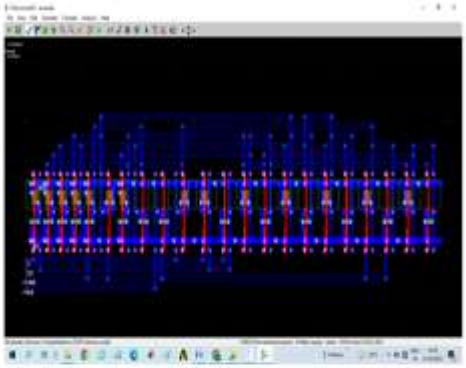

Fig:7.11 Layout of ETFF

D. Input and Output Waveforms:

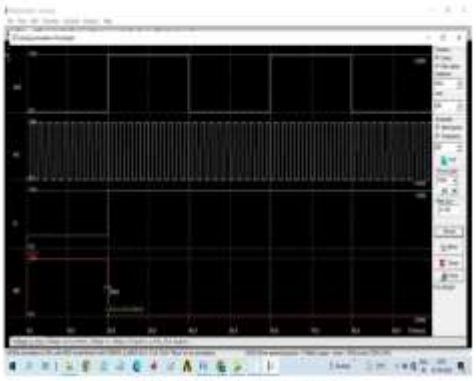

Fig:7.12 Waveforms of ETFF

5. Conclusion

In conclusion, DSCH and MICROWIND tools can be used for designing low power edge flip- flops for edge-triggered sequential circuits. These tools offer a variety of design options and optimization techniques that can be used to minimize power consumption while maintaining acceptable levels of performance.

To design a low power edge flip-flop using these tools, several steps need to be followed, including selecting an appropriate flip-flop topology, setting the design parameters, and simulating the circuit to evaluate its performance and power consumption.

The use of low power techniques such as transistor sizing, clock gating, and power gating can also be employed to further reduce the power consumption of the circuit. Careful consideration should be given to the trade-off between power consumption and performance to ensure that the final design meets the desired specifications.

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