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COMMON GATE CMOS LNA IN 2.4 GHZ ISM BAND USING ADS (ADVANCED DESIGN SYSTEM)SOFTWARE

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ABSTRACT
This paper presents the design of a common gate CMOS LNA for RF applications that achieves high linearity and input impedance matching using the Advanced Design System (ADS) software. The LNA is designed to operate in the 2.4 GHz ISM band and is implemented in a standard 0.016 µm CMOS process. The design methodology is applicable to other frequency bands as well. The proposed LNA achieves high linearity with a third-order input intercept point (IIP3) and high input impedance matching with a return loss of better than across the frequency band of interest. The design incorporates a two-stage LNA topology and utilizes passive devices such as inductors and capacitors for input matching and output matching. The ADS software is used for schematic capture, simulation, and layout design. The simulated results show that the proposed LNA meets the design specifications and achieves excellent performance metrics such as a gain and a noise figure . The proposed design is suitable for low-power and low-noise RF applications in wireless communication systems.
Keywords: ADS (Advanced Design Simulation) Software; LNA (Low Noise Amplifier); CMOS (Complementary MOSFET); Common Gate (CG).

Introduction:
Since customers want high levels of flexibility and complexity in their wireless communication receivers, as well as he ongoing evolution of standards, the front-end of these devices is getting more sophisticated every day. The low noise amplifier (LNA), which is a significant component of the RF receiver's front end, is present. As we can anticipate the total noise performance of wireless receivers by knowing the low noise amplifier's specification, the performance of the low noise amplifier has an impact on the performance of the entire RF receiver system [1].

When the low noise amplifier has a high gain and a low noise figure, the noise figure of the stages that follow it in the receiver is reduced. As a result, one of a low noise amplifier's key feature is to boost the incoming signal without introducing further noise. However, it is challenging to obtain low noise figure at modern technology while having linearity, as required by wireless standards, because to the ongoing demand for decrease in the sizes of devices and low supply voltage. Additionally, the characteristics of low noise amplifiers, including noise figure, linearity, gain, and input matching, interact with one another [2]. A variety of applications employ low noise amplifiers. Low noise amplifiers are used in RF communication systems, two-way radio, personal digital assistants (PDA), computers, and other devices. Commonly used for narrowband applications, the inductively degenerated common-source (CS) low noise amplifier topology offers higher gain and lower noise figure, but below 10 GHz, it is more challenging to achieve impedance matching at the input than the common gate (CG) low noise amplifier topology. Furthermore, compared to common gate low noise amplifier design, inductively degraded common source LNA topology requires more inductors (4 or

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6 for differential amplifier). As a result, the inductively degenerated common source low noise amplifier architecture occupies a larger area on the chip [3] [4]. In order to achieve this, the common gate (CG) low noise amplifier architecture has been presented in this research. The proposed circuit, which is seen in figure 1, is used for input matching. Common gate low noise amplifiers, however, have low gain and large noise figures because of impedance matching restrictions [5] [6]. The below figure describes about the common gate construction between the two transistors M1 & M2. The VDD supply is given precisely as 0.8 v and the passive elements that are attached to RFIN, RFOUT are C1 and C5.

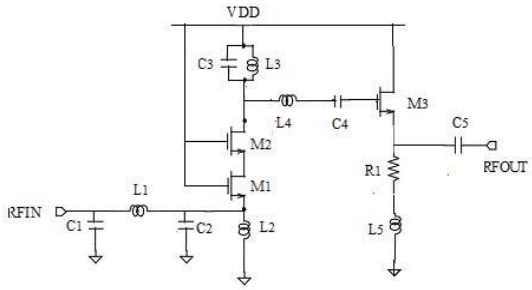

Fig 1. Proposed Common Gate Cmos Lna

Literature survey

Everyone is aware that the LNA is one of the most crucial and fundamental components of RF receivers and that it impacts the device's overall performance. In order to lessen the noise effect of the following circuits for the RF communication system, the focus of this study is to increase the power gain and decrease the noise with reasonable power consumption for the LNA. The design of a fully integrated 2.4 GHz CMOS LNA is described in this study since WLAN and Bluetooth may both operate at this frequency. In this study, an additional gate-source capacitor is added to the input transistor of the cascade architecture to help the LNA achieve good noise and input matching while using a manageable amount of power. The primary goal in the design of LNA is to achieve higher power gain with reasonable noise figure. In this design we used the inductive source degeneration cascade architecture. We neglect the bias circuits for short. The cascade topology is extensively used for most of CMOS LNA designs because cascade amplifier has the benefit of low power consumption along with minimum noise figure and it also provides good isolation between input and output stage of the LNA. The bias circuit provides a stable voltage which can make sure that transistors always remain in saturation region which is required for the desired results of LNA [1].

The low-noise amplifier (LNA) is a critical component of a conventional radio receiver since it dominates the sensitivity. Many considerations exist in LNA design, including noise figure (NF), gain, linearity, impedance matching, and power dissipation. A variety of LNA design strategies have been described to achieve these objectives. The classical noise matching (CNM) technique, the SNIM technique, the power-constrained noise optimisation (PCNO) approach, and the power-constrained simultaneous noise and input matching (PCSNIM) technique are a few examples. However, the previously published publications only detail one of these methodologies, and the analytical approaches are contradictory with one another [2].

The market for RF integrated circuits (RFICs) for wireless LANs has grown in popularity due to its potential cheap cost and system level integration. The need for low voltage operational RF chips with lower power consumption and a superior performance/price ratio is skyrocketing. While CMOS technology scaling benefits digital circuits, it does not benefit RF analogue circuits, and redesigning

RF analogue circuits in a new CMOS technology is challenging. The most serious effect of technology scaling on RF analogue designers is a drop in voltage supply [3]. Insufficient voltage room can cause some circuit topologies to fail to meet the requisite parameters or possibly fail to operate.

In wireless communications, a common-gate (CG) LNA is extensively employed. The major disadvantage of the CG LNA is its high minimum noise figure (NF), which is often greater than 3 decibels. As a result, the NF is somewhat greater than that of an inductively degenerated common-source (IDCS) LNA, limiting the use of the CG LNA. However, a typical IDCS LNA has limited input matching capabilities, limiting its use in wideband systems. To address this issue, an input matching network with numerous on chip inductors was constructed. As a result, the noise level of an IDCS LNA increases [4]. The CG input stage, on the other hand, provides a very basic input matching realising them.

The proliferation of wireless communication protocols used in a single geographic region, as well as occupying small frequency bands, severely limits RF-system linearity. Furthermore, the pricey front-end module (FEM), which requires a highly linear receiver, is being simplified/eliminated in radio research. Because the low noise amplifier (LNA) is the first component in the receiver chain, it must be linear enough to minimise interference while maintaining high sensitivity. LNA linearization algorithms should be simple, use minimal power, and maintain noise figure (NF), gain, and input matching. Many conventional linearization approaches are impractical for LNAs. Resistive source degeneration and floating-gate input attenuation, for example, diminish gain and impair NF or input matching. As a result, LNA linearization is substantially more difficult [5].

This study describes a low power, low noise differential amplifier developed for Wireless Sensor Network (WSN) applications in the TSMC 0.18 m RF CMOS technology. It should function well at a frequency of 2.44 GHz, and the forward gain is tuneable, ranging from 12 dB to -2 dB in 2 dB increments. In this study, a two-stage cascade common-gate (CG) architecture and two external inductor choke coils are employed to accomplish LNA input matching while consuming little power, and a differential inductor is used as the load to produce appropriate gain while reducing chip space. Cadence Spectre was used to simulate and validate it [6].

A wideband or turn able low-noise amplifier (LNA) is a critical circuit block in realising a reconfigurable multi-standard radio receiver. Only one integrated receiver chain with a single IC input pin (single-ended or differential) is used in a reconfigurable receiver to receive any desired radio standard at a time. As a result, because the RF input signal pins of the LNA in the receiver RFIC are shared across several standards, broad band input matching is necessary, or narrowband matching must be adjusted to the desired frequency band. The integrated reconfigurable receiver can be preceded by a bank of external RF preselect ion filters and switches, or, in the future, by a frequency adjustable RF band pass filter [7].

Proposed Methodology

For input matching in a traditional common gate (CG) low noise amplifier design, the main transistor's transconductance should equal the inverse of the source resistance, i.e., 1/gm = Rs. This condition should hold true over the whole frequency range of operation. Short channel device transconductance is provided by

$g_m = [\mu C_{ox}/2]*[W/L]*[1/\theta]$----(1)

where,

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W and L are the primary transistor's channel width and length, respectively, while ș is a fitting parameter. According to equation (1), the primary transistor's transconductance (gm) is independent of biassing current. As a result, the channel width of the primary transistor (W) is technology dependent, and its value is determined by:

$W_{opt} = [2/\mu C_{ox}]*[\theta*L*g_m]$---(2)

Since linearity and gain are two opposing poles that are difficult to reconcile, enhancing gain degrades linearity and vice versa. As a result, pi-matching is employed to improve the forward gain of LNA by giving an extra degree of freedom. Because of its superior features, the complementary MOS (CMOS) transistor is employed in low noise amplifiers. High noise immunity and static power are two significant properties of CMOS transistors. The internal structure of CMOS includes a sequence of NMOS and PMOS transistors. As a result, the power is absorbed by the series combination when it switches between ON and OFF states, because one of the transistors in the series connection is always turned off. As a result, CMOS devices generate less heat than other logic families such as transistor transistor logic (TTL), NMOS, and so on. The suggested LNA is made up of common gate and common source stages, with the common gate topology being used for input matching in the first stage. For the input matching of a common gate amplifier, parallel resonance is present rather than series resonance. The common gate amplifier's quality factor (Q) is stated as

$Q_{CG} = w_o{}^{Cgs/g_m}$ (3)

$W_o = 1/L_sC_{gs}$ (4)

The power gain of a common gate amplifier, on the other hand, is smaller than that of a common source amplifier. To compensate for the power gain, we employ a common source amplifier in the second stage of our circuit. The LC tank circuit is matched for the centre frequency to guarantee that the circuit is optimised. Inductor L2 is used to prevent RF current leakage to ground. The value of L2 for a common gate amplifier is greater than that of a common source amplifier. At the input, C1, L1, and C2 form a pi-matching network, while C5 is a DC blocking capacitor.

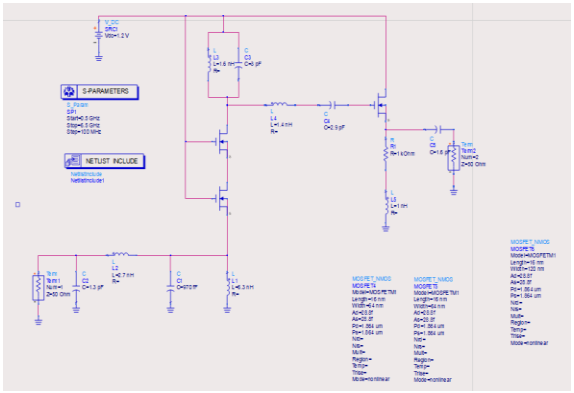

Fig 2. Schematic of Proposed Common Gate LNA

Results and discussion

Simulations of the proposed LNA for 16nm CMOS process were performed using ADS. The input reflection coefficient (S11) is 0.12 dB as shown in figure 3 and the output reflection coefficient (S22) is -1.25 dB as shown in figure 6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S12), as shown in figure 4, is –60.604 dB. From the result, it can be concluded that the simulated amplifier’s characteristics summary is presented .

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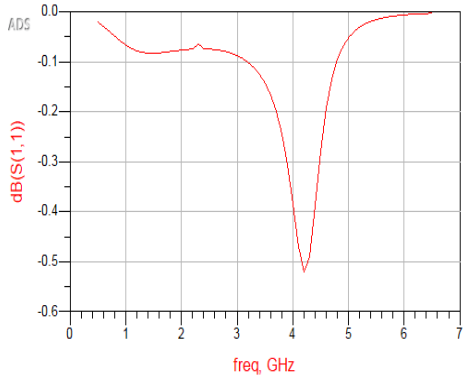

Fig 3. input reflection coefficient (S11)

S11 (input reflection coefficient) represents how much power is reflected from the input antenna. Therefore, it is also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. For 4.4 GHz, as shown in figure 3, the value of S11 is -0.894 db.

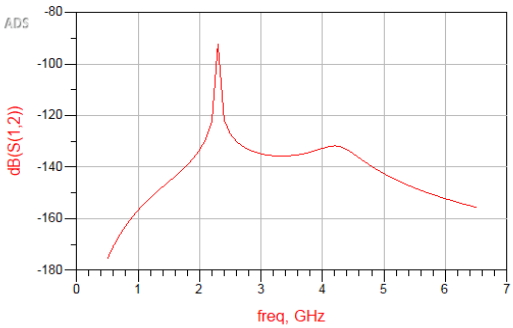

Fig 4. reverse isolation (S12)

S12 (reverse transmission coefficient) represents power received at input antenna relative to power input at output antenna. Also, known as reverse isolation, it measures how much the input signal is reflected back. For 2.5 GHz, as shown in figure 4, the value of S12 is -60.604 db.

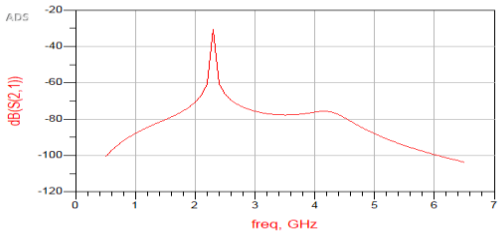

Fig 5.S21 (forward transmission coefficient)

S21 (forward transmission coefficient) represents power received at output antenna relative to power input at input antenna. Also known as forward gain, it measures how well the signal goes from input to output. For 2.5 GHz, as shown in figure 5, the value of S21 is -30 dB

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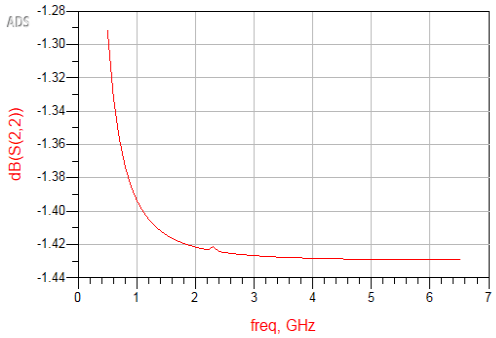

Fig 6.S22 (output reflection coefficient)

S22 (output reflection coefficient) represents power reflected from output antenna. Also known as output return loss, it represents the measure of matching of the output impedance to load impedance. For 1.4 GHz, as shown in figure 6, the value of S22 is -1.246 db.

Conclusion and future scope

Many current communication systems rely on low noise amplifiers (LNAs) with strong linearity and input impedance matching. They are generally the initial stage in a receiver chain and are used to amplify weak signals with little distortion and noise. As there is a rising demand for high-speed and high-performance communication systems, such as 5G and beyond, the future scope of LNAs with high linearity and high input impedance matching is promising. These systems necessitate LNAs capable of operating at higher frequencies and with reduced power consumption while maintaining good linearity and low noise. Using advanced semiconductor technologies, such as gallium nitride (Gan) or silicon carbide (Sic), which offer greater breakdown voltages and better thermal performance than classic silicon-based technologies, is one strategy to achieve high linearity and low noise in LNAs. These sophisticated technologies may also be utilised to create LNAs with better input impedance matching, lowering input losses and improving overall system performance. Another strategy is to employ unique circuit topologies and design approaches, such as distributed amplifiers or noise-cancelling techniques, to increase linearity and minimise noise while retaining high input impedance matching. Overall, the future of LNAs with high linearity and good input impedance matching is bright, as developments in semiconductor technology and circuit design lead to more efficient and high-performance communication systems.

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