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DESIGN OF DIGITAL PHASE LOCKED LOOP DEMODULATOR BASED ON FPGA

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Abstract- This paper studied the principle of analogue phase-locked loop demodulation and work process of digital phase-locked loop.It is found that the higher the reference signal frequency is the smaller the duty ratio of the discriminator output signal. Carrier detection is achieved by using this relationship.The experimental results indicate that the demodulator based on the principle could realize high-quality transmission of digital signals and could be an effective FM communication mode for studying wireless transmission of digital signals.

The all-digital phase-locked loop (ADPLL) has been widely used in digital communication and automatic control field because of the advantages of stable performance, reliable operation and so on. With the development of digital signal processing technology and programmable devices, the onchip realization of all-digital phase-locked loop has become a hot topic. Analog and digital PLL circuits consists of four basic element i.e phase detector, low pass filter , variable frequency oscillator and feedback path. There are several variation of PLL, DPLL is one of the variation.

Keywords: PLL, ADPLL, FM.

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Introduction:

The simplest PLL is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. Keeping the input phase and output phase in lock step also implies keeping the input and output frequencies the same. Phase-locked loops are widely employed in radio, telecommunications and other electronic applications. A single IC can provide a complete phase-locked-loop building block; the technique is widely used in modern electronics devices with output frequencies from few hertz to gigahertz. An analog PLL with a digital phase detector as edge trigger JK and may have digital divider in the loop as NCO. Phase-locked loops are widely used for synchronization purpose, demodulate frequency modulated signals.

As components for digital signal processing are steadily improving, more and more applications of processing signals in the radio-frequency (RF) range are moving from the analog to the digital domain. The phase-locked loop (PLL) possesses a wide range of applications in modern communication systems. The all-digital phase-locked loop (ADPLL) has been widely used in digital communication and automatic control field because of the advantages of stable performance, reliable operation.

Literature Survey:

The motivation of this paper arose from the need of a flexible offset local oscillator (offset LO) in a fast phase detection system for closed-loop RF controls in the heavy-ion particle accelerator SIS18 at GSI. Since the signal frequencies of that application are in the range of tens of megahertz, the processing power of a microcontroller with integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) is insufficient, while the design of a custom application-specific integrated circuit (ASIC) for quantities of a few hundreds is too expensive.

This area of application is covered by field-programmable gate arrays (FPGAs), which play an important role in high-energy physics experiments because they offer the speed, density, and computational power that are otherwise only achievable with ASICs and are flexible like microcontrollers (in terms of configurability). Therefore, an FPGA with fast ADCs and DACs was chosen as the platform for the offset LO that is based on a discrete-time all-digital PLL (ADPLL). ADPLLs have been described and analyzed in several publications, but there are only a few reports about FPGA-based or discrete-time PLL designs.

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Existing Method:

Block diagram of DPLL consists of digital blocks. It takes digital signal only as input signal. Structure of DPLL consists of three basic blocks Phase Detector, Loop filter and NCO. Figure gives basic block of PLL. The main aim of DPLL is to make synchronization among the phase of input signal and output signal and also the frequency. Phase detector is used to reduced the signal error differences among two signals, loop filter is used to removed the noise and the output of NCO is used to make the output signal closer to the input signal.

Phase Detector Phase Detector is also known as Phase Comparator it makes comparison between input signal and NCO output signal. In this paper the Phase Detector is design by using Edge triggered JK flip-flop. It contains a JK flip flop. These circuits have the advantage that whilst the phase difference is between ± 180˚a voltage proportional to the phase difference. AC components are not produced when the loop is out of lock and the output from the phase detector can pass through the loop filter to bring the PLL into lock.

Proposed Design:

This paper describes a new ADPLL, where all parts are working as discrete-time components running at a fixed sampling rate. All input and output signals are sampled waveforms coming from ADCs or going to DACs. To avoid the discussed phase detection problems, the sampled input signals are converted first into analytic signals using the Hilbert transform, which is followed by a Cartesian-to-polar conversion. It is shown that, by spending more resources, it is possible to realize a highly linear PD with extended detection range. This makes it possible to analyze and simulate the whole PLL using the z transform, which enormously ease the design process. Apart from the simplified design, the lock-in time becomes independent from the magnitude of a

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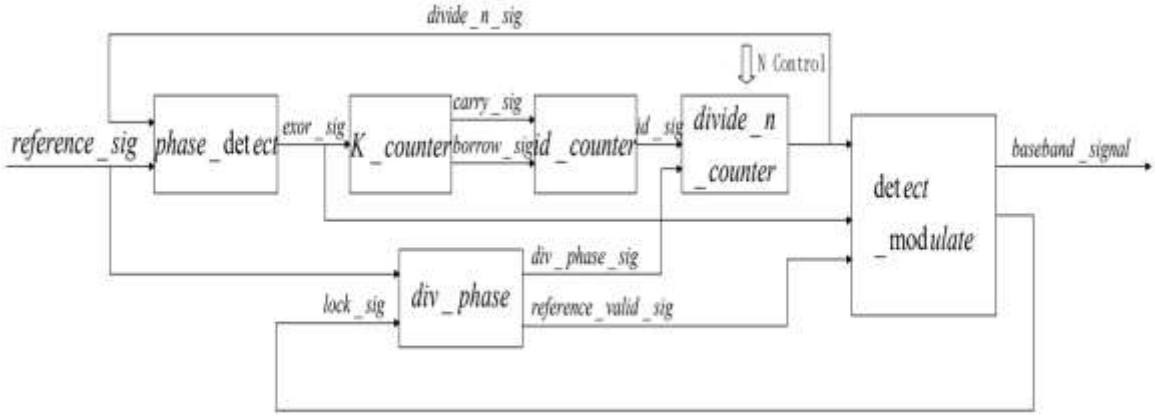

frequency change, and additional circuits for frequency estimation becomes necessary.

The FM wave is amplified by the amplifier and the output of the voltage-controlled oscillator is sent to the phase detector. The output of the phase detector reflects the phase error information of the two input signals. Then the obtained voltage signal passed loop filter changes with the change of the modulation signal frequency so as to realize the mediation process.The div-phase and detect_modulate module, which are used to detect the effective input signal, control phase adjustment, and detect phase locking state.

In the following, two linear PLL models, i.e., one for an approximated continuous PLL with reduced complexity and one exact discrete model, are derived. Next, the resulting properties like coefficient relations, working range, stability, and lock-in range,the implementation details are explained. As mentioned before, the ADPLL is used as an offset LO from which the main requirements to the presented structure were derived. It is described the frequency offset generation.

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SimulationResults:

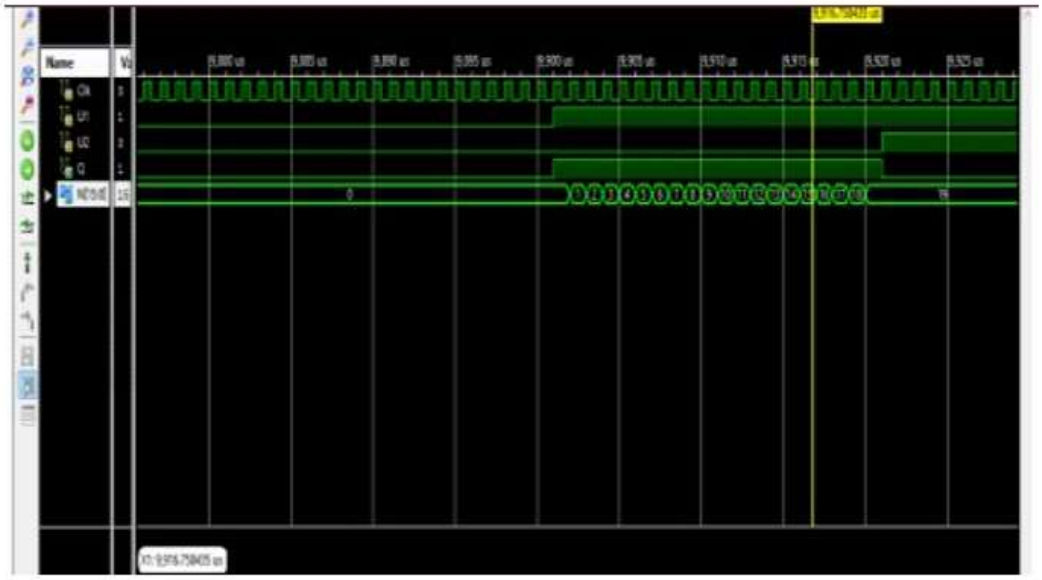

Fig: Simulation Result for Phase detector Stage

Fig: Simulated Result of OFDM Transmitter

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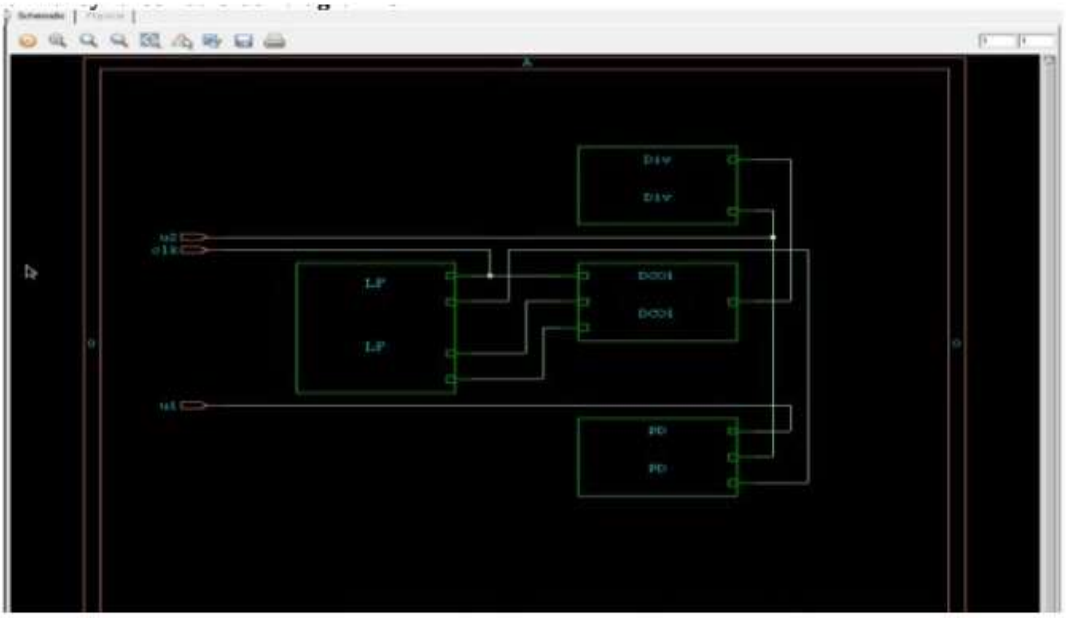

Fig: Synthesized Block Diagram

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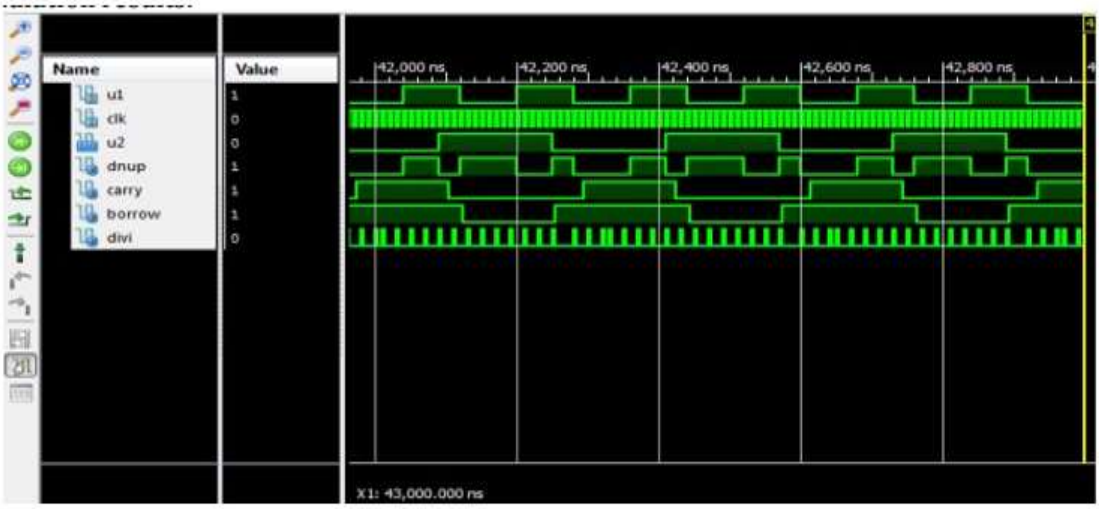

Fig: Simulation Result for Filter cum Counter stage

Conclusion:

Design of an ADPLL for low frequency range has been performed, in view its applications in various fields like wireless communication, biomedical etc, which require a low power, high speed and small devices. The designed can be extended for accumulator based DCO which improves accuracy. Area optimization obtained from the synthesis report shows only 1.3% of device utilization Thus leaving behind a lot of space for other fittings in an SOC IC. This architecture avoids the use of analog vco, provides fine frequency steps, DDs allows exhibits much faster channel switching, Also as a further direction different types of ADPLL architectures can be designed and implemented for various frequencies, depending on its applications. The design and architecture can be modified to increase the range of frequencies and performance of ADPLLS. In fact to enhance the DCO requirements Clock should be typically about three to four times the output. In

present VLSI technologies it is difficult to perform such operations at such speeds especially if power dissipation is critical.

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