Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

DESIGN OF USB Encoder AND DECODER USING VIVADO SOFTWARE

1. Dr. A V S Swathi, Associate Professor, Raghu Institute of Technology (A), email: arinanaswathi@gmail.com, Visakhapatnam.

2. B Sai sunil, UG student, Raghu Institute of Technology (A), email: balususaisunil@gmail.com, Visakhapatnam.

3. B Sai krishna Reddy, UG student, Raghu Institute of Technology (A), email: boreddykrishnakittu3701@gmail.com, Visakhapatnam.

4. Gayathri A, UG student, Raghu Institute of Technology (A), email: sweetyallamsetti@gmail.com, Visakhapatnam.

5. B Manikanta, UG student, Raghu Institute of Technology (A), email: manikantaboddu786@gmail.com, Visakhapatnam.

6. K Eswar Sai Gopal, UG student, Raghu Institute of Technology (A), email: saigopalkolli143@gmail.com, Visakhapatnam.

Abstract- The design and the implementation of 8x10 encoder and 10x8 decoder by using 3 bit down ripple counter has been proposed in this paper .In a ripple counter , a flip-flop output transition serves as source for triggering other flipflops .The clock skew problem can be reduced by using this ripple counter technique. By reducing clocks skew we can reduce the power consumption of hardware. So ripple counter technique has been used in this paper for the purpose of reducing the power consumption of the encoder and decoder circuits .The super speed USB 10GBPS specification adds a 10GBPS speed mode that uses a more efficient data encoding and will deliver effective data.The speed of end product depends on layer architectures and their internal designs.

Physical layer IP core of USB 3.1 includes the DC balanced 128b/132b coding with very fast FPGA from Xilinx family. Scrambling and descrambling modules are also added to support USB 3.1 physical layer transactions. The code is implemented in Verilog. Module 128b/132b encoder needs to be designed to convert 128 bits to 132 bits. A software module needs to be framed for link packet framing, sending and receiving to USB 3.0 Physical layer.

Keywords: USB, USB 3.1, GBPS.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

Introduction:

The VLSI engineers gives more emphasis on the resources used by the hardware. They are trying hard to reduce the consumption of resources which leads to the growth of the VLSI industry. The main resource comes into role is power. Less power consumption will certainly leads to less cost of the hardware. Lot of research is going on reduction of power consumed by the hardware There are many techniques which are used to reduce the power such as clock gating and clock divider etc These techniques can also be used to reduce the clock skew problem and due to removal of clock skew power consumption can be reduced. USB 3.0 adds the new transfer rate referred to as Super Speed USB (SS) that can transfer data at up to 5 Gbit/s (625 MB/s), which is about ten times as fast as the USB 2.0 standard.

Manufacturers are recommended to distinguish USB 3.0 connectors from their USB 2.0 counterparts by blue color-coding of the Standard-A receptacles and plugs, and by the initials SS. In USB 3.0, dual bus architecture is used to allow both USB 2.0 (Full Speed, Low Speed, or High Speed) and USB 3.0 (Super Speed) operations to take place simultaneously, thus providing backward compatibility. Connections are such that they also permit forward compatibility, that is, running USB 3.0 devices on USB 2.0 ports. The structural topology is the same, consisting of a tiered star topology with a root hub at level 0 and hubs at lower levels to provide bus connectivity to devices In this paper, we have designed the 8x10 encoder and 10x8 decoder using Verilog HDL.

Literature Survey:

In the 8x10 encoder design, there are 8 inputs (ABCDEFGH) and these inputs are encoded into 10 outputs (abcdeifghj). For encoding the inputs, two different encoding schemes are used. One is 5 bits to 6 bits encoding and second is 3 bits to 4 bits encoding. Detailed working is referred in the literature In the 10x8 decoder design, there are 10 inputs (abcdeifghj) and these inputs are decoded into 8 outputs (ABCDEFGH). For decoding the inputs, two different decoding schemes are used. One is 6 bits to 5 bits encoding and second is 4 bits to 3 bits encoding.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

Existing Method:

Virtebi algorithm is an approach towards finding the most common sequence of hidden states in all listed states. It is dynamic programming algorithms that find the probability of all observed sequence for each combination. Pr (observed sequence | hidden state combination) It is a feasible procedure to find the common sequence .The complete calculation in each combination is much costly .It is evaluated for the error correction for noise in the digital communications. Virtebi algorithm is familiar algorithm works on the state machine assumption for the conventional codes. By using the system can be modeled at certain state. There are finite numbers of states. There will be a survivor path mostly a common path in a multiple sequence path that can lead to a given state.

It can describe the hardware and the soft ware implementations. The noisy channels are usually corrected by the conventional codes as they are efficient for correcting the corrupted channels.A state machine assumption is used for the functioning of Turbo algorithm. There is finite number of states, at any time system being modeled in some state. The survivor path which is at least one of the most likely paths to the state when number of sequences of paths can be directed to given state. The most likely state is kept by examining all the possible states which are the fundamental assumption of the algorithm. Thus by keeping only one path is necessary and do not need to keep all the track of all states.

Proposed Design:

Dual bus architecture.Cable structure supporting full duplex transmission, Connector supporting cable structure ,Link level power management and Asynchronous notify.Popularity, Transfers HD data in short time and Superior than its competitors. 10X performance increase over USB 2.0.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

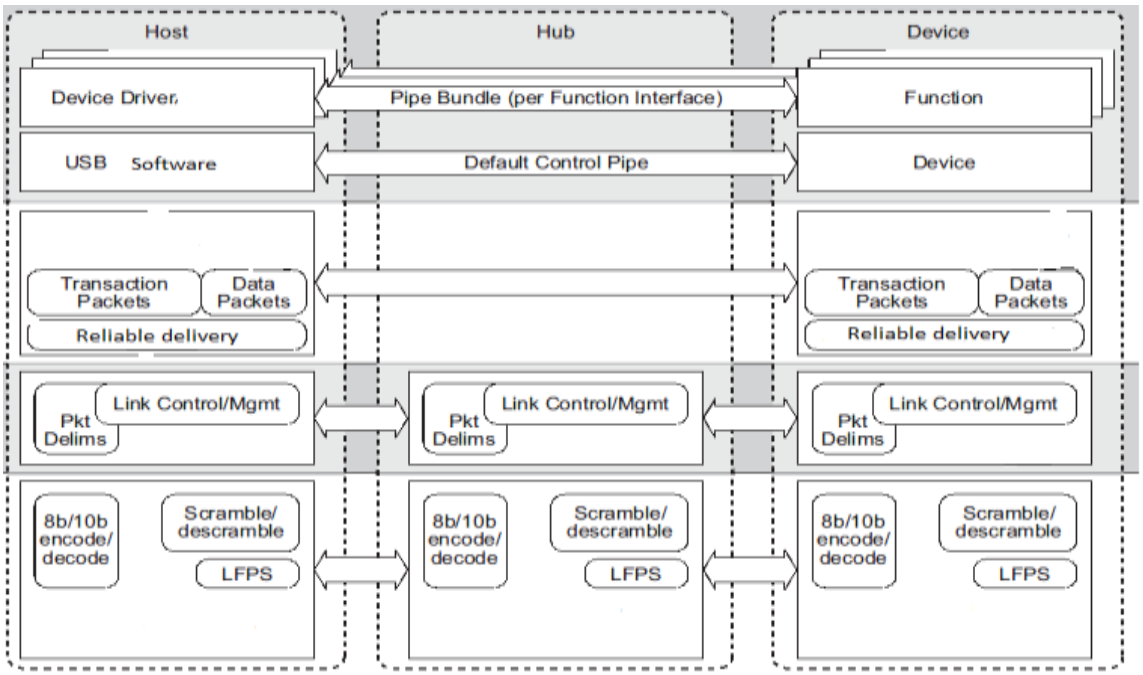
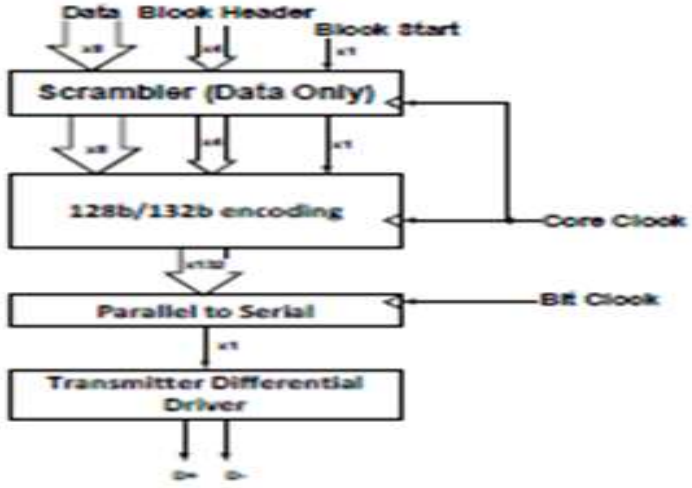


Fig: Super Speed Architecture

One of the major goals of 128b/132b encoding is to embed a clock into the serial bit stream before transmission across the link. This eliminates the need for a high frequency 5.0 GHz clock signal on the link that could generate significant EMI. Every byte to be sent is converted to a 132-bit value, called a symbol. a look-up table associated with the encoder. As the two tables suggest, two types of information are encoded.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

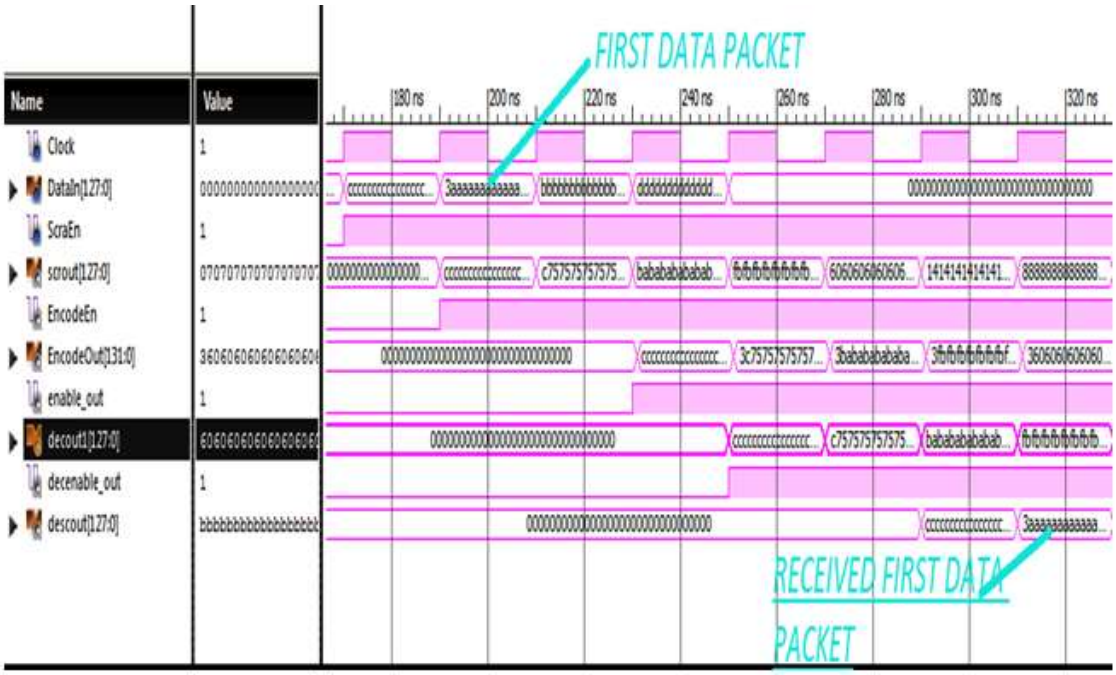


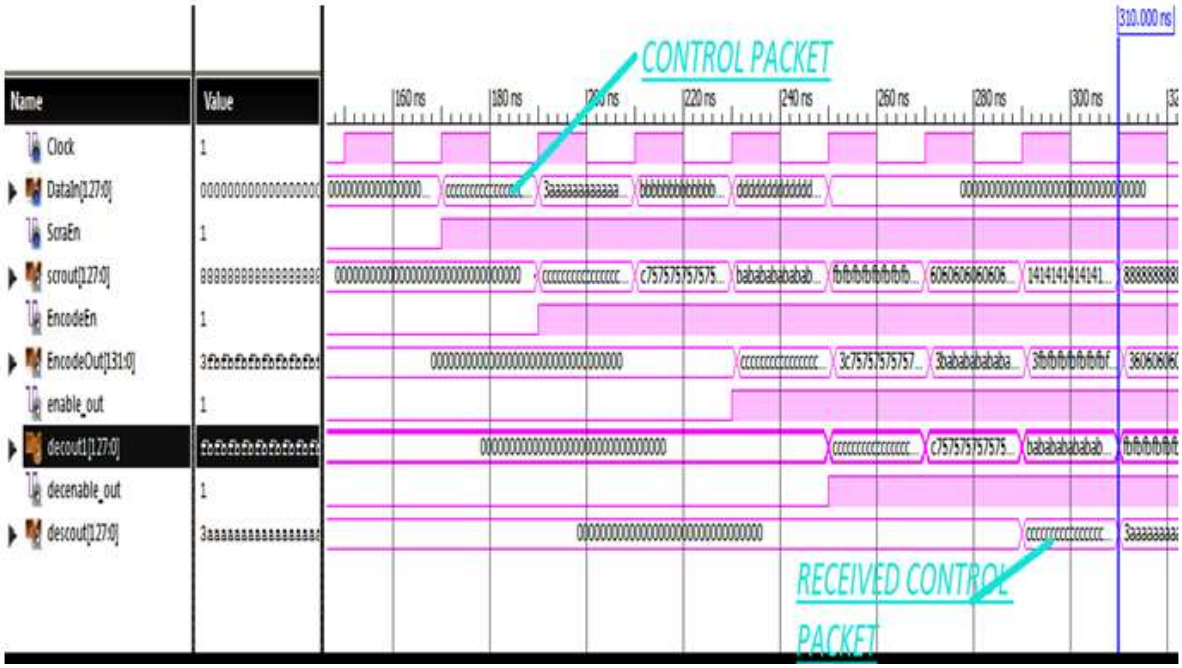
The 128b/132b Decoder uses two look up tables (the D and K tables) to convert the 132-bit symbol stream back into bytes. Each symbol value is submitted to both look up tables but only one of the tables will find a match for the symbol. The state of the D/K# signal indicates that the received symbol. Scrambling reduces repeated patterns in the bit stream and lowers EMI by preventing the concentration of emitted energy at only a few frequencies. Scrambling works by generating a pseudo-random data pattern that is XORed with the outgoing bit stream. The algorithm used for scrambling data is expressed as a polynomial implemented as a linear feedback shift register (LFSR).

Disabling scrambling is intended to help simplify test and debug equipment. Control of the exact data patterns is useful in a test and debug environment. Since scrambling is reset at the physical layer, there is no reasonable way to reliably control the state of the data transitions through software. The Disable Scrambling bit is provided in the training sequence for this purpose. The mechanism(s) and/or interface(s) used to notify the physical layer to disable scrambling is component implementation specific and beyond the scope of this specification.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

Simulation Results :





Conclusion:

In this project, various scenarios including the implementation and the functionality verification of the USB 3.1 GEN2 has been done using Verilog HDL language in Xilinxtool. The Simulated Behavioral model wave form for USB3.1 GEN2 has been obtained. This design is validated in

Xilinx ISIM simulator and synthesized using Xilinx ISE14.5 Design suite. The number of clock cycles required for the transmission of a signal from transmitter to receiver has been calculated and found to be 5. The efficiency is ensured by the accurate results.

References:

[1] A.X.Widmer, P.A.Franaszek, "A DC-Balanced Partitioned Block, 8B/10B Transmission Code," IBM J.RES. DEVELOP Vol.27, No.5, and September 1983.

[2] JagritKathuria, M. Ayoubkhan, Arti Noor, "A Review Of clock Gating Technique," MIT International Journal of Electronics and Communication Engineering, MIT Publications, ISSN 2230-7672, Vol 1, No.2, Aug 2011.

[3] Gajendra Singh Solanki, Rekha Agarwal, Sandhya Sharma, "Power Optimization of High Speed Pipelined 8B/10B encoder," International Journal of Innovative Technology & Exploring Engineering, Vol.3, No.7, December 2013.

[4] Mohammad Maadi, "An 8b/10b Encoding Serializer/Deserializer (SerDes) Circuit For High Speed Communication Application Using a DC Balanced, Partitioned Block, 8B/10B Transmission Code," International Journal of Electronics & Electrical Engineering, Vol.24, No.2, April 2014.