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DESIGN OF SINGLE PRECISION FLOATING POINT ADDER

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Abstract
The electronics industry has grown broadly over the past few decades, largely due to the rapid development of large- scale integration ways and system design usages. With the appearance of Very Large-ScaleI ntegration (VLSI) designs, the VLSI layout design using Complementary Metal Oxide Semiconductor(CMOS) becomes obsolete due to its short channel effects and leakage currents, which causes power dissipation and degrades overall circuit performance. Quantum Dot Cellular Automata (QCA) technology is one of the arising technologies that can be used to replace CMOS technology. Due to its extremely low power consumption, high operating frequency, and small size, it has attracted considerable attention in recentyears. In floating point adder computation results that fall outside of the available precision must be round to a neighbouring number. Because of rounding there will be enhancement in speed and energy consumption. This paper is to design an effective architecture for Floating point adder using QCA technology analysing its performance with respect to power, area, and delay.

Keywords:
QCA, Rounding.

1. INTRODUCTION

A floating-point adder (FPA) takes two figures as an input and calculates their sum. So, in order to perform this addition floating- point calculation is frequently used in systems with very small and very large real figures that claim fast processing times.
The term floating point indicates that a number's radix point(decimal point, or, more generally in computers, binary point) can" float"; that is, it can be placed anywhere relative to the significant integers of the number. This position is determined by the exponent, and therefore the floating- point representation can be supposed of as a form of scientific memorandum which is in a standard form.The speed of floating- point operations is an important specific of a computer system, especially for operations that involve acute mathematical computations.
A Floating-point number has the form
$X = m\beta^e$
Where, e is called exponent, m is mantissa and β is the base of the number system.
The most generally used floating point standard is the IEEE standard. According to this standard, floating point numbers are represented with 32 bits (single precision) or 64 bits(double precision).

1.2 Quantum Dot Cellular Automata (QCA):

Quantum dot cellular automata (QCA) is new nanotechnology which recently has become one of the top emerging technologies. The logic states or values in QCA are demonstrated no longer by voltage levels but rather by the position of electrons. A quantum dot makes this structure by creating a site with a low potential. A QCA cell consists of four or five quantum dots. This technology operates according to the interaction between QCA cells consists of four quantum dots and two mobile electrons. Because of columbic repulsion these electrons, tend to occupy longest distance from each other so, they occupy antipodal dots of cell. Therefore, there are two stable polarizations where

electrons put least energy on each other, those are binary one and zero. A polarized cell forces neighbouring cell into the same polarization because electron static energy in cells should be minimized. Basic elements in QCA such as majority gate, binary wire, inverter gate and other gates can be designed based on columbic interactions among cells. The needed attribute of QCA technology is clocking. Cells can only be in part of 2 states and the tentative alter of assert in a cell is dictated by the assert of its adjacent neighbours. But occasionally, a way to regulate information passage is a need to clarify the direction whereat assert transition occurs in QCA cells. The clocks of a QCA system attend two ambitions powering the automaton, and regulating information passage direction. QCA clocks are areas of conductive fabric below the automaton's lattice, modulating the electron tunnelling barriers in a QCA cells.

2. LITERATURE SURVEY

The literature review on floating point adders reveals that using QCA the power dissipation can be reduced at a advanced percentage compared to CMOS nm technology, due to new design in this paper the vital parameters of any VLSI circuit design, namely power dissipation area and delay have been enhanced significantly. The Quantum dot cellular automata is proposed to overcome the downsides of CMOS circuits at nanoscale.

Hamid Reza Roshany proposed" Novel efficient circuit design for multilayer QCA" using the QCA technology. It shows that the two new multilayer QCA infrastructures have advancements in terms of area, cell count but requires high device viscosity.[3]

Brett Mathis and JamesE. Stine "A Novel Single/ Double Precision Normalized IEEE 754 Floating-Point Adder/ Subtractor. In this paper 32nm CMOS technology and ARM standard- cells is used and design of a completely IEEE 754-compliant FPA creating a high- speed, low- power design is done. It is concluded that the design is useful for any floating- point unit that has a concern for delay optimization but in the case of underflow, the current design generates an exception rather than convert to a renormalized.[4]

"Tunable floating-point Adder" -Alberto Nannarelli, Senior Mentor, IEEE. It addresses the design of and adder in this tunable floating point [TFP] precision. TFP is a variable precision format in which a given precision can be chosen for a single operation by a selecting a specific number of bits for significand and exponent in the floating-point representation. By Tuning the precision of an algorithm to the minimum precision achieving an acceptable target error which makes the computation more power efficient.[6]

"A new floating -point Adder FPGA-based implementation using RN Coding of number" Tulio Aravjo, Matheus B.R Cardoso Eriveltion G, Nepomuceno, Carlos H. Clanos, Javier Arias Garcia. RN [round-to-nearest] has an advantage that rounding to nearest is equivalent to a word truncation. They proposed hardware architectures for binary and floating-point adder analyzing for the latter it's performance interns of error and resource consumption in FPGAs.[7]

3 Proposed Design:

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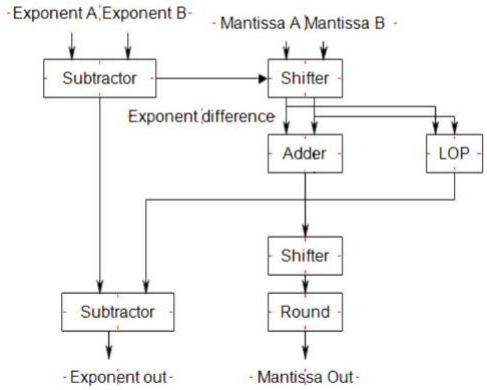

Figure 1: Floating Point Adder

3.1 Description of Block Diagram

In the design of floating-point adder, comparator plays an essential role as a controller. Consider two floating-point numbers, mantissa A and mantissa B. The 'less than' output of the comparator is used to control the shift register to right shift the mantissa of A. Similarly, the 'greater than' output of the comparator is used to manage the shift register to right shift the mantissa of B. If these outputs are high, then there will be a shift in the corresponding mantissa, if and only if there is a mismatch in exponents. When both exponents are equal, there is a logic high signal. on the equal output of the comparator which gives the resultant mantissa.

The layout consists of all the optimized designs of comparator andshift register and adder/subtractor module. All the required modules are designed in QCA to get the optimized architecture. The individual steps are explained in detailed below-

The block diagram of floating-point architecture consists of various modules. Here, we consider two numbers. Exponents of these two numbers are compared. Addition or subtraction operation of the mantissa can be performed only if the exponents are equal. If the exponents of the two numbers are not equal, we need to align them such that they are equal. Generally, the size of the exponent is 8 bit of a single precision number so an optimized novel 8-bit comparator is used to perform the comparison of the exponents. Before going to the shifting operation, we must know the amount of shift. The number of bits to be shifted is equal to the difference of the exponents and thus subtractor module is used. The shift registers used can be used to perform left shift or right shift. The main reason to include this module in the architecture is to shift the mantissa of the numbers when the exponents are not equal. Implementation of the shift registers can be done by using flip flops. Also, D flip flop and a multiplexer can be used which will have a good performance in terms of area and delay.

Perform addition/subtraction depending on the sign bit. Let As and Bs be the sign bits so if A_SB_S=00 it is a positive number if A_SB_S=11 it is a negative number. Now the addition is performed on A_m and B_m.If A_SB_S=01, since one number is negative, subtraction is performed. Subtraction can also be done by taking 2's complement to the negative number. Now the final task is to represent the result in the standard form. For this the decimal value of the result must be adjusted. Here, the exponent can either be incremented or decremented without modifying the original data.

4 Design and Simulation results:

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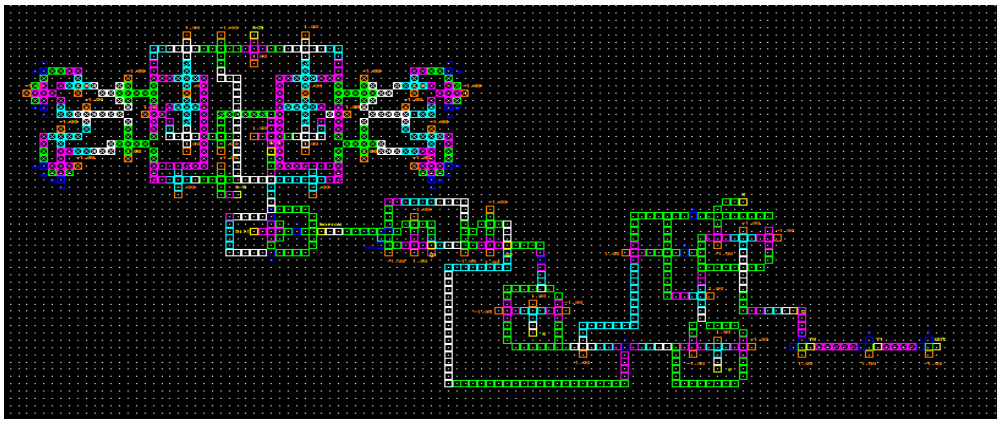

Figure 2: QCAD design of Floating point adder

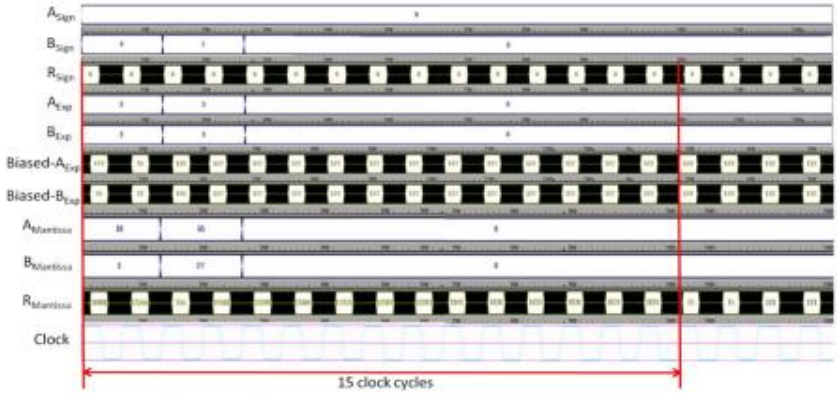

Figure 3: Simulation results of Floating-point adder

CONCLUSION

An efficient method is proposed in this paper to reduce the area, number of cells used, delay and energy dissipation, thereby increasing the computational speed of the floating-point adder. The compared results show that the modified floating-point adder has consumed less energy and area which is a great advantage.

Overall, floating point adder using a quantum dot cellular automata is a promising technology that could have a significant impact on energy consumption, power dissipation, area and delay.

FUTURE SCOPE

Future scope for the design and development of floating-point adder is vastas there is a need for energy efficient devices that occupy smaller area. The design of a floating-point adder using quantum dot cellular automata is a significant step towards more efficient and sustainable energy usage. As energy efficiency continues to be an important factor, the design using technologies like this will be helpful to reduce the energy and area of the circuits.

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