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EFFICIENT DESIGN OF FIR FILTER USING VEDIC SUTRAS

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ABSTRACT
Finite Impulse Response (FIR) filters are most widely used in communication, audio and other signal processing applications. Having a Fast and suitable multiplier in FIR filter plays a major role, as we know that multiplication operation is one of the most important elementary operations, which finds its place in the implementation of various algorithms in many applications. In present days, the demand for faster and power efficient algorithms has been increased the need for faster and power efficient multipliers, since multiplication is used more frequently. The multiplication method proposed ancient Indian texts known as Vedas. Vedic multiplier which is derived using different Vedic sutras, which helps in efficient multiplications. This work combines mainly two sutras namely Urdhvatiryagbhyam, Nikhilam along with Karatsuba algorithms to form Hybrid multiplier to carry out multiplications .

INTRODUCTION
FIR (finite impulse response) filters are generally chosen for applications where linear phase is important and a decent amount of memory and computational performance are available. They have a widely deployed in audio and biomedical signal enhancement applications [1]. In other applications, the FIR filter circuit must act as a low power circuit that operates at moderate sample rates [2]. The structure of the multiplier circuit also affects the resultant power consumption and speed. Choosing multipliers with more hardware breadth rather than depth would not only reduce the delay, but also the total power consumption.

LITERATURE SURVEY
[1]A Low power and low area VLSI implementation of Vedic design FIR filter for ECG signal de-noising was presented by MSumalatha etal.,(2019).In this paper,Vedic design-carry look ahead Adder FIR filter is designed using Urdhva Tiryagbhyam sutra. Significance of multiplier in FIRfilter is much more improved by using Vedic multiplier. The sutra used in this paper is Urdhva Tiryagbhyam,which works based on "vertically and crosswise" approach. In PE, Vedic multiplier is used to perform the multiplication operation which helps to reduce the hardware utilization. The optimal CLA adder is also used to perform the FIR filter. Finally, the process speed and area are improved in this method. But the design becomes more complex as the size of the numbers to be multiplied increases.
[5]Design and Evaluation of a FIR Filter Using Hybrid Adders and Vedic Multipliers was proposedbyJuthiFarhanaSayedetal.,(2021)[5].HereauthordesignedFIRfilterusingaVedic multiplier,overall power consumption is reduced using this design, yet it is observed that FIR filter is lessreliable anddesignlayoutis complex.
[6]A Modified Binary Multiplier Circuit Based on Vedic Mathematics was presented by Shamim Akhteretal.,(2019).In this paper,an efficient novel technique is presented for binary multiplier circuits based on Vedic mathematics. It is proved from the synthesis results that the proposed technique is much efficient in terms of delay and LUT requirements. The proposed technique can be extended for a larger bit size. But Performance of multiplication can be improved in terms of speed.
[7]Design and performance comparison of adiabatic 8-bit multiplier was proposed by H.V. RavishAradhya et al.,(2016). In this work, Vedic-Dadda hybrid multiplier, which replaces Wallace

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compression with Vedic multiplier dissipates lesser power, compared to Wallace-Dadda hybrid multiplier. 8-bit Vedic multiplier proves to be an optimized design with respect to power, delay, and area for 8-bit multiplication.

In this Literature survey, we have encountered Various approaches that are utilized by researchers to apply these Vedic sutras, and algorithms. Yet, they have failed to overcome few drawbacks due to applying only one sutra which is not flexible to all size of multiplicands, which can achieved by using alternative efficient multiplier using Vedic sutras employed at different levels of the designs.

PROPOSED DESIGN

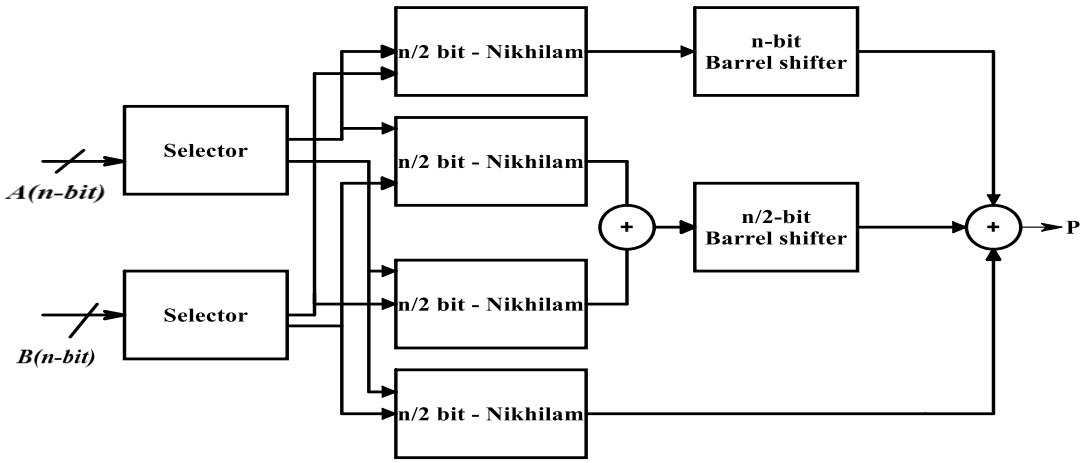

Fig 1: Hybrid Multiplier Using Nikhilam Sutra

The Proposed block diagram is designed using the following algorithm, in order to select the bits selectors are used and to shift the bits n-bit and n/2-bit Barrel shifters are used in the design of Hybrid multipliers

$$P = 2^{n}(A_H B_H)+2^{n/2}(A_H B_L+A_L B_H) +A_L B_L$$

4 RESULTS AND DISCUSSIONS

The proposed design is simulated in Xilinx Vivado 2018.1

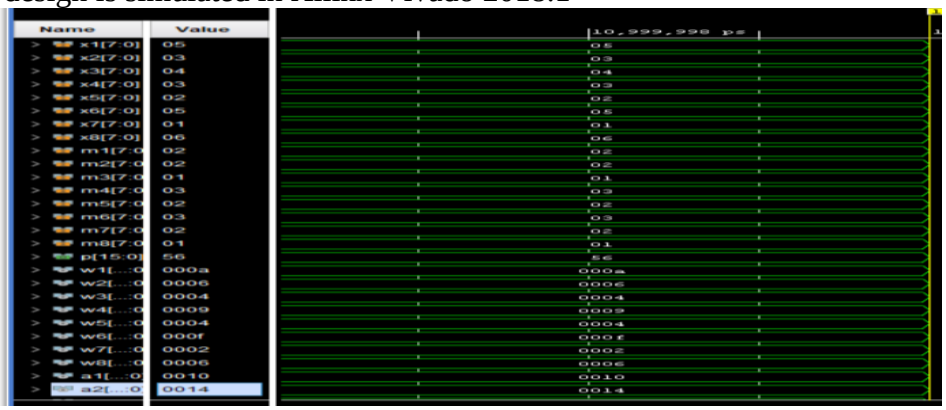

Fig 2: Simulation results of proposed design

The simulation results of proposed designs are compared with the previous designs in the following table

Table 1: Comparison of different FIR Filter designs

FIR Filter Design	Power(mW)	Area (No of LUT'S)	Delay(nS)
UT	22.636	876	32.867
NIK	36.615	878	28.873
KARAT	25.547	675	25.678
Prop_NIK	28.657	567	26.768

We can observe the performance in the Proposed designs have been improved compared to the existing designs .The power consumption in Proposed design is reduced with minimum reduction in area with moderate delay.

CONCLUSION:

In conclusion, the performance of FIR filters can be enhanced using the Urdhva Tiryakgbhyam sutra, Nikhilam sutra and Karatsuba algorithm. The computational complexity of the filter can be made simpler through calculation process optimization, resulting in quicker execution times and less resource usage. Urdhva Tiryakgbhyam multiplier is used at the lowest level Nikhilam multipliers used as a building -blocks, which are combined together using the Karatsuba algorithm and this is being proposed as Hybrid multiplier gives better results compared to the existing one. Using Vedic multiplier in FIR filter improves the performance in terms of area, delay and power consumption. The Proposed hybrid Vedic multiplier using above sutras helps to improve overall performance of FIR filter, with moderate delay and reduced area. Hence, the proposed hybrid multiplier combines the advantages of all algorithms.

FUTURE SCOPE:

Here we have done our work with considered sutras from the literature survey, and we can also study more in the area. The hybrid multipliers can be modified by replacing any proposed multiplier block in the design in order to further improve the performance and to reduce the complexity of the design .

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