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DESIGN AND PERFORMANCE ANALYSIS OF SRAM CELLS USING CNTFET TECHNOLOGY

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ABSTRACT
In the memory design, the primary goal is to create a memory cell that exhibits high data stability and consumes low power in the deep nano scale range. However, the use of MOSFETs in implementing VLSI circuits faces certain constraints, such as leakage power and second order effect caused by variations in parameters such as process, voltage, and temperature (PVT). To overcome these limitations, a promising alternative is Carbon Nano Tube Field Effect Transistor (CNTFET), where the conventional MOSFET's channel is replaced by a Carbon Nano Tube (CNT). In this paper, performance analysis of different CNTFET SRAM cells will be done. The write delay, read delay and power consumption are analyzed and compared for different CNTFET SRAM cells using HSPICE simulation tool.

1. INTRODUCTION
In the world of computing, Static Random Access Memory (SRAM) is an essential building block that requires a considerable amount of area and power consumption. To cater to the needs of portable devices like smart phones, biomedical devices and wireless sensor networks that require stable designs with low power, the development of low power SRAM is crucial. FPGA devices that facilitate implementation of digital systems relay on SRAM for storage purposes. Therefore, optimizing SRAM cells in aspects such as leakage power and speed can further enhance the overall efficiency of FPGA devices.
The incorporation of CNTs into the transistor structure, CNTFETs have shown remarkable performance advantages such as low leakage power, high switching speed, and excellent electrostatic control. Therefore, CNTFETs are considered as speed, and excellent electro static control. Therefore, CNTFETs are considered as a potential replacement for conventional MOSFETs in advanced VLSI circuits.
The characteristics of size reduction in CMOS technology will gives the short channel effects, stability of data storage and leakage currents. The strength of this leakage current is dependent on many factors like supply voltage, temperature and threshold voltage. Leakage currents which leads to the functionality and stability of the SRAM cell that occurs with the scaling down technology, Which includes different leakage reduction technique like body biasing, power gating and Stability of the data is defined from the Static Noise Margin(SNM) of the circuit.

2. LITERATURE SURVEY
[1] Zubair Ahmed, "Modelling CNTFET performance variation due to Spatial Distribution of Carbon Nanotubes" In this paper, the authors propose a methodology to account for the spatial distribution variability of Carbon nanotube field-effect transistors(CNTFETs) in order to calculate the mean and statistical distribution of their current. Overall, this methodology improves our understanding of CNTFET performance and can aid in the design and optimization of CNTFET circuits.
[2] Arushi Shrivastava, Parul Damahe, Vijay Rao Kumbhare, Manoj kumar Majumder "Designing SRAM using CMOS and CNTFET at 32nm Technology" The research demonstrated that CNTFET

based SRAM memory cells have inherent characteristics such as drive current, immunity to short channel effect, and good gate controllability, which make them perform better than CMOS based cells. These characteristics enable CNTFET based cells to consume less power and operate with lower delay.

[3] Robert Giterman, Osnat Keren, and Alexender Fish "A7T Security Oriented Cell" The implementation of the proposed 7T SRAM cell is based on a 28nm technology. In this paper, the proposed modified 7T SRAM cell is designed to address the information leakage issue during write operations in conventional 6T SRAM cells. The modified 7T SRAM cell employs a two-phase write operation that includes an equalization phase and a write phase. This is a promising approach to improve the security of SRAM cells and protect sensitive data stored in memory.

[4] Robert Giterman, Maoz Vicentowski, Itamar Levi, Yoav Weizman, Osnat Keren and Alexander Fish"Leakage Power Attack-Resilient Symmetrical 8T SRAM cell" Leakage power attacks can exploit the correlation between the stored data and the power consumption of the SRAM cell to extract sensitive information. To, address this issue, the proposed solution is an 8T SRAM cell, which incorporate additional transistors and a two-phase write operation to reduce the correlation between the stored data and the leakage power dissipation.

[5] P Sandeep, P.A Harsha Vardhini, V Prakasam "SRAM Utilization and Power Consumption Analysis for Low Power Applications" The design of SRAM cell architecture is focused on achieving low power consumption for high-speed applications. To achieve this goal, various architectures are reviewed and compared using different techniques, leading to an optimized solution for low-power SRAM cell design. The analysis of current and power components of these SRAM designs helps in identifying an optimized architecture. By incorporating specialized techniques suggested by the designers, an optimized low-power SRAM architecture can be designed.

3. SRAM CELLS:

3.1 6T CNTFET SRAM CELL:

The 6 Transistor (6T) SRAM cell is shown in Fig.1(a) uses one access transistor and one cut-off transistor. This design helps in high stability and low leakage power at a size of 32nm and it has good tolerance to static noises under read operation. The word line (WL) is a control signal that selects a particular SRAM cell for reador write operation.

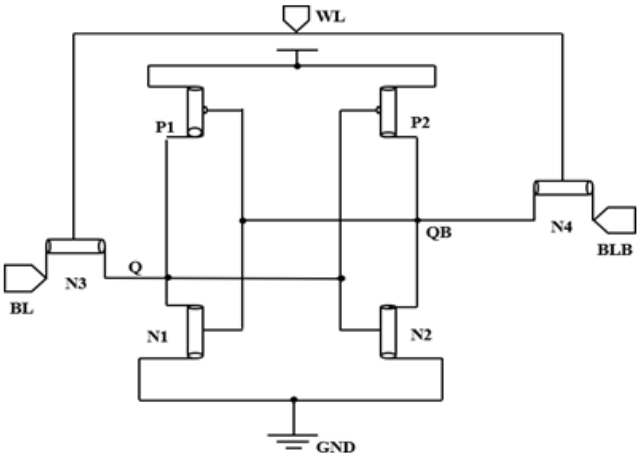

Fig1 (a): 6T CNTFET SRAM CELL

3.1.1 Write Operation:

When WL is high, the access transistors N3 and N4 are turned 'ON', connecting the storage nodes Q and QB to the bit lines BL and BLB respectively. To write a logic 1 into the storage node Q, the BL is pre charged tologic1and BLB is pre charged to logic 0.Then a write pulse is applied to WL, which turns on the transistor

N3 and N4, allowing the stored value of the bit line (BL) to be written into the storage node Q. Similarly in order to write logic 1 into the storage node QB, the BLB is pre charged to logic 1 and BL is pre charged to logic 0.So, write 1 operation is performed by the storage node QB.

3.1.2 Read Operation:

The read operation is started by asserting the word line (WL) enabling both the access transistors N3 and N4.The second step occurs when the value stored in 'Q' and 'QB' are transferred to the bit lines 'BL' and 'BLB' through N1 and N4. On the BL side, the transistors N2 and N3 pull the bitline towards Vdd (When"1" is stored at Q). If the content of the memory is 0, the reverse would happen and 'BLB' would be pulled towards 1 and'BL'towards0.

3.1.3 Hold Operation:

This mode of operation is also known as Standby Mode. The WL is kept to below (logic 0). The storage nodes are disconnected from the bitlines and the data in the storage nodes are kept as they are.

3.2 8T CNTFET SRAM CELL:

The 8T SRAM cell is shown in Fig.1(b) uses a decoupled read port in order to enhance the stability in the read operation and it also uses different word lines and bit lines for read and write cycles. The 8T SRAM provided significantly improved RSNM which is similar to the HSNM of the 6T SRAM cell.

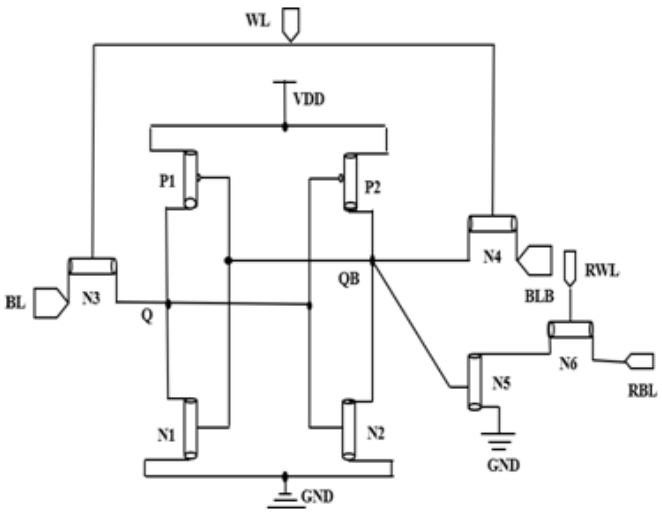

Fig1(b): 8T CNTFET SRAM CELL

3.2.1 Write Operation:

During the write operations the read ports RBL and RWL are kept low. When WL is kept high, the access transistors N3 and N4 are turned ON, connecting the storage nodes Q and QB to the bit lines BL and BLB respectively. To write a logic1 into the storage node Q, the BL is pre charged to logic1 and BLB is pre charged to logic 0. Then a write pulse is applied to WL, which turns on the transistor N3 and N4, allowing the stored value of the bitline BL to be written into the storage node Q. Similarly in order to write logic1 into the storage node QB, the BLB is pre charged to logic1 and BL is pre charged to logic0. So, write1operation is observed at storage node QB.

3.2.2 Read operation:

The read operation is performed using the transistors N5 and N6. During the read operation, WL is kept to below, RWL is set to high. This, in turn, switches 'ON' transistor N6 and RBL is pre charged to VDD. If the datain Q is '1', this in turn switches 'ON' transistor N5 and RBL value is discharged through N5 and N6. If the data in Q is'0',the RBLvalue is maintained as it is.

3.2.3 Hold Operation:

During the hold operation the WL, RWL and RBL are kept to below. The storage nodes are

disconnected from the bitlines and the data in the storage nodes are kept as they are.

3.3 10T CNTFET SRAM CELL:

The 10T SRAM cell is shown in Fig.1(c). The 10T CNTFET SRAM cell is a key building block of modern digital circuits, providing past and reliable storage of binary data [8]. To read the stored value, a fully differential read sensing method is employed, which improves theread stability of the memory cell.

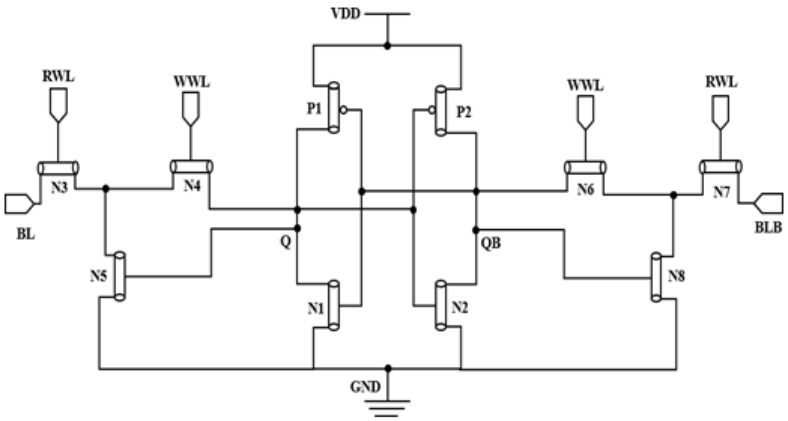

Fig1(c):10T CNTFET SRAM CELL

3.3.1 Write Operation:

During the write operation, the value which we are storing will be kept in BL and its complement is stored in BLB. The WWL and RWL are kept to be high which turns ON the transistors N3, N4, N6, N7. The values are transferred to the storage nodes Q and QB through BL and BLB.

3.3.2 Read Operation:

During the Read Operation, the wordline(WWL) is kept low. As it is kept to below the transistors N4 and N6 will be turned 'OFF'. The storage nodes Q and QB will be decoupled from the bitlines. Before performing theread operation, the BL and BLB were pre charged to V_{DD} for some time. When RWL is raised to high, thetransistors N3 and N7 re turned 'ON'. Based on the values in the storage nodes the transistors N5 and N8 are turned 'ON'. This makes any one of the bit-line to maintain the same potential and the other bit line is discharged through 'ON' transistor. By using the sense amplifier, the potential difference between bit lines is sensed. So, the resultant stored value is obtained from the output of the sense amplifier.

3.3.3 Hold Operation:

During the Hold Operation, WWL and RWL are kept be low. This in turn switches 'OFF, the transistors N3,N4, N6 and N7. Hence the storage nodes are disconnected from the bit lines, the data stored in the storage nodes are kept as they are.

4. RESULTS AND DISCUSSIONS

4.1 Write Delay (nsec)

The delay observed during the write operation of the SRAM cell is defined as the write Delay. The time difference between the WL (50%) and the Q (90%) is considered as the write '1' delay. The time difference between the WL (50%) and the Q (10%) is considered as the write '0' delay. The write delay is calculated for6T, 8T and 10T CNTFET SRAM cells.

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	V_{dd}(V)	
SRAM cells	**0.9V**	**1.0V**
6T	0.31	0.29
8T	0.27	0.22
10T	0.33	0.2

Table1.Write‘1’Delay (nsec) of different SRAM cells

	0.9V	**1.0V**
6T	0.37	0.33
8T	0.43	0.40
10T	0.18	0.29

Table2.Write‘0’Delay (nsec) of different SRAM cells

4.2 Write Power (µw)

The power consumed by the SRAM cell during the write operation is termed as the write power.The write power is calculated for different CNTFET SRAM cells.

	0.9V	**1.0V**
6T	29.27	39.91
8T	0.98	0.95
10T	5.89	9.43

Table 3. Write‘1’ power(µw) of different SRAM cells

	0.9V	**1.0V**
6T	13.86	19.79
8T	8.13	8.38
10T	19.45	21.23

Table 4. Write‘0’ power(µw) of different SRAM cells

4.3 Read Delay (nsec)

The time observed at 50% of the WL is considered as T_1.A 50mv difference is maintained at BL and BLB and the time at that point of BL is taken as T_2. The difference between T_1 and T_2 is calculated as read delay.The read delay for different SRAM cells is shown below.

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	0.9V	1.0V
6T	0.19	0.16
8T	0.31	0.24
10T	0.27	0.22

Table 5. Read '0' Delay (nsec) of different SRAM cells

4.4 Read Power (µw)

The read power for different SRAM cells is observed as below.

	0.9V	1.0V
6T	0.22	0.30
8T	0.16	0.22
10T	0.21	0.29

Table 6. Read '0' Power (µw) of different SRAM cells

CONCLUSION

In this paper, the performance analysis of different CNTFET SRAM cells like 6T, 8T and 10T CNTFET has been done. The result as shows that the 8T CNTFET SRAM cell has less delay during write '1' operation, while 10T as less delay during write '0' operation. 8T CNTFET SRAM cell consumes less power as compared with conventional 6T and 10T CNTFET SRAM cells during write and read operation. During read operation, 6TSRAM cell offer less delay during read '0' operation. Here, read stability of 8T SRAM cell is improved by using different paths for reading and writing. The 8T CNTFET SRAM cell offers excellent power performance than the conventional 6T and 10T CNTFET SRAM cells.

FUTURE SCOPE

The smaller size of CNTFETs allow for a higher density of transistors, leading to higher memory density transistors, leading to higher density capacity. Their potential for future applications, such as neuromorphic computing and quantum computing, further highlights their superiority over other SRAM cell options. A 9T CNTFET SRAM can be implemented using a feedback loop cutting method.

REFERENCES

1. Z. Ahmed, L. Zhang, K. Sarfraz and M. Chan, "Modelling CNTFET Performance Variation Due to Spatial Distribution of Carbon Nano tube",2016IEEE Transaction on Electronic Devices, vol.63, no.9,pp.3776-3781,Sept.2016
2. A. Shrivastava, P.Damahe, V. R. Kumbhare and M. K. Majumder, "Designing SRAM Using CMOS andCNTFET at32 nm Technology",2019IEEEInternational Symposium on Smart Electric System(ISES)(FormerlyiNiS),Rourkela,India,2019,pp.284-287
3. R.Giterman, O.KerenandA.Fish,"A7TSecurityOrientedSRAMBitcell,"inIEETransactiononCircuitsandSystemsll:ExpressBriefs,vol.66,no.8,pp.1396-1400,Aug.2019
4. R. Giterman, M. Vicentowski, I.Levi, Y. Weizman, O.Keren and A.Fish, "Leakage Power Attack -

ResilientSymmetrical8TSRAMCell,"
inIEEETransactiononVeryLargeScaleIntegration(VLSI)Systems,vol.26,no.10,pp.2180,oct.2018
5. PSandeep,P.AHarshaVardhini,VPrakasam"SRAMUtilizationandPowerConsumptionAnalysisforLowPowerApplications"2020InternationalconferenceonRecentTrendsonElectronics,Information,Communication&Technology(RTEICT),2020,pp.227-231
6. Young Bok Kim, Yong-Bin Kim, Fabrizio Lombardi and young Jun Lee, "A low Power 8T SRAM cellDesigntechniqueforCNTFET,"2008InternationalSoCDesignConference,Busan,Korea(South),2008,pp.l-176-l-179
7. S.B.RamakrishnaandA.R.Aswatha,"DevicecharacterizationandimpactofCNTdiameter variationontheread write stability of CNTFET 6T SRAM cell," 2017 International Conference on Innovative MechanismsforIndustryApplication(ICIMIA),Bengaluru,India,2017,pp.561-566
8. Krishnaiah RV, Anil T, Rao ML, Nalajala P, Ahammad SH. Implementation of logic gates using CNFET for energy constraint applications. International Journal of Engineering & Technology. 2018;7(1.1):355-9.
9. M Elangovan, k Gunavathi, "High stable and low power 10T CNTFET SRAM cell" J CIRCUIT SYSTCOMPfromwww.worldscientific.combyuniversityof newEngland.