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DESIGN OF RIPPLE CARRY ADDER USING HIGH-SPEED HYBRID LOGIC FULL ADDER

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ABSTRACT
As the technology in growing immensely in recent years, certain improvisation needs to be made. People are using electronic equipment such as mobile phones, laptops, etc., are playing very important role in our lives. for the better use of these electronic systems, designer search for minute size, high speed and energy efficient circuits. Adder is the most important component in the computing devices. improving the performance of Adders improves the performance of the total system for significantly. By using hybrid XOR-XNOR circuits full adder is designed with high performance, low power consumption and high speed. By using pass transistor an inherent voltage drop problem may occur. To overcome this, transmission gates is used to designfull adder, but transmission gates have low performance. The working of this circuit can be improved using buffer at the output. In the considered base paper hybrid design style is used whose performance and speed is highly depends on XOR-XNOR circuit. The efficiency of the designed circuit in the base paper will be measured by simulating in the LTspice tool. using 45 nano meter complimentary MOS technology. The XOR-XNOR circuit designed uses very few of transistors compared to other reference papers and a full voltage swing is also provided.

Keywords: Pass transistor logic, Hybrid logic design, Transistor gate

1. LITERTURE SURVEY
[1] Gianluca Giustolisi, Gaetano Palumbo-Analysis and Comparison in the Energy-Delay space of Nanometer CMOS one-bit Full adders, the transistor count increases hence speed decreases and high propagation delay.
[2] Hamed Naseri, Timarchi – Low Power and Fast Full adder by Exploring new XOR and XNOR gates, the circuit requires and external inverter and due to external inverter it increases power consumption.
[3] Majid amini Valashani, Sattar Mirzakuchaki, A Novel Fast, Low Power and High performance XOR- XNOR cell, In this power dissipation is more.
[4] Mayur Agarwal, Neha Agarwal, Md. Anis Alam – A new Design of Low Power High Speed Hybrid CMOS Full adder, They lack driving capability.

2. INTRODUCTION
A full adder is a digital circuit that performs the arithmetic operation of addition, including the carry from onedigit to the next. It is usually used in combination with other circuits to create more complex logic functions such as subtractors, multipliers, and dividers. The full adder can be constructed using two half-adders and an OR gate. Full adders are capable of adding two single bit binary numbers and a carry bit, making them more versatile than half adders. Full adders can be cascaded together to create circuits that can add multiple bits at once. Full adders are more efficient than using multiple half adders in a row to achieve the same result. A ripple carry is a digital circuit that adds two binary numbers by cascading full adders, with the carry output from each stage being connected to the carry input of the next stage. the circuit gets its name from the ripple effect of the carry output signal propagating through the stages. A high- speed hybrid-logic is a type of full adder circuit that combines both static and

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dynamic logic styles to achieve faster operation while maintaining low power consumption. It consists of a static portion that performs the bulk of the computation and a dynamic portion that generates the final sum and carry outputs.

EXOR/EXNOR Gate using 10 transistors:

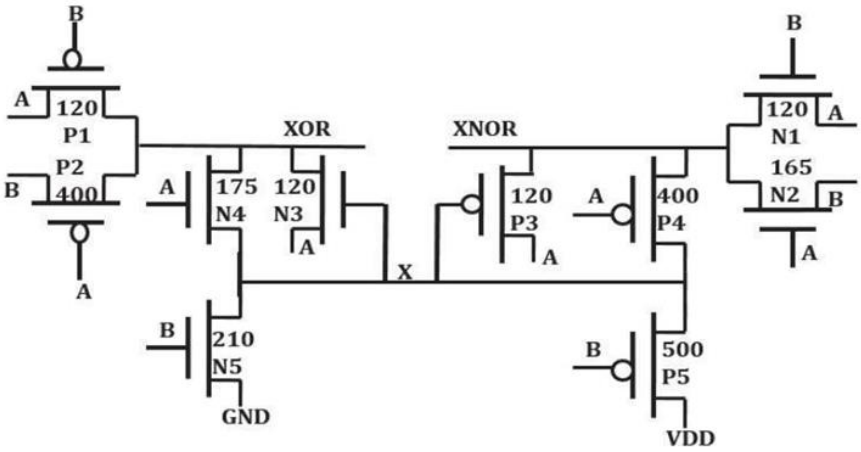

Fig.1 Schematic diagram of 10T-EXOR-EXNOR gate circuit

The EXOR/EXNOR circuit have the 10 transistors. This 10 transistors circuit uses the CMOS logic. The circuitis having 5 PMOS and 5 NMOS transistors. When logic 0 is applied as the input to both the transistors the PMOS transistor will ON and the NMOS transistor will OFF. And the other case is that when the input appliedis logic 1 then the PMOS transistor will OFF and the NMOS transistor will ON. First the two AND gates are connected and then the output of this is given as the input to the OR gate from this we get the EXOR output, for this CMOS Inverter is given then the EXNOR output will come. The main disadvantage of this circuit is the more number of transistors are used having the more area. Now the simplified circuit of EXOR/EXNOR gate with less number of transistors are designed.

EXOR/EXNOR[6] Gate:

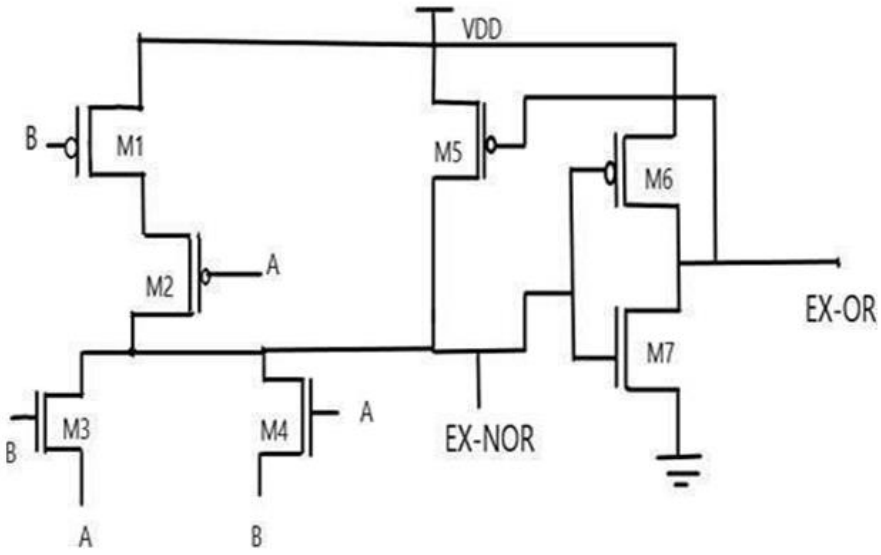

Fig.2 Schematic diagram of EXOR-EXNOR [6] gate circuit

The EXOR/EXNOR circuit contains four PMOS transistors and three NMOS transistors. When logic 0 is usedas an input, the PMOS transistors are turned on and the NMOS transistors are turned off. When logic-1 is usedas an input, the PMOS transistors are turned off and the NMOS transistors are turned

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on. When the input operands are (0,0), the transistor M5 is used to obtain full output voltage swing (1,1). The termination and comparison bits are provided by the outputs of the EXOR/EXNOR circuits.

EXOR/EXNOR[7] Gate:

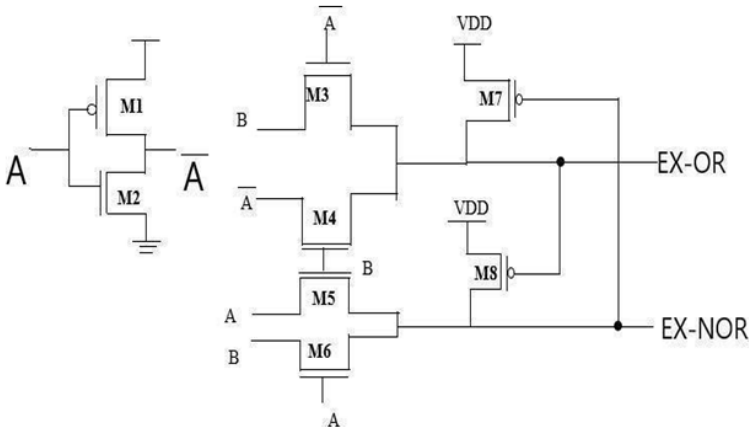

Fig.3 Schematic diagram of EXOR-EXNOR [7] gate circuit

The EXOR/EXNOR circuit is made up of eight transistors. The pass transistor logic and the CMOS logic wereused in this 8 transistor EXOR/EXNOR circuit. The pass transistor logic is used in the circuits M3,M4,M5, and M6. Three PMOS transistors and five NMOS transistors are used in the EXOR/EXNOR circuit. When logic-0 is used as an input, the PMOS transistors are turned on and the NMOS transistors are turned off. Whenlogic-1 is applied as an input, the PMOS transistors are turned off and the NMOS transistors are turned on.

EXOR/EXNOR[8] Gate:

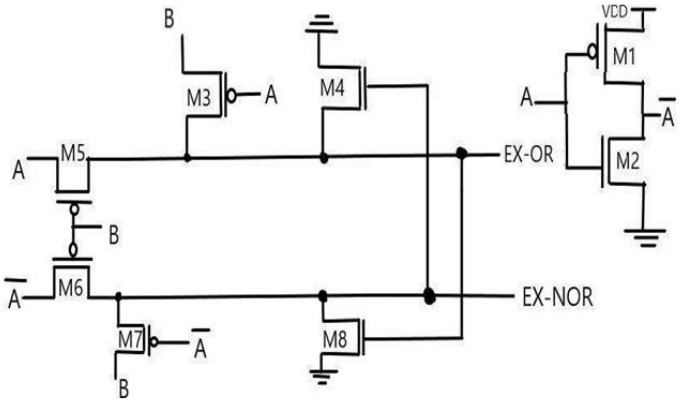

Fig .4 Schematic diagram of EXOR-EXNOR [8] gate circuit

The EXOR/EXNOR circuit is made up of eight transistors. The pass transistor logic and the CMOS logic wereused in this 8 transistor EXOR/EXNOR circuit. The pass transistor logic is used in the 17 circuits M5 and M6.The EXOR/EXNOR circuit contains 5 PMOS and 3 NMOS transistors. When logic-0 is used as an input, thePMOS transistors are turned on and the NMOS transistors are turned off. When logic-1 is applied as an input,the PMOS transistors are turned off and the NMOS transistors are turned on.

3. CIRCUIT DIAGRAM OF SUM MODULE:

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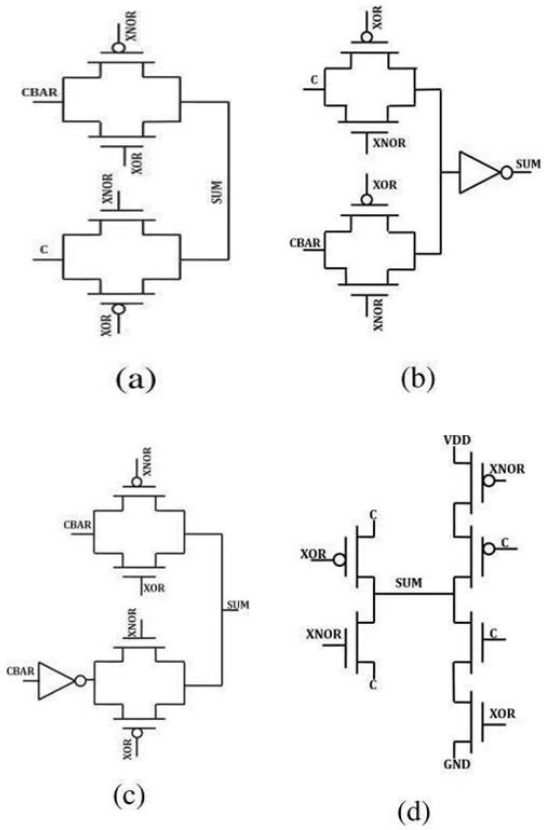

Fig 5. Schematic diagram of Sum Modules

There are four different designs of Module II as shown in the figure. The SUM circuit, shown is implemented using TG as 2 to 1 multiplexer and employed using four transistors. In this circuit, XOR and XNOR signals are used as the inputs to the gate and CIN and CIN are used as the input to the sources of two TGs. This circuit provides low power consumption and high speed with full output swing. However, this circuit has a driving capability problem due to the creation of parasitic capacitance and resistance during fabrication and provide the worst performance in the cascading systems.

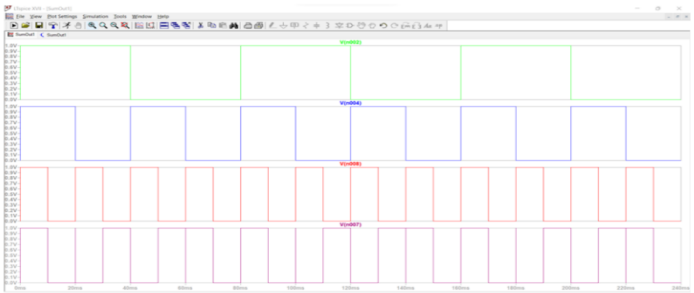

Fig 6. Waveform of Sum Module III

Circuit description of the Carry Module

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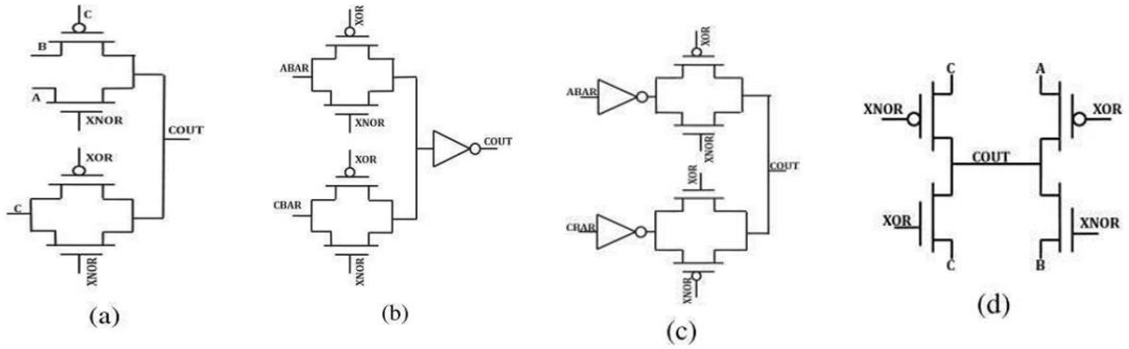

Fig 7. Waveform of Carry Module

Module II is available in four different designs, as illustrated in the figure. The SUM circuit shown is implemented with TG as a 2 to 1 multiplexer and four transistors. In this circuit, the inputs to the gate are XOR and XNOR signals, and the inputs to the sources of two TGS are CIN and CIN. This circuit has a lowpower consumption, high speed, and full output swing. However, due to the creation of parasitic capacitanceand resistance during fabrication, this circuit has a driving capability problem and provides the worst performance in cascading systems.

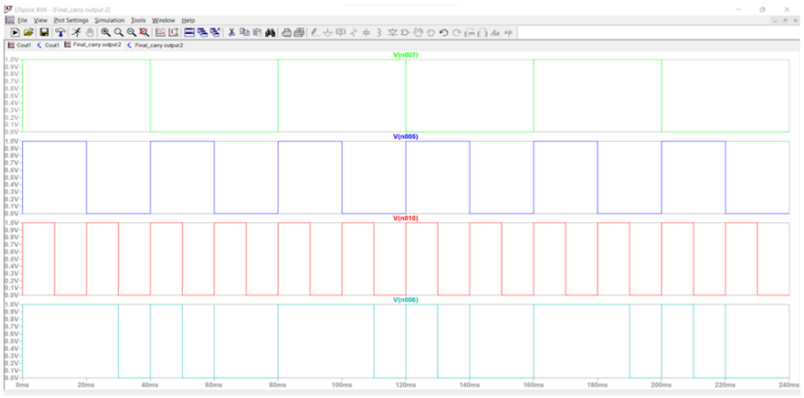

Fig 8. Waveform of Carry Module III

1-bit Full Adder:

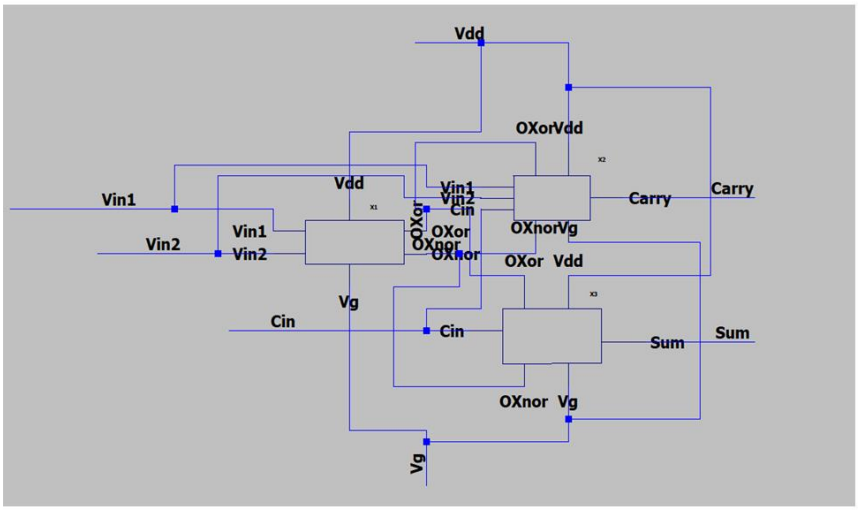

Fig 9. Design of 1-Bit Full Adder

4-bit Full Adder:

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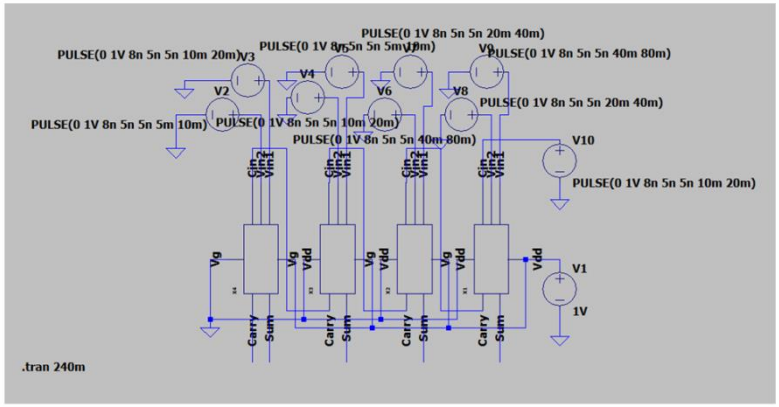

Fig 10. Design of 4-Bit Full Adder

8-bit Full Adder:

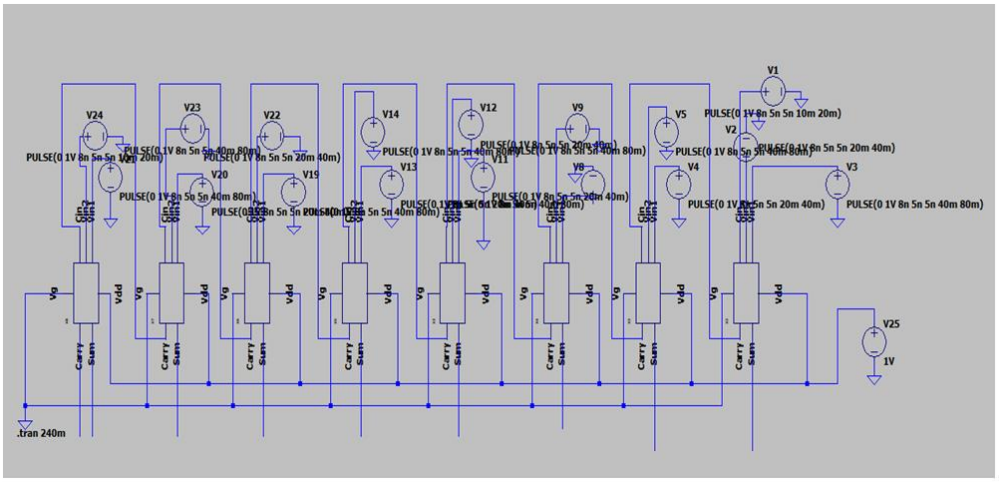

Fig 11. Design of 8-Bit Full Adder

Waveform of 1-Bit Full Adder

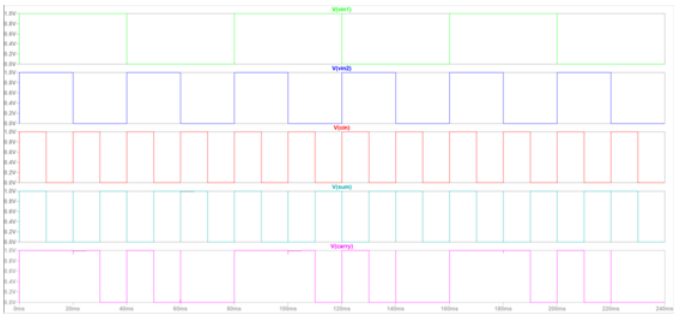

Fig 12. Output of 1-bit Full Adder

Waveform of 4-Bit Full Adder

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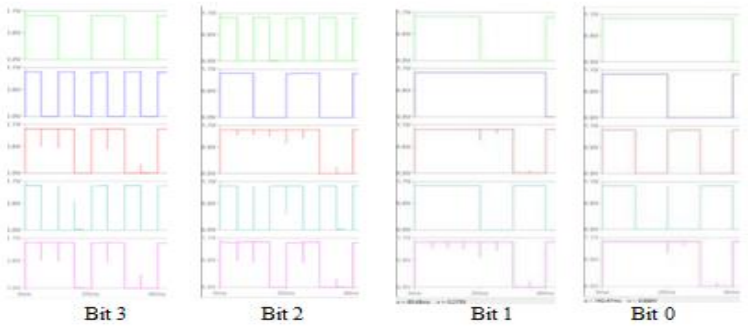

Fig 13. 4-bit Full Adder Output

Waveform of 8-Bit Full Adder:

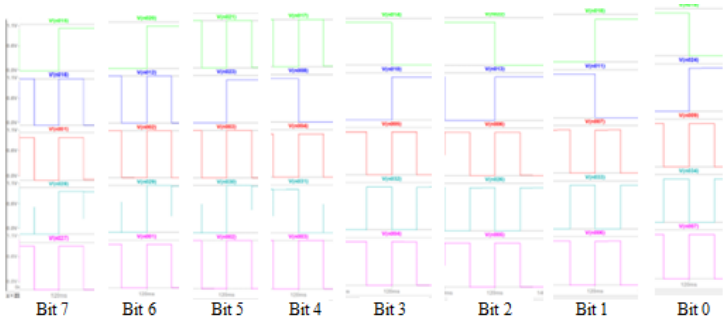

Fig 14. 8-bit Full Adder Output

4. RESULTS

Number of bits	Types of EX-OR Gates	Techno -logy	Number of Transistors	Supply Voltage (V)	Delay(ns)	Power Dissipated(pW)
4-bit	10T EXOR / EXNOR	45nm	80	1.2	2.67	120.31
	EXOR/EXNOR [1]	45nm	68	1.2	**1.33**	73.94
	EXOR/EXNOR [2]	45nm	72	1.2	236.3	97.174
	EXOR/EXNOR [3]	45nm	72	1.2	239.6	**67.34**
8-bit	10T EXOR/ EXNR	45nm	160	1.2	2.26	240.62
	EXOR/EXNOR [1]	45nm	136	1.2	**0.396**	**146.74**
	EXOR/EXNOR [2]	45nm	144	1.2	100.5	194.34
	EXOR/EXNOR [3]	45nm	144	1.2	86.81	194.15

From the above comparison table the comparison is for various EXOR/EXNOR gates is as like number of transistors, theoretical delay and power. In the above comparison we are using different logic gates such as 10T EXOR/EXNOR gate, EXOR/EXNOR [6], EXOR/EXNOR [7], EXOR/EXNOR [8]. If the number of
transistors are increased then the design of the circuit will become complex. The value of the Delay becoming more when the number of transistors are increased, for the propagation delay term the

operation is based onthe number of the transistors. The above comparison is for the EXOR/EXNOR circuits which are placed in the place of the 10T EXOR/EXNOR circuit in the 4-bit and 8-bit full adder.

5. CONCLUSION

Implementation of 4-bit and 8-bit ripple carry adders with Four different EXOR/EXNOR gates in LT spice software namely 10T EXOR gate, EXOR [6], EXOR [7], EXOR [8] gate is done. The simulation results of 4-bit and 8-bit Ripple Carry Adders using four different EXOR gates in 45nm CMOS technology is observed. And also the values of power, delay and the number of transistors used is observed. By comparing the parameters of ripple carry adders it is identified that the EXOR [6] gate is power efficient, delay efficient and also area efficientwhile considering 8-bit ripple carry adder. While considering the 4-bit ripple carry adder EXOR [6] gate is delayefficient and area efficient and EXOR [8] gate is power efficient.

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