Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

DESIGN OF LOW POWER SRAM CELL FOR HIGH DENSITY MEMORY APPLICATIONS

Dr. J. Sudhakar[1], Ch. Naveena[2], D. Indrani[3], G. Chandrakala[4], G. V. Naga Lakshmi[5]
[1]Principal & Professor, Dept. of ECE, Vignan's Institute of Engineering for Women, Duvvada.
[2,3,4,5] UG Students, Dept. of ECE, Vignan's Institute of Engineering for Women, Duvvada.
[2]naveenachalla2002@gmail.com

ABSTRACT
SRAM cells are the fundamental components in modern digital systems. The design of an efficient and reliable SRAM cell is crucial for the successful implementation of these digital systems. So, this paper aims to explore the potential of low power SRAM standard cells for high density memory applications. Here, various designs and configurations of low power SRAM cells are evaluated and compared to traditional SRAM cells and it also focuses on analyzing the performance of these cells in terms of power consumption, speed, and area utilization. The results of this study will provide valuable insights for the development of high-density memory applications with low power consumption and efficient area utilization. After performing necessary analysis and comparing all the SRAM cells with each other we observed that the proposed 8T SRAM cell provides low power dissipation and less delay than the remaining SRAM structures. Therefore, the proposed SRAM cell can be a good option for low power and high-density memory applications.

Keywords:
Low Power, Static Random Access Memory (SRAM), Less Delay, Power Delay Product (PDP)

1. INTRODUCTION
SRAM (Static Random Access Memory) cell is a type of memory cell that stores a bit of digital information in an electronic circuit. It is called "Static" because the data stored in the cell remains there as long as power is applied to the circuit. SRAM cells are widely used in microprocessors, cache memory, and other digital integrated circuits. They play a crucial role in the functioning of modern digital systems, providing fast and reliable memory solutions for a wide range of applications.
Now a days, low power applications like medical devices, internet of things devices, wearable and portable electronic devices are in demand which has the necessity of ultra-low power SRAM cells to store the information. In order to design low power SRAM cells, controlling the power consumption of the cell in SoCs (System on chips) has become a major task. While designing the SRAM cells one should consider minimum number of transistors to avoid more space.But when we try to reduce the area by decreasing the transistors it gives rise to process variations which can result in deviations from the ideal performance of the SRAM cell. These variations can arise due to variety of factors, such as variations in the doping of silicon substrate, variations in the thickness of the oxide layers, and variations in the alignment of the lithographic mask used to pattern the various layers. It also worsens the scaling that can cause adverse effects in the cell operation by increasing the leakage power which leads to increase in power consumption of SRAM cell which is not recommended to implement low power SRAM cells. So,to reduce the power consumption in the SRAM cells, we need to reduce the supply voltage to threshold voltage level. But if we take down the supply voltage it results in the degradation of stability and performance of the cell.
By considering all the above aspects one should design a SRAM cell without effecting its operationto meet their requirement. In this paper, different SRAM cell structures (6T, ST1, WRE8T, SB9T, 12T, 11T, 8T) are analyzed and calculated their performance parameters like average power, delay, and PDP (Power Delay Product) for both read and write operations. Finally, after comparing the results it

shows that the proposed 8T SRAM cell consumes low power than other cells and its speed of operation is also improved compared with the conventional cell. So, this proposed SRAM cell can be a better choice for designing ultra-low power SRAM cells that can be used in many portable electronic devices.

2. LITERATURE SURVEY

In this literature survey, we will review the recent advancements and challenges in SRAM cell design, focusing on the different architectures, techniques, and technologies used to improve the performance and power consumption of SRAM cells.

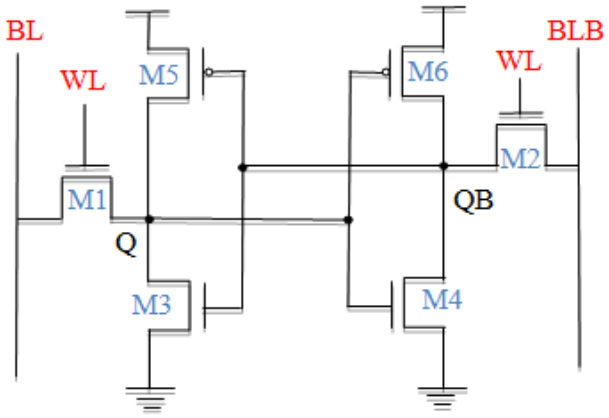
[1] Nabavi, M., & Sachdev, M. (2018), proposed a 290-mV, 3.34-MHz 6T SRAM cell to increase the stability of the bitcell during read operation and uses a boosted wordline to improve the write ability with minimum energy consumption.

[2] Kulkarni, J. P., Kim, K., & Roy, K. (2007), proposed a 160mV robust Schmitt trigger based sub threshold SRAM cell which exhibits built-in process variation tolerance and reduces read/write power. The results of this study shows that the ST bitcell can hold on to the data at low supply voltages.

[3]Javad Mohagheghi, Behzad Ebrahimi & Pooya Torkzadeh (2022), proposed Single-Ended 8T SRAM cells which possess high write ability and less read/write energy. Due to the separate read path from bitlines, the cell provides high read stability.

After surveying the above references and comparing those SRAM cells in terms of power consumption and delay, we aim to design an SRAM cell using eight transistors to improve the overall power consumption and delay of the cell.

3. RELATED WORK



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Industrial Engineering Journal
ISSN: 0970-2555
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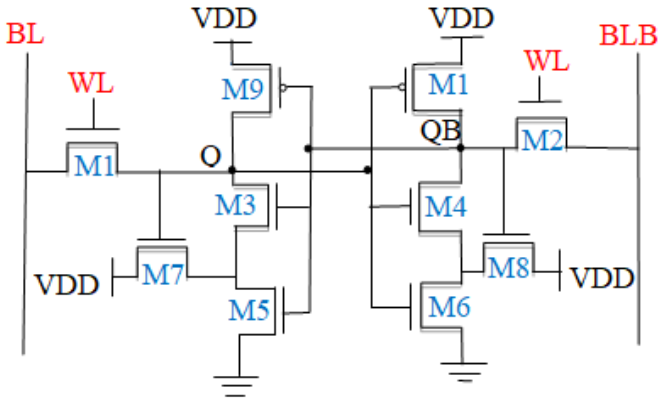

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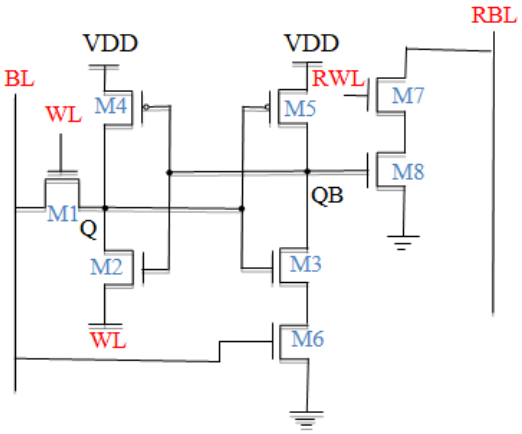

(c)

Figure 1. Schematic of different SRAM cells (a) 6T SRAM cell (b) ST-1 SRAM cell (c) 8T SRAM cell.

6T SRAM cell uses six transistors to store a single bit of data. It consists of two cross-coupled inverters and two access transistors, which are used to read and write data to the cell. The cross-coupled inverters store the data as a latch, while access transistors allow external signals to read and write data to the cell. The circuit provides low standby power consumption, fast read, and write times, and high reliability. Although the cell is designed to be low power, it still requires a significant amount of power to operate, particularly when compared to other types of memory cells. The performance of this SRAM cell is highly dependent on the manufacturing process, making it more sensitive to process variations and more difficult to manufacture constantly.

ST-1 SRAM cell uses ten transistors to store a single bit of data. It is a type of memory cell used in digital circuits that incorporates Schmitt trigger inverters instead of traditional inverters in the memory cell. This cell consists of two cross coupled inverters with a Schmitt trigger inverter in between them, which allows it to operate memory reliably at lower voltages and in noisy environments. This circuit can operate at a low supply voltage than traditional SRAM cells and it also minimizes the power consumption of the memory cell, which is useful in low power applications, but the Schmitt trigger SRAM cells are generally larger and more complex which increase the area and overall size of the chip, which can increase manufacturing cost and decrease yield.

8T SRAM celluses eight transistors to store a single bit of data. This SRAM cell consists of two cross coupled inverters and two access transistors for each of the two inverters. The access transistors allow the external signals to write data into the cell or to read data from the cell. This cell provides improved

stability, reduced leakage, and higher immunity to process variations. But the cell is more complex to design, due to more number of transistors it increases the size and area required on the chip, which may increase the cost of the memory and reduce the overall chip yield. More transistors also increase the dynamic power consumption of the cell, which can increase the time & cost of designing the memory and reduce its overall reliability.

4. PROPOSED 8T SRAM CELL

The proposed 8T SRAM cell includes two additional transistors, one NMOS and one PMOS to the standard 6T SRAM cell as shown in the Figure 2. This cell consists of two word lines and two bitlines in its configuration. This proposed cell uses a single-ended read approach that is, only RWL(Read Word Line) signal is asserted during the read operation which activates the access transistors and allows the stored value to be read from the cell.

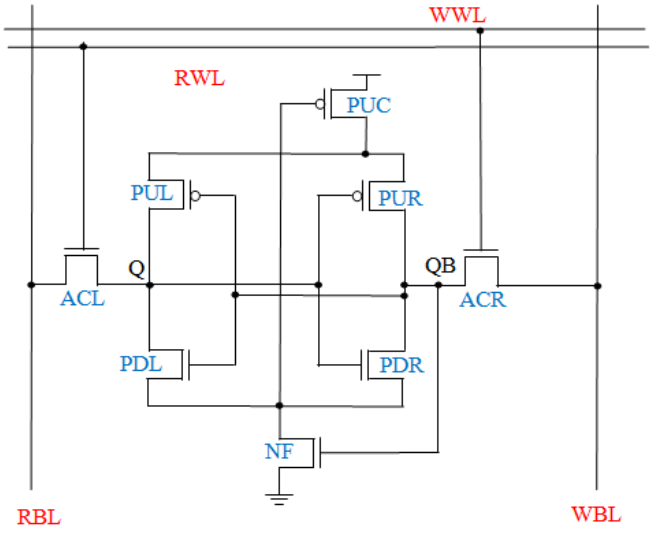

Figure 2. Proposed 8T SRAM cell

Table 1. List of control signal voltages of proposed 8T cell.

Control signals	Hold	Read	Write
WWL	GND	GND	VDD
RWL	GND	VDD	VDD
WBL	VDD	VDD	VDD
RBL	Pre-charge	Pre-charge	Pre-charge

4.1. Write Operation

During write operation, both WWL and RWL signals are set to high which turns on the transistors ACL and ACR that allows connection between the bitlines and storage nodes. The transistor PUC is used to improve the write margin when “1” is stored on the storage node Q. By weakening the drivability of PUC when QB is “0”, the voltage on the drain of NF increases, which makes it easier to write a “0” on the storage node. However, when QB is “1”, the write margin is not as expected. So, by sizing PUR smaller than PUL the write margin can be improved in both WWL and RWL modes.

4.2. Read Operation

Industrial Engineering Journal
ISSN: 0970-2555
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During read operation, only RWL is set to high which turns on the transistor ACL and the ACR is kept off. When Q is 0, transistors PDL and NF discharge the bitline capacitance, while PDR, PUL, and ACR are off. When Q is 1, NF is off and there is no discharging path from Q to ground, which results in significant improvement in read static noise margin.

4.3. Hold Operation

During hold operation, both WWL and RWL signals are set to low which turns off the access transistors ACL and ACR. Since there is no connection between the storage nodes and the bitlines, no read or write operation is performed in the cell. So, the data present in the storage nodes will be in hold state. When Q holds "0" both NF and PDR transistors are turned on which improves the data retention and keeps "0" at QB.

RESULTS AND DISCUSSIONS

6T SRAM CELL:

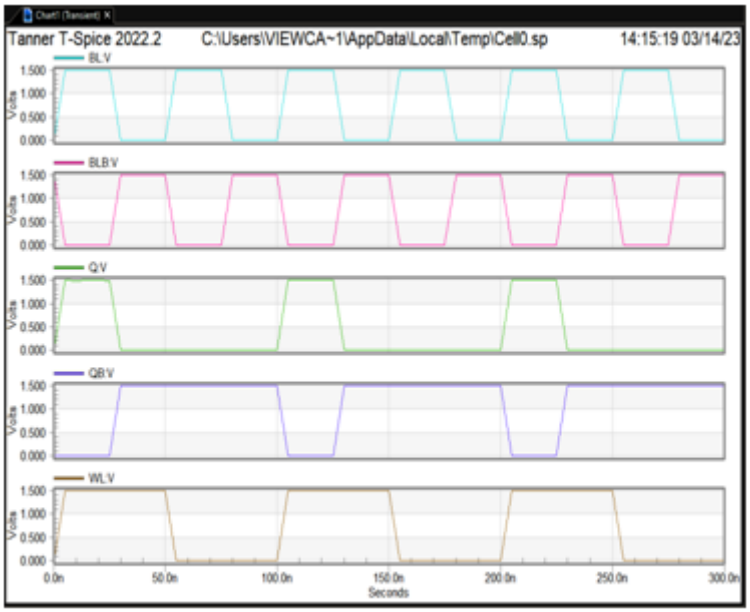

Figure 3a. Write operation of 6T SRAM cell

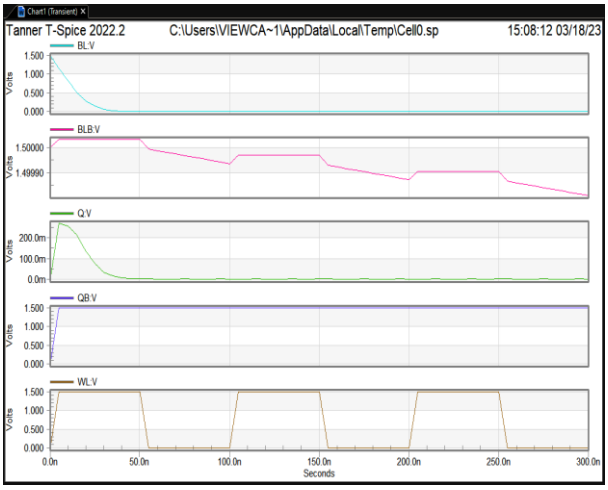

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Figure 3b. Read operation of 6T SRAM cell

ST-1 SRAM CELL:

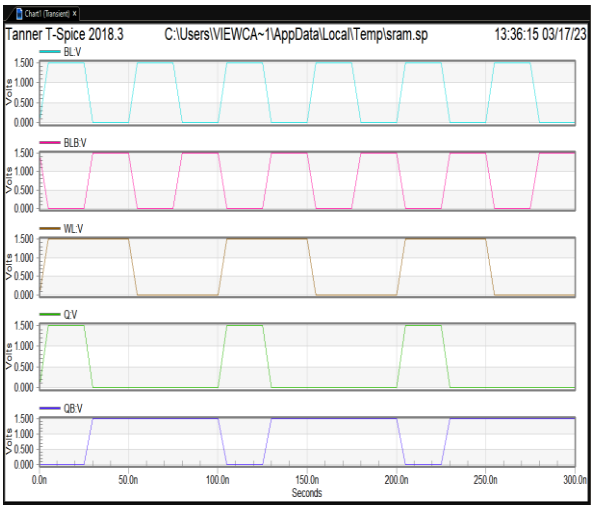

Figure 4a. Write operation of ST-1 SRAM cell

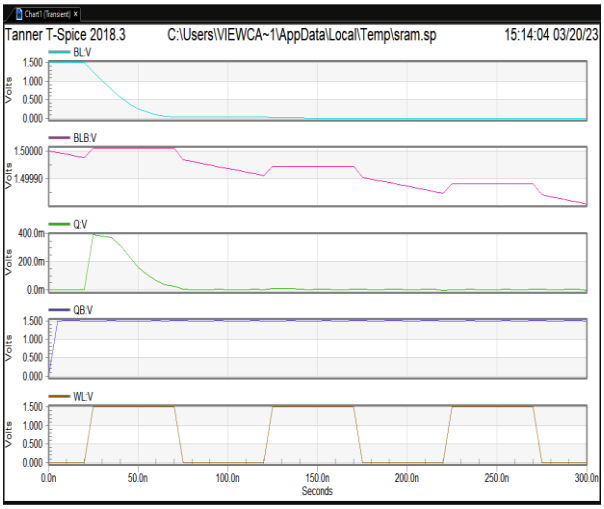

Figure 4b. Read operation of ST-1 SRAM cell

8T SRAM CELL:

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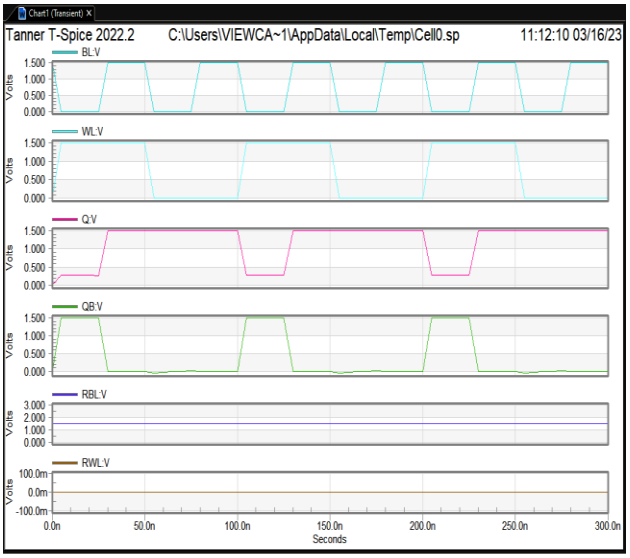

Figure 5a. Write operation of 8T SRAM cell

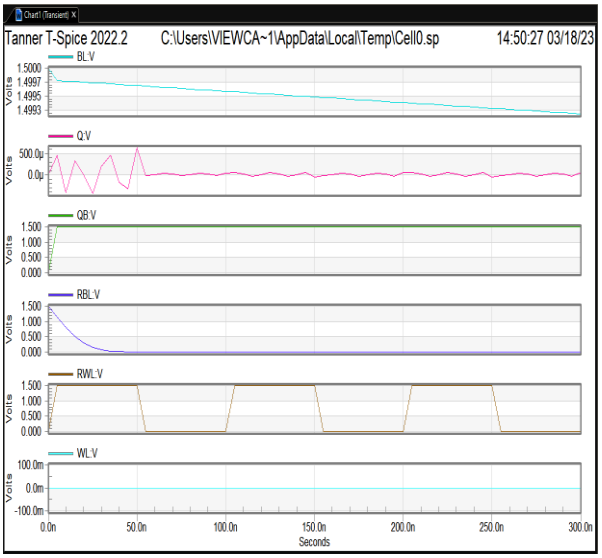

Figure 5b. Read operation of 8T SRAM cell

PROPOSED 8T SRAM CELL:

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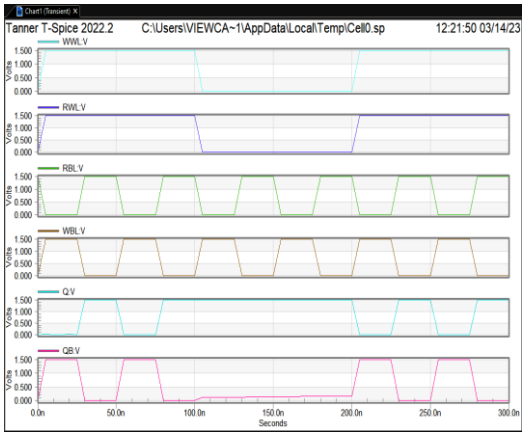

Figure 6a. Write operation of Proposed 8T

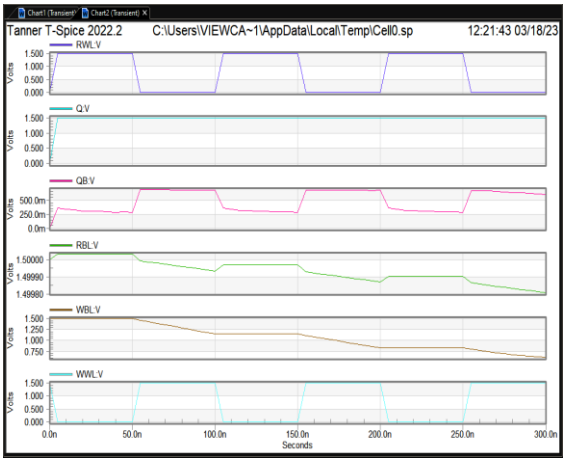

Figure 6b. Read operation of Proposed 8T

SRAM cell SRAM cell

Table 2. Comparison table of various SRAM structures

SRAM Cells	Power (µWatts)	Delay (nSec)	Power Delay Product
6T	53.2916	26.5734	1416.13
ST-1	57.5547	26.4379	1521.62
8T	123.4218	33.8912	4182.91
PROPOSED 8T	49.3997	30.40631502.06	

CONCLUSION

This project is entitled “Design of a proposed low power 8T SRAM Cell for High Density Memory Applications.” is useful to design an SRAM cell for low power and high-density memory applications. In this project the comparison between different types of SRAM cells in terms of power and delay are done. Finally, after analyzing the results, we conclude that the proposed 8T SRAM cell provides low

power consumption and less delay to improve the speed of operation.

FUTURE SCOPE

As of now, the proposed cell uses a single-ended read approach which will reduce the swing of the output. There are several future scope techniques for 8T SRAM cells that can improve their performance, power efficiency, and reliability such as FinFET technology, Write-assist techniques etc needs to be further explored.

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