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A Short Review on Low Power VLSI Design Techniques

B.Rajani, Assistant professor, Department of Electronics and Communication Engineering , PSCMR College of Engineering and Technology , Vijayawada , Andhra Pradesh , India

B.Sushma, Assistant professor, Department of Electronics and Communication Engineering , PSCMR College of Engineering and Technology , Vijayawada , Andhra Pradesh , India

ABSTRACT

Since CMOS technology consumes less power it is a key technology for VLSI circuit design. With technologies reaching the scale of 10 nm, static and dynamic power dissipation in CMOS VLSI circuits are major issues. Dynamic power dissipation is increased due to requirement of high speed and static power dissipation is at much higher side now a days even compared to dynamic power dissipation due to very high gate leakage current and subthreshold leakage. Low power consumption is equally important as speed in many applications since it leads to a reduction in the package cost and extended battery life. This paper surveys contemporary optimization techniques that aims low power dissipation in VLSI circuits.

Keywords: Power dissipation, dynamic power, static power, clock gating, adiabatic logic

I. INTRODUCTION

In the past, chip performance (speed), size, and price were priorities for IC designers. However, with speed, the semiconductor industry have recently been increasingly concerned with the power consumption of the VLSI ICs. Due to the scaling down of MOSFETs in nanoscale technologies and mass production, chip size and cost are not yet a key problem.

In CMOS circuits, the two primary causes of power dissipation are dynamic power dissipation and static power dissipation. The switching of the circuit's input, output, and internal nodes from logic 0 to logic 1 and vice versa accounts for the majority of the dynamic power consumption. When both PMOS and NMOS transistors are ON, power dissipation via short-circuit current flow from the supply to the ground has a negligible impact on dynamic power consumption. Leakage current flow in the OFF state MOS transistors is the second cause, which results in static power dissipation. Due to the vast number of transistors in the off state on today's chips, static power dissipation is becoming more dominant.

Leakage current is a critical part to be considered when designing low power VLSI circuits. Low power consuming components along with low power design has add on advantages. In the past, the real focus for VLSI design was on performance, area, and cost. But now low power is as important as these factors since there is scaling down of technology along with increasing complexity. Scaling down leads to leakage current which pose a major challenge in VLSI design. Many researchers presented that leakage power dissipation is up to 40 percent of total power consumption in deep sub-micron technologies. Reducing power consumption varies from application to application. For example, in mobile phones, which fall in the class of small scale fueled battery applications, the main objective is to keep the battery life long enough along with a low cost.

II.POWER DISSIPATION IN CMOS CIRCUITS

In CMOS circuits, there are two types of power dissipation: static and dynamic. Switching power dissipation and short-circuit power dissipation are two more categories for dynamic power dissipation. The charging and discharging of the circuit's node capacitances (also known as parasitic capacitances) is the primary cause of switching power dissipation.

When both PMOS and NMOS transistors are turned ON simultaneously in CMOS circuits, short-circuit current flow from VDD to ground is the cause of short-circuit power dissipation. Short-circuit current flow duration affects the quantity of short-circuit power dissipation.

III. TRANSISTOR LEVEL TECHNIQUES

Threshold voltage change : Both a higher and a lower MOS transistor threshold voltage can help to reduce power dissipation. Transistors with higher threshold voltages have lower subthreshold leakage current. Lower static power dissipation is the outcome of this. On the other hand, one may reduce the supply voltage of the circuit by using transistors with lower threshold voltages, which reduces dynamic power dissipation.

SOI transistors : We have been utilizing bulk transistor technology for a long time. Technology for SOI (Silicon on Insulator) transistors has recently been created. The existence of a buried oxide layer underneath the active silicon layer is the primary distinction between bulk and SOI transistors. As a result, it is possible to electrically separate one transistor from the others.

IV. CIRCUIT LEVEL TECHNIQUES

Gate delay and power dissipation in a combinational circuit are impacted by transistor size. A logic gate with wider transistors will have a decreased gate delay, but its switching power dissipation

will be higher. It is computationally challenging to determine the size of the transistor that minimises power dissipation for a specific delay restriction. Calculating the slack at each gate in the circuit is one approach to this problem. Positive slack gives us the flexibility to slow down the gate while maintaining the crucial path delay. When processing circuits with positive slacks, transistor size is decreased until the slack is zero or when all transistor sizes are equal.

The NAND gate circuit in Figure 1 was created using CMOS technology. A quick qualitative inspection of this circuit reveals that Cout and Ci's parasitic capacitances should experience less charge transfer for low power dissipation. Applying a high transition signal to input A and a low transition signal to input B will accomplish this. Pin ordering is the name given to this method.

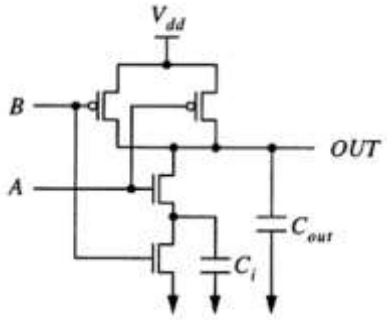

Figure 1. Input CMOS NAND Gate

V.ADVANCED TECHNIQUES

The adiabatic name for this logic design method refers to the ideal case in which it uses no power. Static CMOS circuits are powered by a steady source of electricity. During the charging and discharging of the load capacitance, energy is lost in this circuit due to the channel resistance of the MOSFETs. Figure 2 depicts a four-phase adiabatic inverter that was initially designed to reduce this power dissipation and maximize energy recovery.

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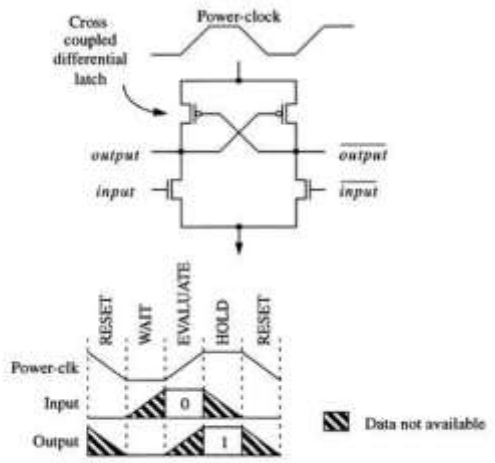

Figure 2. Four-phase Adiabatic Inverter

The circuit receives a differential input, and the output is also differential. For this circuit to function, a four-phase power clock is necessary. The supply voltage varies. The circuit is powered by a variable power-clock, however. Positive feedback is produced by cross-coupling differential output PMOS transistors. When doing logic computing, NMOS transistors serve as evaluation transistors. As seen in Figure 2, logic is calculated during the EVALUATION and the HOLD phases. For the circuit to operate synchronously and step-by-step, the other phases are necessary.

Only at lower frequencies can an adiabatic circuit have high power efficiency. As shown by graphs in Figure 10, at higher frequencies, the energy consumption of adiabatic circuits became comparable to that of static CMOS circuits.

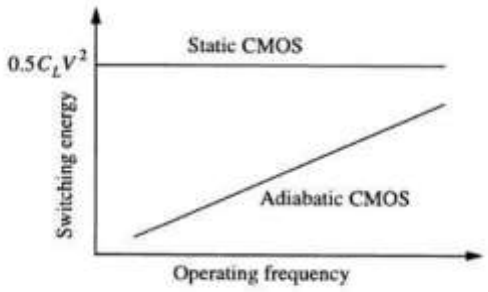

Figure 3. Switching Energy of Adiabatic Logic and Static CMOS

Today, high frequency clock signals applied to synchronous processor units cause the majority of dynamic power dissipation in the device. There will be significant power savings if we are successful in designing an asynchronous processing unit since a clock signal is not needed. The intrinsic delay of the circuit elements restricts the speed of the asynchronous compute unit.

Figure 4 shows a generic block diagram of an asynchronous processing unit. The acknowledge and request signals serve as a clock signal by keeping the computation sequence in sync. The

acknowledge and request signals do not need to be routed throughout the IC, similar to the clock signal. The switching actions in the asynchronous compute unit are greatly reduced in the absence of a high-speed clock signal.

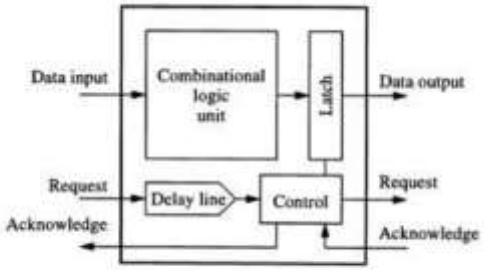

Figure 3. A General Asynchronous Computation Unit.

VI.CONCLUSION

At several levels of design abstraction, power optimization strategies are described. Due to the extremely high degree of integration, static power dissipation on the chip is constantly rising. of order to reduce the extremely high leakage current of CMOS circuits, new manufacturing and design methodologies and techniques are currently being developed. Currently, high speed clock signals contribute far more to dynamic power dissipation than chip-based data processing. The clock gating approach is the most commercially prevalent power optimization technique among those discussed in this study. While asynchronous processing and adiabatic logic architecture are preferable options, they have significant practical drawbacks. Techniques for power optimization at the software and operating system levels are becoming increasingly popular these days.

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