Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 5, May : 2023

# Low Power and Area Efficient Design of VLSI Circuits

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## ABSTRACT

Leakage power, which accounts for an ever-increasing fraction of chip overall power consumption in deep submicron technologies, is crucial for a low power design. When designing CMOS VLSI circuits, power dissipation is a crucial factor. In battery-powered applications, high power consumption reduces battery life and has an impact on packing, cooling, and dependability. We provide a method for constructing CMOS gates dubbed LCPMOS that considerably reduces leakage current without raising dynamic power dissipation. In order to solve the leakage issue in CMOS circuits, the LCPMOS technique employs a single additional leakage control transistor that is driven by the output from the pull up and pull down networks and placed in a path from the pull down network to ground. This additional resistance reduces the leakage current in the path from the supply to ground. The key benefit of LCPMOS over other approaches is that it reduces space requirements and active state power consumption because it doesn't need any additional control or monitoring circuitry. Along with this, another benefit of the LCPMOS approach is that it decreases leakage power to a level of 91.54%, which is more effective than other leakage power reduction techniques in terms of area and power dissipation.

**Keywords** - sub threshold leakage current; LCPMOS; voltage scaling; LCT; self-controlled LCT; deep-submicron.

## I.INTRODUCTION

The three main causes of power loss are: 1) capacitive power loss caused by the charging and discharging of the load capacitance; 2) short-circuit currents brought on by the brief time a logic gate is in a transition state and a conducting path exists between the voltage supply and ground; and 3) leakage current. Subthreshold currents and reverse-bias diode currents make up the leakage current. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors as shown in fig1.Digital integrated circuits are found everywhere in modern life and many of them are embedded in mobile devices where limited power resource is available (e.g. mobile phones, watches, mobile computers…). To permit a usable battery runtime, such devices must be designed to consume the lowest possible power. Furthermore, low power is also very important for non-portable devices, too. Indeed reduced power consumption can highly decrease the packaging costs and highly increase the circuit reliability, which is tightly related to the circuit working temperature.

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Hence, low power consumption is a zero-order constraint for most ICs manufactured today. In fact, higher performance-per-watt is the new mantra for micro-processor chip manufacturers today.In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. The reduction of the supply voltage is dictated by the need to maintain the electric field constant on the ever shrinking gate oxide. Unfortunately, to keep transistor speed (proportional to the transistor "on" current) acceptable, the threshold voltage must be reduced too, which results in an exponential increase of the "off" transistor current, i.e. the current constantly flowing through the transistor even when it should be "non-conducting". As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor increases when it is off as shown in fig2. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e. leakage power dissipation has become a significant portion of total power consumption for current and future silicon technologies. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above.

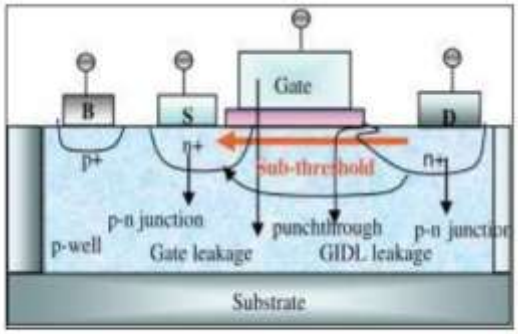


Fig.1:StaticCMOSleakagesources.

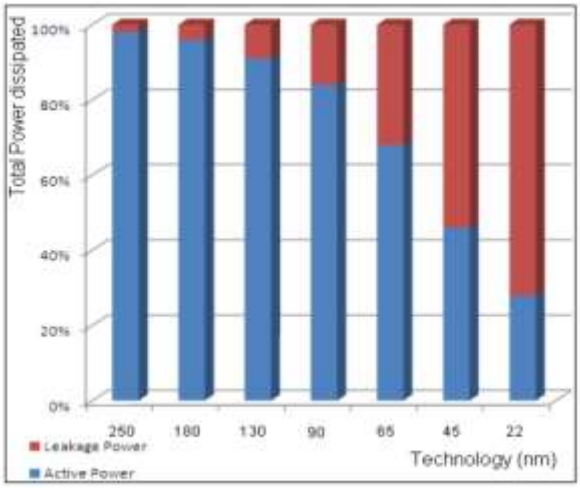


Fig.2:TechnologyVsLeakagePower

## II.LCPMOS

In the suggested method, a single leakage control transistor (LCT) is added within the logic gate, and its gate terminal is controlled by the output of the circuit itself. It results in a large reduction in leakage currents by raising the resistance of the route from the pull down network to ground and consequently increasing the resistance from Vdd to ground. The key benefit of LCPMOS over other approaches is that it doesn't need any additional control or monitoring circuitry, which reduces active state area and power consumption.

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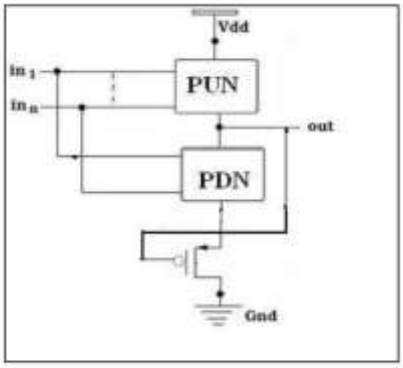


Fig.3. LCPMOSCMOSGate

The topology of a LCPMOS CMOS gate is shown in Figure 5. One LCTs are introduced between nodes N1 and Gnd. The gate terminal of LCT is controlled by the output of the circuit itself. As LCT is controlled by output , no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCT increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

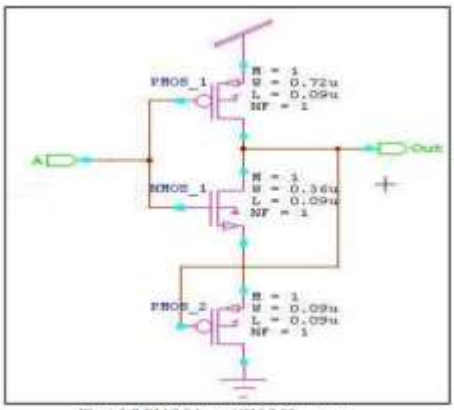


Fig.4:LPCMOS basedCMOSInverter

Leakage ControlPMOS(LCPMOS) technique is illustrated in detail with the case of an inverter. A LCPMOS INVERTER is shown in Figure6. A PMOS is introduced as LCT between N1 and Gnd nodes of inverter. When Vdd =1V, input A=0, the output is high. As the output drives the LCT the LCT goes to OFF state hence provides high resistance path between Vdd and Gnd. When A=1,theoutput is low; hence LCT will be in ON state hence output is low.LCPMOS inverter for all possible inputs are tabulated in Table I.

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TABLEI. STATEMATRIXOFLCPMOSINVERTER

| Transistor Reference | InputVector(A) | |
|---|---|---|
| | 0 | 1 |
| M1 | ONState | OFFState |
| M2 | OFFState | ONState |
| LCT | Near Cut-OFF State | ONState |

In the sleep related technique, the sleep transistors have to be able to isolate the power supply and/or ground from the rest of the transistors of the gate. Hence, they need to be made bulkier dissipating more dynamic power. This offsets the savings yielded when the circuitisidle. Sleep transistor technique depends on input vector and it needs additional circuitry to monitor and control the switch in sleep transistors, consuming power in both active and idle states. In comparison, LCPMOS generates the required control signals with in the gate and is also vector independent. Single transistor is added in LCPMOS technique in every path from Vdd to Gnd irrespective of number of transistors in pull-up and pull-down network. Where as, forced stack save 100% area overhead. The loading requirement with LCT is a constant which is much lower.

## III.APPLYINGLCPMOSTO CMOSCIRCUITS

Various circuit applications of the LCPMOS technique are explored in this section. The LCPMOS technique is applied to the following CMOS circuits and also the irrespective base case are implemented to calculate the amount of leakage power reduced in LCPMOS technique.

A. *LCPMOS basedNOT gate*

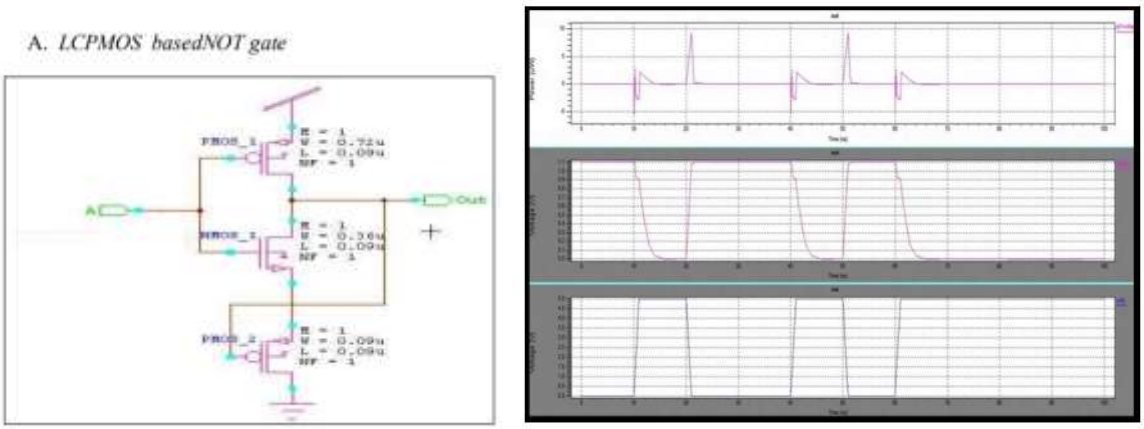

**Fig.5: Simulation wave form so fLCPMOS NOT**

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## V.EXPERIMENTALRESULTS

The leakage power is measured using the S-EDIT simulator. The results obtained through the technique for NOT gate is shown in Table III. Simulation for the NOT is performed by taking three different process parameters Viz.180nm, 90nm, 65nm.

TABLEII. NOT RESULTSFOR VARIOUSTECHNOLOGIES

| Technology | Leakagepower (uW) | | | %age decreasein power dissipation (LCPMOS) |
|---|---|---|---|---|
| | BASE CASE | LECTOR | LCPMOS | |
| 180nm | 130 | 78 | 39 | 70 |
| 90nm | 110 | 31 | 9.3 | 91.54 |
| 65nm | 98 | 5 | 3.8 | 95.4 |

## VI.CONCLUSION

The increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nano meter technologies and thus it becomes a great challenge to tackle the problem of leakage power. LCPMOS uses one LCT which is controlled by the output of circuit itself. LCPMOS achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LCPMOS technique when applied to generic logic circuits achieves up to 80-92% leakage reduction over the respective conventional circuits without affecting the dynamic power. A tradeoff between Propagation delay and area overhead exists here.

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