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Performance Analysis of FIR Filter Designs with Different Parallel Prefix Adders

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ABSTRACT

A typical digital filter application on a digital signal processor (DSP) reads input samples from an A/D converter, performs the mathematical operations required by theory for the required filter type, and outputs the result via a D/A converter. Finite Impulse Response (FIR) filters are the most popular type of filters in this scenario.Unlike analogue filters, which utilise finite precision arithmetic to calculate the filter response, digital filters use finite precision arithmetic to represent signals. This project uses the VERILOG programming language to construct a FIR filter in Xilinx ISE. In this project, the FIR filter's VERILOG coding is implemented, and waveforms are seen through simulation.The adders Koggestone, Sklansky, and Square Root Carry Select have been selected for this project. As part of this project, we must create an RTL for the structures, test their functionality, and use the Xilinx synthesiser to do the synthesis. The findings for various fir constructions are contrasted in terms of speed.Keywords : FIR filter, Skalansky adder, koggestone adder, Brent kung adder and VLSI Architecture.

1.INTRODUCTION

Filters are a crucial component of DSP. Actually, one of the main factors contributing to DSP's enormous popularity is their extraordinary performance[2]. Essentially, a filter is a device or network that enhances the quality of a signal, extracts information from it, or separates two or more signals that were previously merged. In many applications today, digital filters are taking over the traditional function of analogue filters by performing a variety of filtering functions.[1]These filters have gained popularity because analogue filters may provide performance levels that are difficult to reach within

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designers' reach with digital filtering. thanks to their exact reproducibility.Three basic mathematical procedures can be combined to create digital filters. adding or subtracting, multiplying (often by a fixed amount, and time delay (the practise of delaying a digital signal by a predetermined number of sample cycles)) are all operations that can be performed on signals.A digital filter is depicted graphically in Figure 1 by applying the aforementioned mathematical processes to illustrate the filter's behaviour.

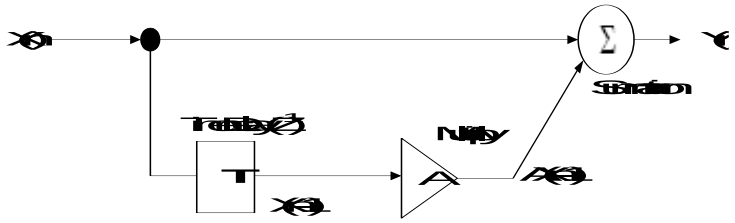

Figure 1: Block diagram of a Simple Digital Filter

A digital filter's reaction The "impulse response," In reaction to a unit impulse function input (n), the system's output is denoted by the function h(n)[2]. Any input sequence x(n) can be predicted using the system's impulse response. A system is defined as one that receives the unit impulse. when the sample index is set to 0. This means that When n is equal to zero, the impulse response, denoted by h(n), is negative. Since the system would not generate this impulse response in the absence of an input, we classify it as causal. A linear time-invariant system will always respond to a delayed unit impulse with another delayed unit impulse, h(n-k), according to the time-invariance property of the system. The output of a system in response to a sum weighted inputs is the sum weighted output of the inputs themselves. according to the linearity property. [1,2]The following expression describes the output of the system given the input x(n).:

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

The main need for electrical circuit design is an adder with great efficiency and precision. For improved In order to evaluate how well an optical logic gate-based adder circuit performs with optical input signals of varying wavelengths, shown here[9]. The adder's efficiency can be raised by accelerating operations, simplifying the design, and using less power.[9] In this work, a novel adder combination has been designed and tested in order to retain high efficiency with precision. [9]A novel adder built by fusing using the Tree Grafting Technique (BSKTGT), the adders Brent Kung, Sklansky, and Kogge Stone's reasoning have been evaluated alongside the original versions of these algorithms.

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2.LITERATURE REVIEW

D. Jhansi and P. EswaraRao'suse of adder trees to implement low-area and delay-bit arithmetic. [3] Audio applications increasingly use digital filters. As a result, the design of audio systems must take appropriate digital filter performance into account. Unlike analogue filters, which utilisedigital filters employ signal representations based on finite-precision arithmetic and thereafter rely on this representation in order to calculate the filter's output.In this instance, a FIR-filter was built using the VERILOG programming language. in Xilinx ISE. B.Siva Prasad, K. Pradeep, M. Anusha, and The phrase "An Optimisation Power Of Adder Trees For Multiple Constant Multiplications" [4]The primary delays in data flow graphs (DFG) and digital circuits are propagation delays. Many different methods have developed to shorten propagation delays. The retiming procedure is one of them. Retiming is a method that focuses on switching up the flow graph's delay elements without modifying the inputs or outputs of the circuit. This approach focuses focus particularly on adders and multipliers, the fundamental building blocks of addition and multiplication. Digital filters differ from analogue filters in that they encode signals with finite precision and employ finite precision arithmetic to calculate thefilter response

. 3.EXISTED DESIGN

A)FIR FILTERS USING KOGGE STONE ADDER

Practically any type of digital frequency response can be implemented using a FIR filter[1,2]. These filters frequently employ they use a multiplier, an accumulator, and a delay circuit to generate their result. A multiplier was used in a conventional FIR filter to multiply the input data and fixed coefficients.TheKogge stone adder was used to combinethe end result. The schematic of a simple FIR filter of length N is shown below. Delays have an impact on the input samples. The multiplicative coefficients used are bi, i=1, 2, 3,... All of the delayed samples are combined together, multiplied by the appropriate factors, and then the o/p at a moment is obtained.

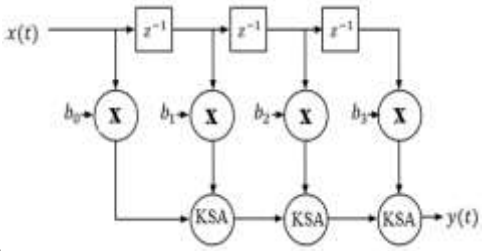

Figure 2:Logical Structure of FIR Filter using kogge stone adder

KOGGE STONE ADDER

KSA is shorthand for a prefix form-based carry look-ahead adder. High speed arithmetic circuits typically use it because it generates carry in O (log n) time.. It is commonly regarded as the quickest

adder.[5] Through the use of parallelization, KSA is efficient at carrying out carry-on calculations a larger area.By breaking down KSA [5] into its three main components, it is simple to understand how it functions completely.

Pre-processing:[10] Signals to be created and propagated for each bit pair are calculated at this step. in A and B[5].

pi = Ai *xor*Bi

gi = Ai *and* Bi

2 . Carry look ahead network:[5]The uniqueness of this block is what gives KSA its high performance compared to other adders. At this point, the carriers for each bit are calculated.[10]Intermediation is achieved through the usage of group propagate and create.

Pi:j = Pi:k+1 *and Pk:j*

Gi:j = Gi:k+1 *or* (Pi:k+1 *andGk:j*)

3. Post processing:The last step, shared by all members of this family of adders (carry look), forward), is this one. Sum bits[5][10] calculation is required.

Si = pi xor Ci-1

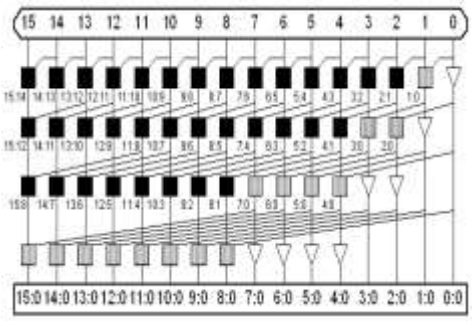

Figure 3:16 bitkogge stone adder

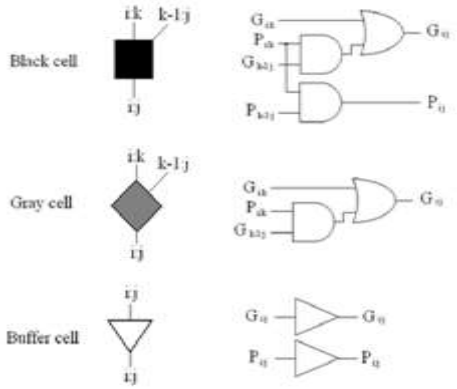

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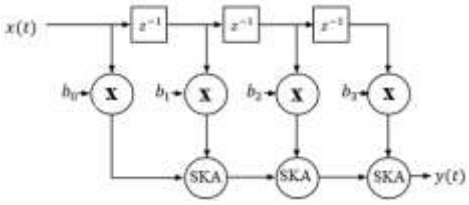
Figure 4:Complex logic cells inside the Prefix Carry Tree

B)FIR FILTERS USING SKLANSKY ADDER

To implement practically any kind A FIR filter is used digitally to provide a frequency response. Multipliers, The output of is typically generated using adders and a chain of delays. these filters. Traditional FIR filters used a multiplier to combine the input data with the filter's fixed coefficients[1,2]. The Sklansky adder was used to sum the results from. The following diagram depicts the basic N-length FIR filter. The input samples suffer from delays. Multiplication uses the coefficients bi, where i=1, 2, 3, etc. The o/p is accomplished by by multiplying the total number of lag-time samples by delay period. Relev

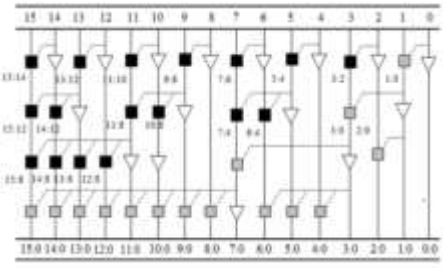


ant coefficients.

Figure5: FIR filter using skalansky adder

SKALANSKY ADDER

Known as a typical scheme in parallel prefix adders, the Sklanskystructure.However, the big fanout's increased delay limits its application[8].Figure depicts the 16-bit Sklansky adder's schematic[6]. Another name for the TheSklansky adder is the tree of divide and conquer. 1960's Sklansky'sIn order to achieve a minimal depth prefix network, Prefix addition logic that uses conditional sum addition makes more fan-out compromises for specific computation nodes. When a node is present, the longest wires are used for lateral fanning. is connected to n more nodes. Large amounts of latency are explained by the Sklansky's adder's fan-out, which greatly rises throughout the critical path from inputs to outputs[6]. The performance of the structure degrades as the number of bits in the



adder grows.

Figure 6: 16 bitskalansky adder

4.PROPOSED DESIGN

FIR FILTERS USING BRENT KUNG ADDER

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A FIR filter is used to implement practically any type of digital frequency response. These filters frequently employ a multiplier, adders, and a series of delays to produce their output.[1,2] In a typical FIR filter, the input data and fixed coefficients were multiplied. A square root carry select adder was used to combine the output from. The following figure displays the basic FIR filter diagram with N length. A delay affects the input samples.. For multiplication, the coefficients bi, i=1, 2, 3, etc. are used. All of the delayed samples are combined together, multiplied by the appropriate factor, and then the o/p at a time is obtained. coefficients.

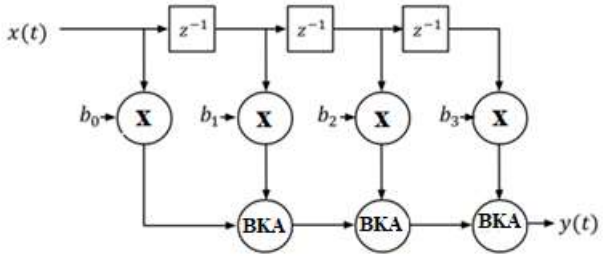

Figure7: FIR filter using BKA

BRENT KUNG ADDER

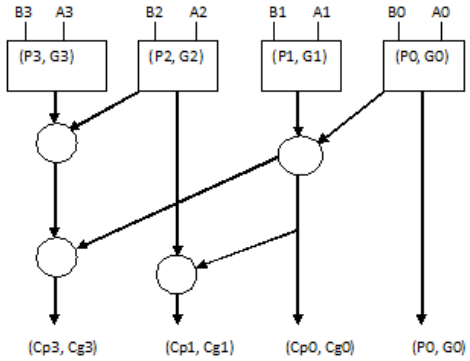

Figure 8: 4-bit Brent-Kung adder

CPO = Pi and Pj

CGO = (Pi and Gj) or Gi

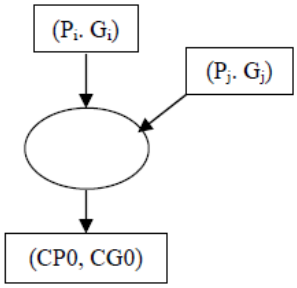

Figure9:Carry network

The Brent-Kung adder has gained widespread acceptance and widespread use. There are a lot of steps from the input to each output, which is great, however the stages in the middle aren't evenly loaded[7]. As such, it is categorised as a parallel prefix adder. It is a member of the exclusive group of adders known as parallel prefix adders, which function by creating and spreading signals. Brent kung adders have both reduced cost and simplified wiring requirements. likewise simpler. However, Brent-Kung adders' gate level depth is 0 (log2 (n)), which results in slower speed.

5.RESULTS

RTL SCHEMATIC:Register Transfer Level (RTL) is an abbreviation for the architectural design document. It is used to evaluate the designed architecture in relation to the ideal architecture.The conversion of the data into the architectural summary into a coded language, such as i.everilog or vhdl. In order to facilitate study, the RTL schematic includes details on the internal connection blocks.The image below depicts the RTL schematic diagram of the planned architecture..

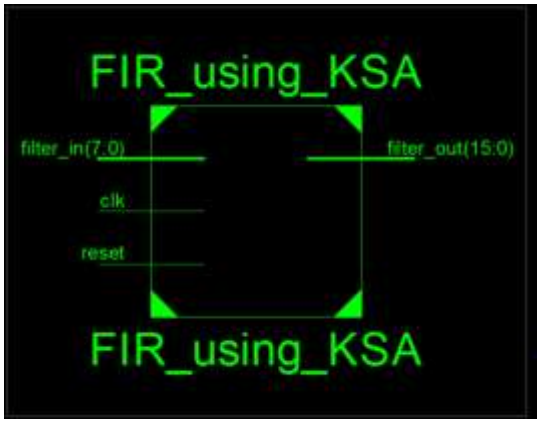

Figure10: RTL Schematic of FIR filter using kogge stone adder

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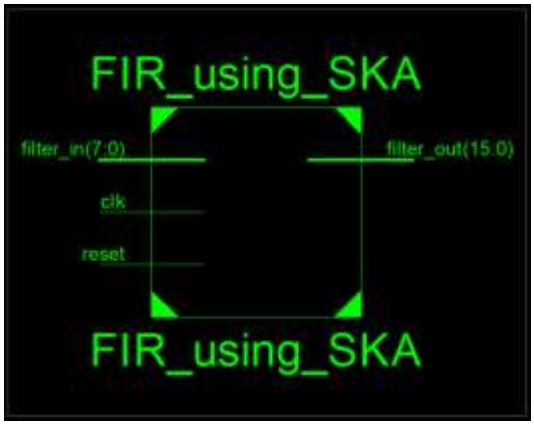

Figure11: RTL Schematic of FIR filter using skalansky adder

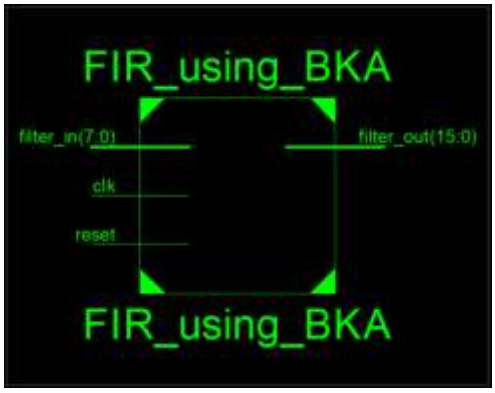

Figure12: RTL Schematic of FIR filter using brent kung adder

TECHNOLOGY SCHEMATIC:The VLSI design estimation procedure makes use of the LUT as a parameter of area, and the technology schematic generates an image of the The LUT format is used for building.The look-up tables (LUTs) of the FPGA are where the code's memory allocation is depicted as a square..

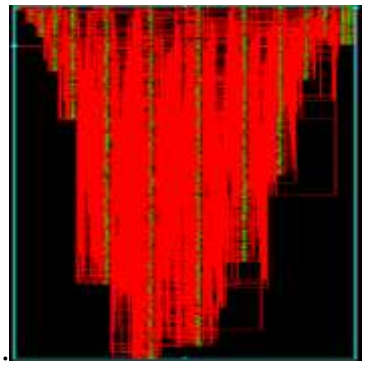

Figure13:View Technology Schematic of FIR filter using kogge stone adder

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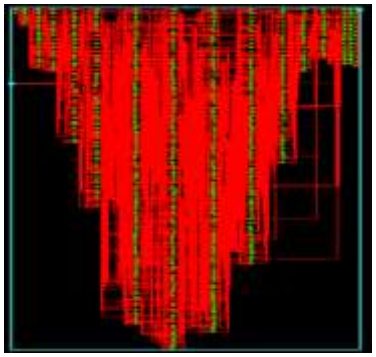

Figure14 :View Technology Schematic of FIR filter using skalansky adder

Figure15:View Technology Schematic of FIR filter using brent kung adder

SIMULATION:The simulation represents the process, while the schematic is used to validate the links and components. When the user toggles the tool from implantation mode to simulation mode, the simulation window opens on the main screen. The results can only take the shape of waves within the simulation window. Here, it's adaptable enough to supply several distinct radix number systems..

Figure16:Simulated Waveforms FIR filter kogge stone adder

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Figure17:Simulated Waveforms FIR filter skalansky adder

Figure18:Simulated Waveforms FIR filter brent kung adder

PARAMETERS:Area, delay, frequency, and power are four variables that are considered in VLSI; using these variables, one can compare one architecture to another. Here, area and Considerations of frequency are made. The HDL language employed is called Verilog., and the tool XILINX 14.7 is used to extract the parameter

Parameter	FIR Using KSA	FIR Using SKA	FIR Using BKA
No of LUTs	528	347	320
Frequency (MHz)	122.234	121.374	128.584

Table1: parameter comparison

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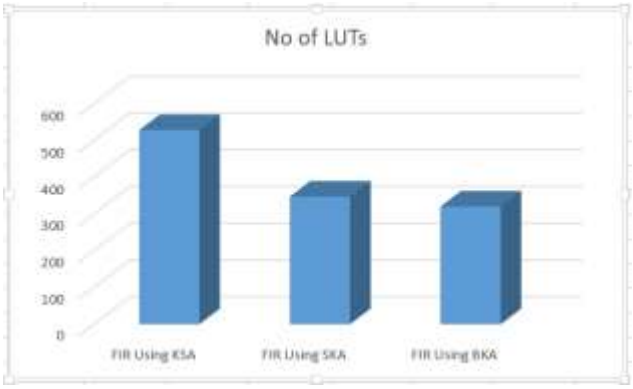

Figure19: LUT comparison bargraph

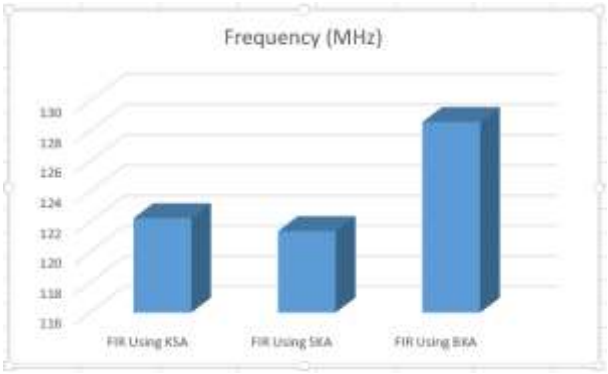

Figure20: frequency comparisonbargraph

CONCLUSION

Many architectures have been developed over the past 20 years for the design of low complexity operating systems. However, the FIR design has not been improved in this way. This project provides the answer to such kinds of needs. It is clear from the table that the FIR using the Brent Kung Adder Structure takes up less space and operates at high speeds compared to the FIR using the Kogge Stone and FIR using the Skalansky Adder Structure. Therefore, based on the needs of industry, it has a chance to use the corresponding structure from this project. Future research on these structures using reversible logics may offer a chance to improve power optimisationslightly.**REFERENCES**

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