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Efficient Power Management and Delay Reduction in Positive Feedback Comparator Design

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Abstract: In this research paper, a new and innovative affirmative feedback comparator design is suggested, which holds a crucial function in electronic circuits, specifically used to match two input signals and yield one output signal. The comparator is a fundamental element in electronic circuits, used to compare analog signals and is a significant component in the design of many electronic systems. The proposed comparator design is a low-energy two-stage dynamic comparator, which incorporates PMOS transistors at the input of the initial and secondary stages of the comparator. This design leads to a halved power consumption, which allows for a manageable pre-amplifier gain. However, it results in a longer delay and an increased transistor count, which can be a limiting factor in high-performance electronic systems. To overcome this limitation, the proposed design introduces a positive feedback comparator, which not only reduces power consumption but also reduces propagation delay in contrast to the existing low-energy two-stage dynamic comparator. The proposed design utilizes advanced techniques to achieve a better overall performance and efficiency, which can be highly beneficial in many electronic applications. The backend simulations for the proposed comparator design are achieved by using MENTOR GRAPHICS in 130nm technology, while frontend simulations are conducted using XILINX. This helps to validate the proposed design and its potential use in real-world electronic systems. Overall, the proposed affirmative feedback comparator design has the potential to offer significant advantages over existing comparator designs, especially in terms of power consumption, propagation delay, and transistor count. This can lead to more efficient and high-performance electronic systems, which can have a broad range of applications in various industries.

Keywords: Dynamic comparator, Positive feedback comparator, Mentor graphics, Pre-amplifier gain, Low-power two stage dynamic comparator

INTRODUCTION :

Nowadays, the applications of Analog to Digital Converters (ADCs) have expanded significantly, making them indispensable across a wide range of industries. These applications include communication systems, biomedical implants, and digitally-assisted analog circuits. Comparators play a pivotal role in these applications, particularly in commonly used ADCs such as Flash, SAR, and Pipeline ADCs. In the past, Operational Amplifiers (Op-Amps) were used as static comparators [1]. However, Op-Amps come with their limitations, including limited speed due to feedback and stabilization, and high power consumption as a result of the circuit being always active due to the small intrinsic gain of the transistors and short channel effects [2].

To tackle these challenges, dynamic comparators were introduced [3,4]. Dynamic comparators offer improved performance compared to static comparators, with faster operation and reduced power consumption. This is made possible by implementing techniques such as positive feedback and latch-based circuits to enable the comparator to operate only when required. The use of these techniques results in a significant reduction in power consumption and improved performance. Overall, dynamic comparators have become an integral part of modern ADCs, as they offer improved performance and efficiency when compared to their static counterparts. These advancements have paved the way for the development of more efficient and high-performance ADCs, which have broad applications across various industries. As a result, there is a growing demand for these technologies, leading to significant advancements in the field of ADCs and associated technologies. In summary, these electronic circuits involve a pre-amplifier stage and a latch that work together to produce the desired output. The pre-amplifier stage generates a differential voltage based on the input differential voltage, while the latch amplifies the differential voltage to match the level of the supply voltages (VDD and GND). However, the direct connection between the pre-amplifier and latch outputs leads to a significant swing that can cause kickback noise. This can be particularly challenging when a capacitive Digital to Analog Converter (DAC) is connected to the input pins of the comparator. Kickback noise can distort the voltage stored on capacitors and cause non-linear errors in an ADC. To address this issue, two-stage dynamic comparators were proposed. These comparators connect their pre-amplifier stage outputs to the latch inputs, resulting in a capacitive path from the latch outputs to the inputs that is a series combination of two Gate-Drain capacitors. This setup minimizes the effect of kickback noise, allowing for more accurate and reliable operation of the ADC. The Gate-Drain capacitors used in the latch stage are usually much smaller in size than those employed in the pre-amplifier stage. This size difference helps to reduce the kickback noise to a great extent. In dynamic comparators, the clock signal and its inverted counterpart (clkn=clk) are both necessary for carrying out the comparison process. However, the direct connection between the pre-amplifier and the latch stages causes the two-stage comparator to still be affected by the issue of kickback noise. To overcome this problem, a low-power technique has been proposed which significantly reduces power consumption. However, implementing this technique can lead to an increase in both delay and transistor count. As an alternative, a new method has been suggested called the “Positive Feedback Comparator”. This type of comparator consumes less power and exhibits less propagation delay compared to low-power two-stage dynamic comparators.

Comparator circuits

The figure labeled as Fig. 1 depicts the two-stage dynamic comparator along with its corresponding circuit during the reset and evaluation phases. The input signals are directed towards the pre-amplifier stage, and the outputs of this stage are connected to the inputs of the latch stage. The comparator's operation involves two phases: the reset-phase and the evaluation-phase. During the reset-phase, the clk signal is set to "1," while the clkn signal (the inverted version of clk) is set to "0." This phase resets the output voltages of the preamplifier stage to ground and the output voltages of the latch stage to vdd. The grey-colored "off" transistors in Fig. 1(b) depict the comparator during the reset-phase. To initiate the evaluation-phase, the clk signal is set to "0," and clkn is set to "1," thereby disconnecting the constant paths to ground and vdd, respectively. Additionally, the pre-amplifier current source (M5 in Fig. 1) is turned "on." Gradually, a differential voltage starts to appear at the output nodes of the first stage. The latch stage amplifies its input

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differential signal (using positive feedback) to vdd on one side and ground on the other side, when the output voltage levels of the pre-amplifier stage exceed the threshold voltage of the input NMOS transistor of the latch stage (M10 and M11 in Fig.1). Moreover, the outputs of the pre-amplifier stage become vdd.

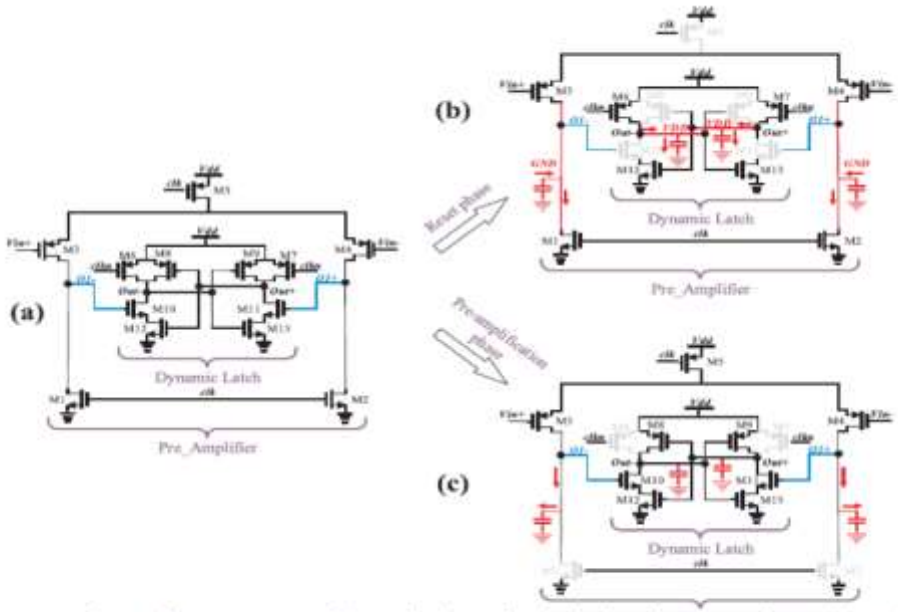

Fig. 1 (a)Two stage dynamic comparator (b) equivalent circuit during the reset phase (c) equivalent circuit during the evaluation phase.

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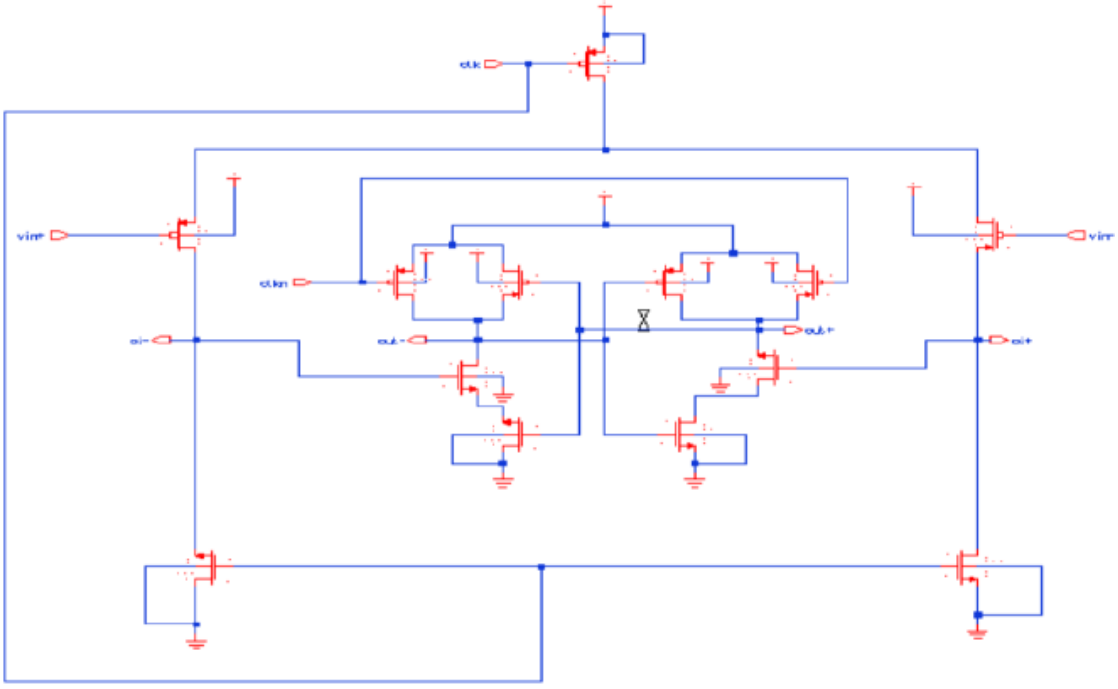

Fig. 2 Two stage dynamic comparator schematic diagram

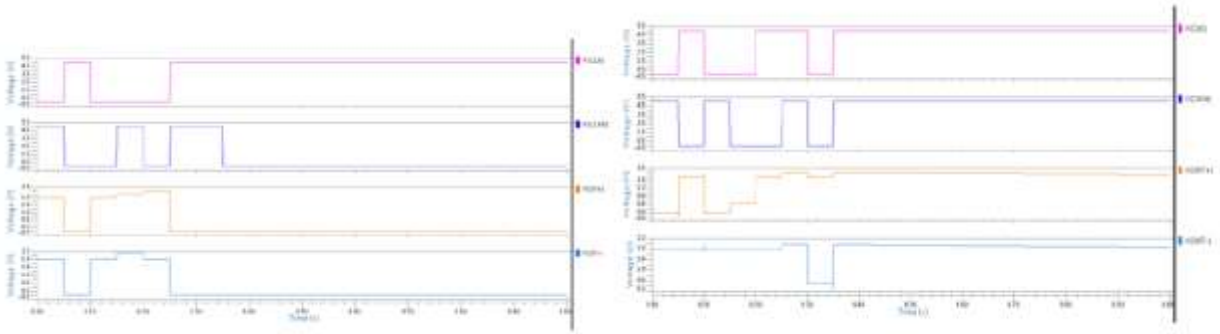

Fig. 3 Two stage dynamic comparator simulation results

2.2 Low-power Two stage dynamic comparator

During the evaluation phase of the two-stage dynamic comparator, the outputs of the pre-amplifier stage gradually increase from zero towards vdd due to the charging process of the output nodes. Unfortunately, this behavior results in an excess power consumption in the pre-amplifier stage, which is the stage that dominates the overall power consumption. It is impossible to avoid this excess power consumption due to the unknown delay of the comparator. However, it is possible to mitigate this issue by employing a low-power two-stage dynamic comparator.

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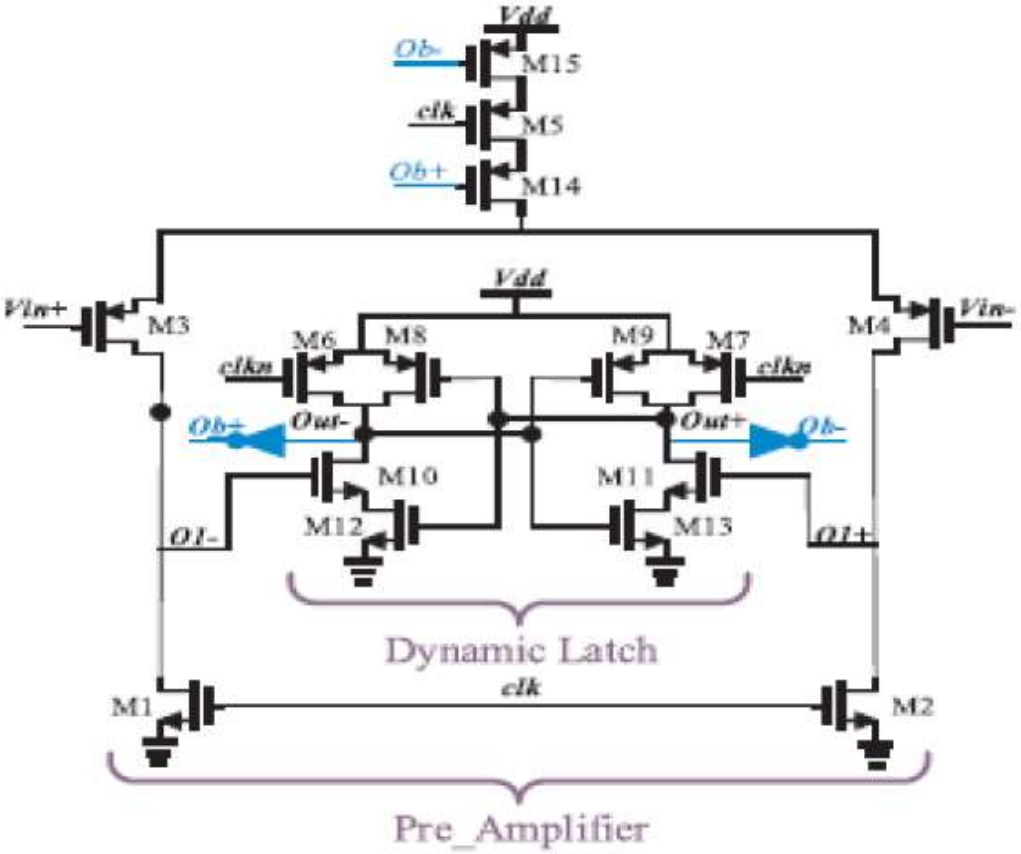

Fig. 4. Low-power two stage dynamic comparator

The figure shown above in Fig. 4 displays the low-power two-stage dynamic comparator along with its output buffers. This comparator is structurally similar to the traditional two-stage dynamic comparator, but with the inclusion of output buffers that are linked to PMOS transistors. These PMOS transistors are connected in series with the current source (M5). The reset and evaluation phases of this comparator are identical to those of the conventional circuit. To prevent excess power consumption, additional transistors, specifically M14 and M15, are utilized. Essentially, when the voltage level of only one of the output buffers approaches vdd, the current source of the pre-amplifier stage is switched off to prevent excess power consumption. This ensures that switching off the pre-amplifier stage has no impact on the dynamic behavior of the comparator. This approach is effective in preventing excessive power consumption without having any negative effects on the other parameters of the comparator. It should be noted that the functionality of the series arrangement of M5, M14, and M15 is insignificant, indicating that the order of these transistors in the circuit is not crucial to its operation.

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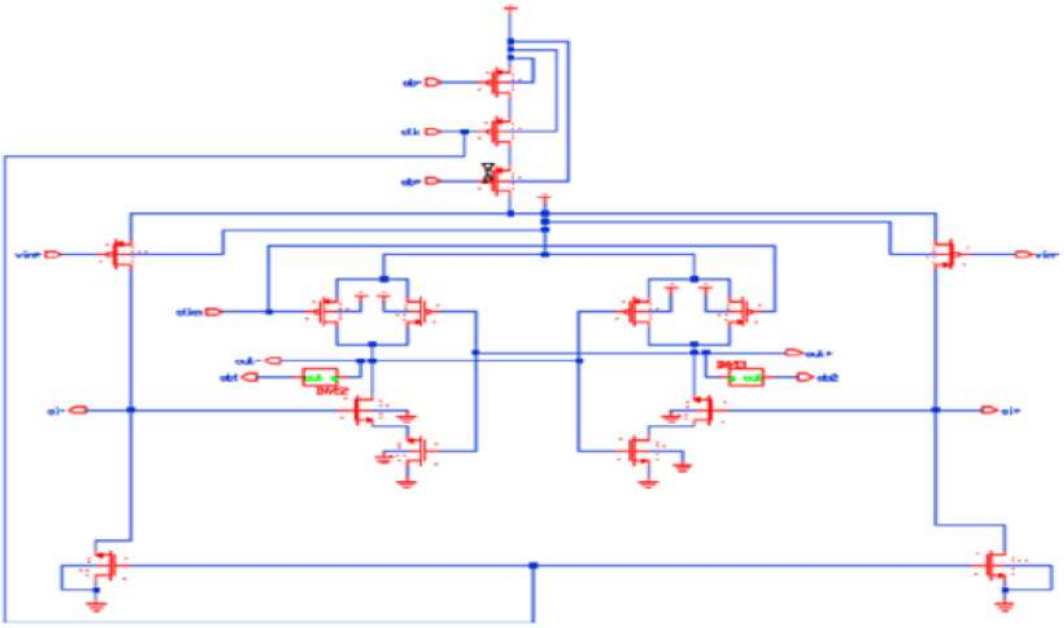

Fig.5 Low –power two stage dynamic comparator schematic diagram

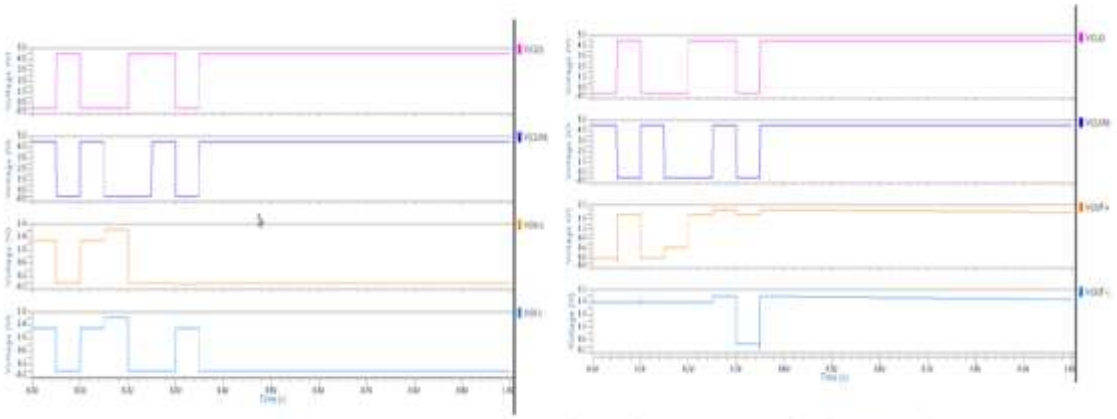

Fig.6 Low –power two stage dynamic comparator simulation results

Below is a figure (Fig. 6) that illustrates the equivalent circuit of the proposed comparator in the pre-amplification phase. At this stage, the parasitic capacitors of the pre-amplifier stage are charged from zero voltage level to vdd. It is important to mention that both voi+ and voi- charge at almost the same rate (dVC1/dt = dVC2/dt) during the pre-amplification process. Therefore, the power consumption of the pre-amplifier stage can be calculated by using the following formula (where Vsupply is equal to Vs, and Isupply is equal to Is).

$Power = 1/T \int_{0T} V_s \times I_s \, dt = 1/T \int_{0T} VDD \times (I_1+I_2) dt$,

$dV_{C1}/dt = dV_{C2}/dt$

$I_{1,2} = C dV_{C1,C2}/dt$

$Power = 1/T \int_{0T} VDD \times 2 C dV_{C1,C2}/dt \, dt = 1/T \int_{V0V1} VDD \times 2C dV_{C1C2}$ $V_0=0$, $V1=V_{final}$ $P=2C/T \times VDD \times V_{final}$, $1/T = f$,

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Power=2C×VDD×V_{final} ×f

Where Vfinal is the voltage stored over C, at the end of the conversion and f is the clock frequency. As discussed earlier, in the conventional comparator, Vfinal=vdd, however, in the proposed comparator Vfinal is less than vdd (e.g., 1.3 V in Fig 6). The power reduction of the proposed method is calculated as follows.

$P_{conventional}$= 2C/T × VDD×VDD = 2C/T×VDD_2 = 2C×VDD_2×f

$P_{proposed}$ = 2C/T × VDD× V_{final} = 2C×VDD×V_{final} ×f

Power reduction = 1- $P_{proposed}$/$P_{conventional}$ = 1- V_{final}/VDD = (VDD-V_{final}) / VDD

The above fig 5 VDD=1.8 and V_{final} = 1.3 then the value of power reduction is

Power reduction(%) = 100× (VDD - V_{final}) / VDD = 100×(1.8-1.3)/1.8=27.7%

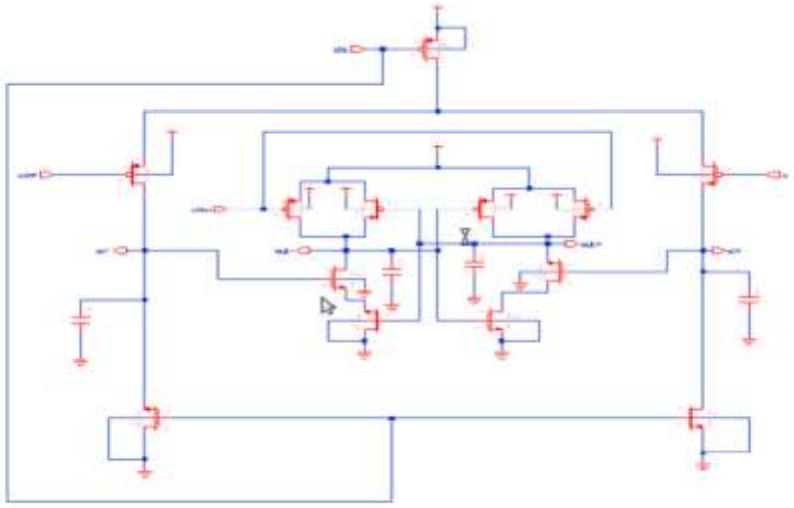

Fig 7. Equivalent circuit of the low-power two stage comparator during the pre-amplification process

III. System Overview

In this approach, we propose a design for a positive feedback comparator that is utilized to decrease the delay and transistor count in comparison to the low-power two-stage dynamic comparator.

3.1 Positive feedback comparator:

The method of positive feedback comparator is suggested as an option for decreasing delay and transistor count compared to the low-power two-stage dynamic comparator. The positive feedback comparator operates in two phases. The first is the reset phase, where the tail transistors are turned off. When the clock is 0, control transistors c1 and c2 are also turned off. The output is reset to ground with the help of transistors r1 and r2. In the second phase, called the regeneration phase, the clock signal is set equal to vdd. In this phase, both transistors c1 and c2 are turned off, and transistors r1 and r2 reset the output to ground. The input voltages cause nodes fn and fp to discharge. If the input voltage (INP>INN), then node fn discharges faster than fp. This causes the control transistor c1 to turn on and pull fp back to vdd. As a result, node fn discharges fully while control transistor c2 remains turned off.

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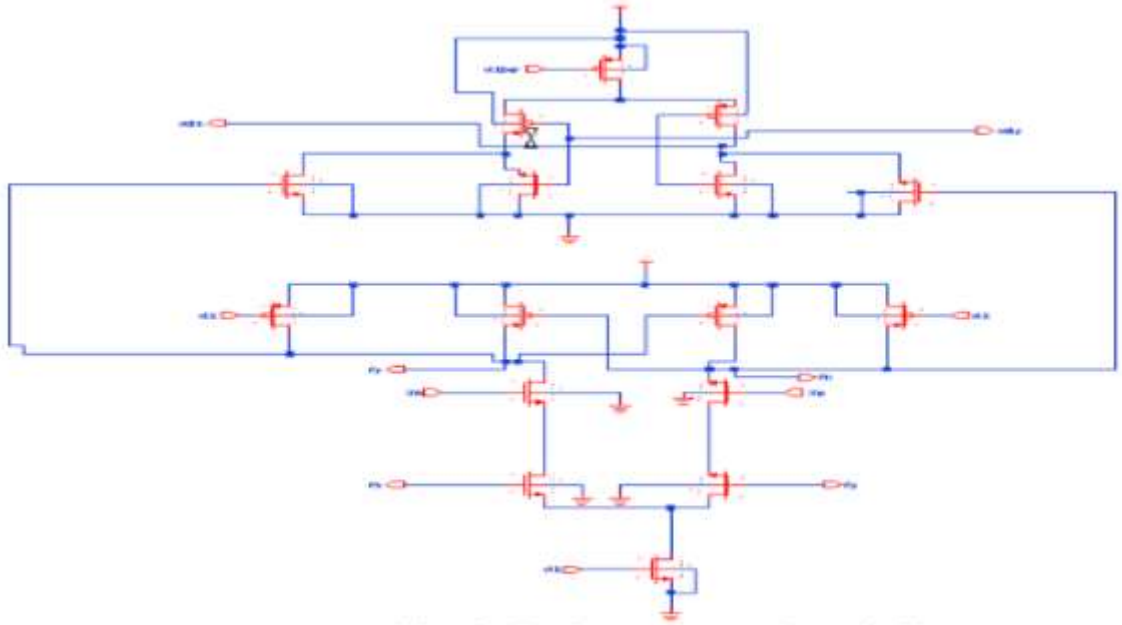

Fig 8. Positive feedback comparator schematic diagram

When the input voltage INN is larger than INP, the positive feedback comparator's operation is reversed. In this situation, node fp discharges more rapidly than node fn, and control transistor c2 is activated to pull fn back to vdd. Consequently, node fp discharges completely while the other control transistor c1 remains inactive. It is crucial to observe that when one of the control transistors is activated, it leads to the current flow from vdd to ground, which results in static power usage. During the reset phase, the node is pre-charged from vdd, and both switching transistors are shut. During the evaluation phase, one of the nodes discharges based on the input voltage, and the control transistors detect the node, which quickens the discharge rate. The switching transistor closes the other side of the node, allowing discharge without any static power usage. This mechanism enables the positive feedback comparator to work with lower power consumption and reduced delay compared to the two-stage dynamic comparator. Nonetheless, it is vital to realize that this mechanism is not the exclusive method to lower power consumption and delay in comparators. Other research can concentrate on various factors, such as precision (dynamic and static offset, noise, resolution), settling time (tracking BW, regeneration speed), sensitivity/resolution (gain), and metastability, to improve the design of comparators.

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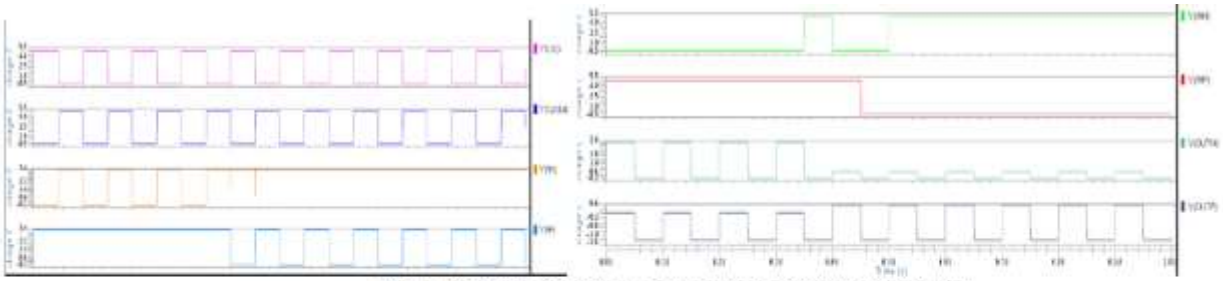

Fig 9. Positive feedback comparator simulation results

IV. Simulation Results

Power and Delay Comparision table

Parameter	Two stage dynamic comparator	Low power two stage dynamic comparator	Positive feedback comparator
Power (µW)	0.11 µW	0.005 µW	0.0005µW
Delay(ps)	291.36ps	414.53ps	100ps
No.of transistors	13	19	16

Xilinx results:

Positive feedback comparator:

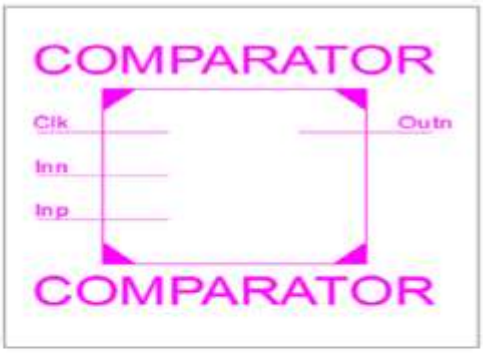

Fig 10.RTL schematic 1

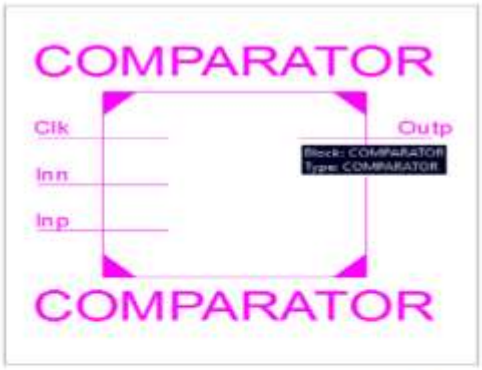

Fig11.RTL schematic 2

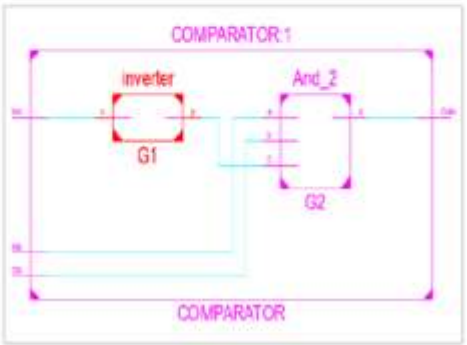

Fig 12. Internal RTL schematic 1

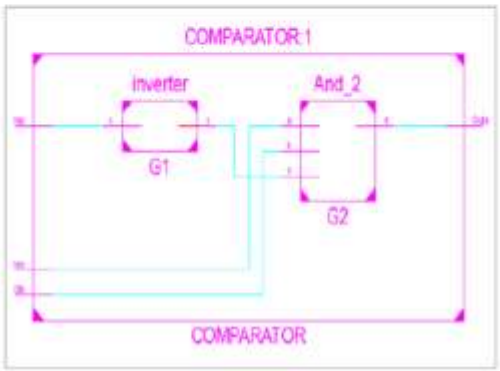

Fig 13. Internal RTL schematic 2

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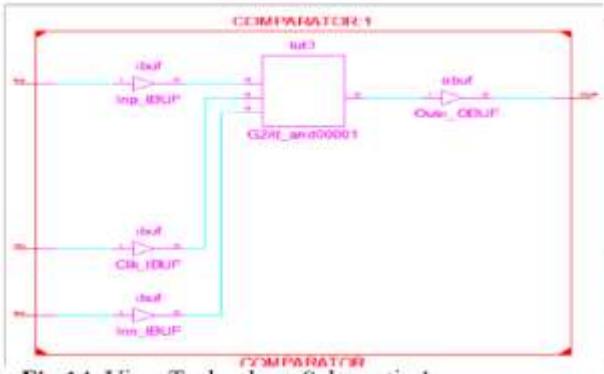

Fig 14. View Technology Schematic 1

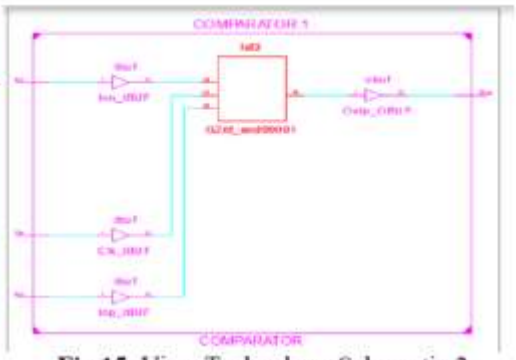

Fig 15. View Technology Schematic 2

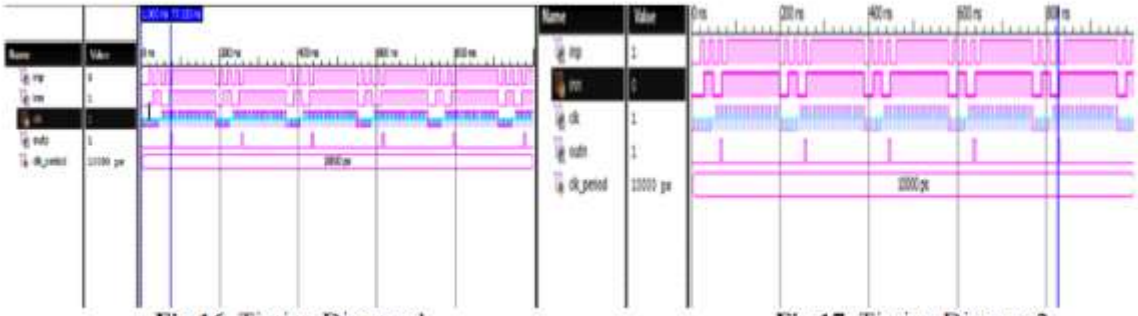

Fig 16. Timing Diagram1

Fig 17. Timing Diagram2

Conclusion and Future scope

This brief proposes a device called a positive feedback comparator that can be used to test different types of analog-to-digital converters, such as ADCS, Flash, SAR, and Pipelined ADCS. The use of this device can make the circuit faster and use less power. The results of simulations using this device can help design circuits that use less power and perform better. To learn more about hysteresis, it is important to reduce the noise created when the device switches. In the future, more research can be done to improve the design of comparators, including looking at how accurately they measure signals, how quickly they settle after a signal changes, and how sensitive they are to small changes in the input signal.

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