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Design and Analysis of High Performance Adders using EDA Tools

Ms. J Stella Mary Associate Professor
Ayesha Nishat, Shivakoti Anusha B.tech Students,

Department of Electronics and Communications Engineering, Bhoj Reddy Engineering College for Women, Vinaynagar, Santoshnagar X roads, Saidabad, Hyderabad - 500059

Abstract

The main objective of this paper is "Design and Analysis of High-Performance Adders using EDA Tools". To achieve this goal the following steps has been taken to Establish an overview of the basic addition speed-up schemes, their characteristics, and their relationships. Derive all possible adder architectures from the above speed-up schemes and compare them qualitatively and quantitively with focus on cell based circuit implementation suitability for synthesis, and realizable of customized adders. Try to unify the different adder architectures as much as possible in order to come up with more generic adder structures. The ideal solution would be a flexible adder architecture covering the entire range of possible area-delay trade-offs with minor structural changes.

I. Introduction

1.1 Introduction

Adders are considered as the critical block in multipliers and other digital circuits. By improving the performance of the adder block, the overall system performance can be improved. In this paper a correlative analysis of several adders like Carry Select Adder (CSelA), Carry Skip Adder (CSkpA), Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) will be designed and analyzed using Verilog HDL code. The performance metrics consider for comparison are area, delay and power and also the simulation as well as synthesis are performed. Hence the power and delay are described in static time analysis.

1.2 Motivation

The core of every microprocessor, digital signal processor (DSP), and data processing application specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition.

Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrementation and magnitude comparison base on binary addition. Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design.

1.3 Objective

The objective of this thesis is "Design and Analysis of High-Performance Adders using EDA Tools". To achieve this goal the following steps has been taken to Establish an overview of the basic addition speed-up schemes, their characteristics, and their relationships. Derive all possible adder architectures from the above speed-up schemes and compare them qualitatively and quantitively with focus on cell based circuit implementation suitability for synthesis, and realizable of customized adders. Try to unify the different adder architectures as much as possible in order to come up with more generic adder structures. The ideal solution would be a flexible adder architecture. Try to unify the different adder architectures as much as possible in order to come up with more generic adder structures. The ideal solution would be a flexible adder architecture covering the entire range of possible area-delay trade-offs with minor structural changes.

1.4 Historical Background

The history of the EDA industry is punctuated by periodic upheavals in technology and consequently in the balance of power. Advances in semiconductor process technology and ever increasing time-to- market demands are necessitating there-creation of Electronic Design Automation (EDA) solutions. Key technologies such as synthesis are becoming commodities and the fundamentals on which traditional logical and physical design flows were built no longer apply. The current multi vendor, multi-tool design flows cannot adequately address timing convergence, nor handle multi-million gate designs. What designers really need is a single, integrated system that can take their design straight through the flow from RTL to GDSII with guaranteed performance.

Electronic design automation (EDA) is at the center of technology advances in improving human life and use every day. Given an electronic system modeled at the electronic system level (ESL), EDA automates the design and test processes of verifying the correctness ofthe ESL design against the specifications of the electronic system, taking the ESL design through various synthesis and verification steps, and finally testing the manufactured electronic system to ensure that it meets the specifications and quality requirements of the electronic system.

1.5 Literature Survey

According to the study of S.Elango et al "Investigation and VLSI Implementation of Linear Convolution Architecture For FPGA Based Signal Processing Applications", Convolution is a mathematical operation in signal processing applications which is used to predict the response of the system for a given impulse response. Focus on this area is stressed as it has various applications on fields like Digital Signal Processing (DSP), Digital Image Processing, Linear Acoustics, and Statistics. A high speed DSP system is therefore required to perform the computational process of convolution in an effective manner. This has a detailed analysis and implementation has been carried out for linear convolution in which the architecture of Vedic multiplication is used to enhance the computational speed of convolution operation. The architecture was simulated using ISim and synthesized using Xilinx synthesis technology. The functional block has been successfully implemented in hardware using Xilinx Spartan 6 XC6SLX45- 2CSG324 Field-

Programmable Gate Array (FPGA). Finally, the output waveforms from the FPGA were displayed on Chip scope VIO console logic analysis for real-time verification.

Sangeeta Rani and Sachin Kumar, studied that Adders are the most basic and essential component used in Digital signal processing and is widely used in the digital integrated circuits. As there are various adder structures which provide the increased operational speed in the arithmetic circuits but in terms of area or delay there is a loose connection (area or delay of the adder circuit design is more as compared to the other structures discovered). With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. The addition of the two bits is very based on the various speed-up schemes for binary addition, a comprehensive overview and different bits carry skip adder structures is given in this paper. They synthesized the Carry skip adder of bits – 4 Bit, 8 Bit, 16 Bit and 32 Bit in ISE XIILINX 10.1 by using HDL - Verilog and will simulate them in Modelsim 6.4a. Also Delay, Slices Used and Look up tables used by the Different bit Carry skip adder structure is given.

Saradindu Panda, A. Banerjee, B. Maji and Dr. A.K. Mukhopadhyay, "Power and Delay Comparison in between Different types of Full Adder Circuits", describes the speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. Power consumption and speed are two important but conflicting design aspects; hence a better metric to evaluate circuit performance is power delay product (PDP). The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. Here, we have given a brief description of the evolution of full adder circuits in terms of lesser power consumption, higher speed and lesser chip size. We have started with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 8 transistors.

J. Kandpal, A. Tomar, M. Agarwal and K. Sharma, "High-Speed Hybrid-Logic Full Adder Using High Performance 10-T XOR–XNOR Cell," proposed Hybrid logic style which is widely used to implement full adder (FA) circuits. Performance of hybrid FA in terms of delay, power, and driving capability is largely dependent on the performance of XOR-XNOR circuit. In this article, a high-speed, low-power 10-T XOR-XNOR circuit is proposed, which provides full swing outputs simultaneously with improved delay performance. The performance of the proposed circuit is measured by simulating it in cadence virtuoso environment using 90-nm CMOS technology. The proposed circuit reduces the power delay product (PDP) at least by 7.5% than that of the available XOR-XNOR modules. Four different designs of FAs are also proposed in this article utilizing the proposed XOR-XNOR circuit and available sum and carry modules. The proposed FAs provide 2%-28.13% improvement in terms of PDP than that of other architectures. To measure the driving capabilities, the proposed FAs are embedded in 2-, 4-, and 8- bit cascaded full adder (CFA) structures.

E. Abu-Shama and M. Bayoumi, "A New cell for low power adders," studied that by Reducing power dissipation at the circuit level is considered one of the main factors in developing low power systems.

1.6 Proposed Method

In existing method Adders are analyzed using FPGA approach, but in previous work only a single adder delay, area and power is calculated and in some previous papers different adders are analyzed of only 8 bit. In some of the existing method ASIC implementation is proposed but performance analysis is not compared for different adders of different bits and they have been used commercial tools for implementation. As, in literature survey we can observe, there is a comparison analysis of only one adder and used commercial tools.

In this paper an ASIC Implementation approach is proposed, open-source solutions to ASIC implementation are proposed and RTL solution to the ASIC implementation are proposed. Adder topologies are compared and analysed using open source EDA tools , for each and every adder for 8 bit, 16 bit, 32 bit and 64 bit area, delay and power are calculated and trade- off condition is observed, as bit size increases in one of the metric an adder may have high performance, it differs from adder to adder according to size of the bit.

Design and Analysis of High-Performance Adders using EDA tools for RTL to GDSII generation refers to the process of designing and analyzing adder circuits with the goal of achieving high performance in terms of speed, power efficiency, and area utilization. Electronic Design Automation (EDA) tools are used to facilitate the design process, starting from the Register Transfer Level (RTL) description of the adder to the final layout generation in GDSII format.

The design of high-performance adders involves the exploration and optimization of various circuit topologies, transistor sizing, interconnect planning, and timing analysis. The adder circuits are typically implemented using Complementary Metal-Oxide-Semiconductor technology, which offers a balance between performance and power consumption.

The analysis of adder circuits involves evaluating key performance metrics such as propagation delay, power dissipation, area utilization, and signal integrity. Various techniques, such as statistical analysis and power-performance trade-off analysis, may be employed to understand and optimize the adder's behaviour under different conditions.

EDA tools play a crucial role in this design flow, providing a platform for circuit simulation, logic synthesis, physical design, and layout generation. These tools enable designers to model and analyze the adder circuits at different abstraction levels, verify their functionality, optimize their performance, and generate the final layout in GDSII format, which is compatible with the fabrication process.

The design and analysis of high-performance adders using EDA tools for RTL to GDSII generation have significant implications for the development of advanced digital systems, such as microprocessors, digital signal processors, and application-specific integrated circuits (ASICs). By optimizing the adder circuits, designers can enhance the overall performance of these systems, enabling faster computations, reduced power consumption, and improved area efficiency.

II. Block Diagram

Block Diagram of Carry Look ahead Adder(CLA), Ripple Carry Adder(RCA), Carry Skip Adder(CSkpA), Carry Select adder(CSelA) are described in this section.

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2.1 Carry Look ahead Adder (CLA

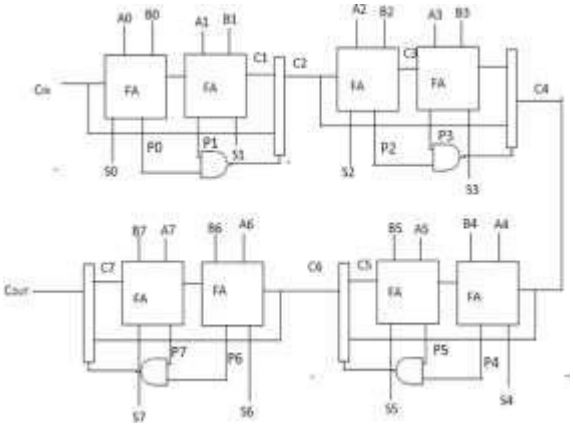

Figure 1 Carry Look ahead Adder(CLA)

The propogation of carry is dependent on the propogation delay which means that propogation can be done after the carry occurs at that particular stage, we can predict carry in advance, so that propogation delay can be reduced.

2.2 Ripple Carry Adder (RCA)

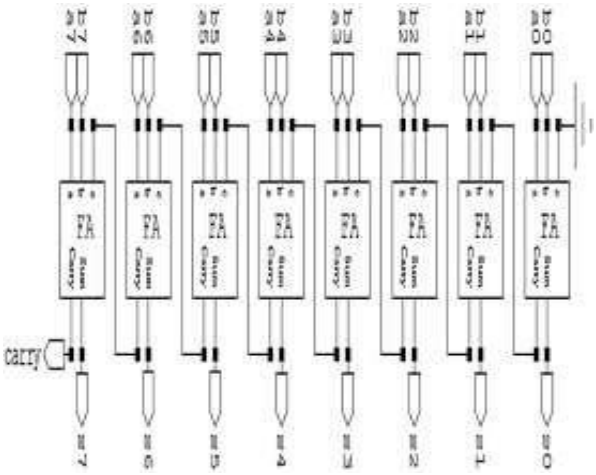

Figure 2 Ripple Carry Adder (RCA)

To design a Ripple Carry Adder full adders are required, for 8 bit RCA we require 8 full adders and they must be in cascaded form. In this circuit the out carry is given as input in next stages. The out carry is dependent on previous carry. It introduces delay, because carry cannot be predicted before, after all the computations are carried out carry can be predicted.

2.3 Carry Skip Adder (CSkpA)

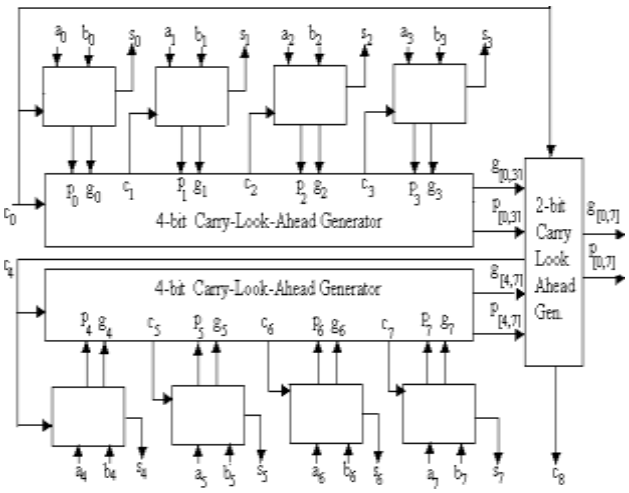

Figure 3 Carry Skip Adder(CSkpA)

Carry Skip is designed using ripple carry adder with speed up carry chain or called as skip chain. This chain defines the distribution of ripple carry blocks, which compose the skip adder.

Depending on lengthg of bits these blocks are divided, here each cell is compared and carry is propagated. In carry skip adder, we try to avoid dependency on previous carry generated. The carry-skip circuitry consists of two logic gates.

2.4 Carry Select Adder (CSelA)

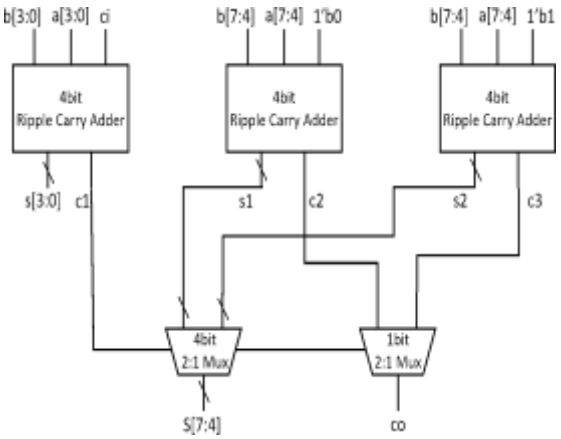

Figure 4 Carry Select Adder (CSelA)

An 8 bit carry select adder consist of three 4 bit ripple carry adders in which,one would calculate the sum and carry for low

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nibble sum (bits 0 to 3) and other two would calculate higher nibble sum and carry (bits 4 to 7). All adders would calculate in parallel, we would then use low nibble carry output as a selector for a multiplexer that would choose correct results from high nibble sums and carries

Carry Select Adder (CSelA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed parallelly. Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. Hence, the delay is reduced. However, the structure is increased due to the complexity of multiplexers.

III Simulation Results and Analysis

3.1 Introduction

It includes simulation waveforms of four adders which are Carry Look ahead Adder (CLA), Ripple Carry Adder (RCA), Carry skip Adder (CSkpA), Carry Select Adder (CSelA) of 8 bit, 16 bit, 32 bit and 64 bits and performance analysis of different parameters which are area, delay and power of adders are reported.

3.2 CLA Simulation Waveform

Figure 5 CLA Simulation Waveform

This is the simulation waveform of CLA 8 bit. In this way, Simulation waveforms are generated for CLA 16 bit, 32 bit and 64 bit.

3.3 RCA Simulation Waveform

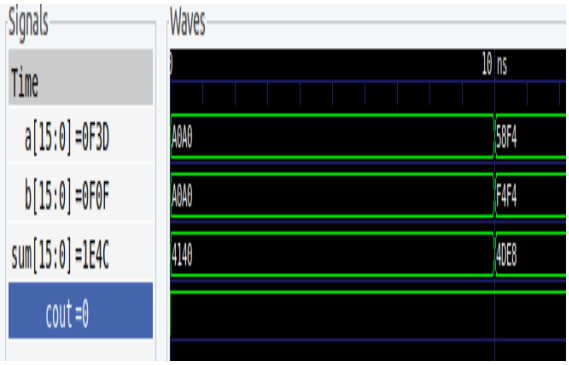

Figure 6 RCA Simulation Waveform

This is the simulation waveform of RCA 16 bit. In this way, Simulation waveforms are generated for RCA 8 bit, 32 bit and 64 bit.

3.4 CSkPA Simulation waveform

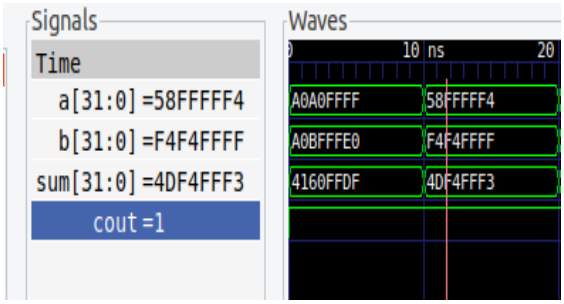

Figure 7 CSkpA Simulation Waveform

This is the simulation waveform of CSkpA 32 bit. In this way, Simulation waveforms are generated for CSkpA 8 bit, 16 bit and 64 bit.

3.5 CSelA Simulation Waveform

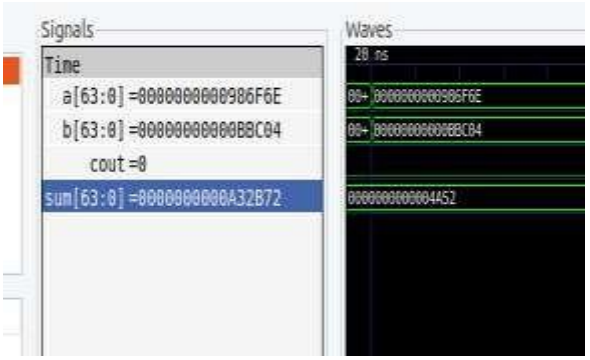

Figure 8 CSelA Simulation Waveform

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This is the simulation waveform of csela 64 bit. In this way, Simulation Waveform are generated for CSelA 8 bit, 16 bit and 32 bit.

3.6 Comparative Analysis of Adders

In this table there are different types of adders, they are Carry Look ahead Adder (CLA), Ripple Carry Adder (RCA), Carry Skip Adder (CSkpA) and Carry Select Adder (CSelA) of 8 bit, 16 bit , 32 bit and 64 bit of different parameters considered which are delay measured in nano seconds, area in micrometer square and power in milliwatts. If the comparison of an adder with different adder is observed then, in terms of delay it has high performance but in terms of area it may have low performance which is a tradeoff condition.

Table 1 Comparison Table of Adders

Adders	parameters											
	Delay (ns)				Area (μm^2)				Power (milliwatt (mW))			
	8 bit	16 bit	32 bit	64 bit	8 bit	16 bit	32 bit	64 bit	8 bit	16 bit	32 bit	64 bit
CLA	60.95	60.97	62.93	64.64	236.476800	564.291200	2718.857600	8483.136000	0.134	0.258	0.561	1.11
RCA	86.09	34.12	40.36	52.84	270.259200	540.518400	1081.036800	2162.073600	0.148	0.296	0.592	1.18
CSkpA	31.00	88.09	92.12	100.18	322.809600	645.619200	1291.238400	2582.476800	0.144	0.292	0.588	1.18
CSelA	26.61	27.03	29.06	32.32	653.126400	130.252800	2612.505600	5225.011200	0.168	0.384	1.06	2.64

From table, carry select adder has less delay while compare to all other adders but carry look ahead adder has lesser area for 8 bit while compare to other adders , if it is 16 bit and 32 bit then ripple carry adder has lesser area whereas for 16 bit carry select adder has less area. In terms of power carry look ahead adder has less power compare to all other adders.

If one adder is separately compared with other adder then again it may be different, if carry skip adder compared with ripple carry adder for delay parameter then carry skip adder has less delay compare to ripple carry adder in such case we prefer carry skip adder in order to produce high performance, like that it may be different from adder to adder in terms of different parameters with respect to different bits of adders.

IV Conclusion and Future Scope

4.1 Conclusion

In this paper an exhaustive analysis of various adder architectures has been carried out, and also explored usage of open source EDA tools and the IC design frontend activities as part of phase 1 which are simulation, synthesis and static timing analysis using Iverilog tool for functional simulation, Gtkwave tool for waveform viewer, yosys and abc tool for RTL Synthesis, Technology Mapping, and Formal Verification, OpenSTA for static timing analysis are completed. Frontend design which is also called logic synthesis has performed wherein RTL is developed and then it is verified for the correctness of the functionality through the testbench, after functional simulation is correct then the synthesis is performed to generate gate

level netlist. Through this paper a correlative analysis of several adders like Carry Select Adder(CSeA), Carry Skip Adder(CSA), Ripple Carry Adder(RCA), Carry Look ahead Adder(CLA) of 8 bit, 16 bit, 32 bit, 64 bit is analyzed using Verilog HDL code and the comparison has been performed using the parameters area, delay and power.

Through the comparison of an adder with different adder is observed then, in terms of delay it has high performance but in terms of area it may have low performance which is a tradeoff condition. From report, carry select adder has less delay while compare to all other adders but carry look ahead adder has lesser area for 8 bit while compare to other adders , if it is 16 bit and 32 bit then ripple carry adder has lesser area whereas for 16 bit carry select adder has less area. In terms of power carry look ahead adder has less power compare to all other adders. So the performance may be different from adder to adder in terms of different parameters with respect to different bits of adders.

4.2 Future Scope

In future this project can be extended by including more adder architectures such as Kogge-Stone Adder, Hybrid Adder and it can be implemented in open-source production PDK(Process Design Kit) foundry from global foundries using technology node of 180nm. The Backend activities can be performed which are Floor-planning, Placement, Clock Tree Synthesis, Routing and GDSII generation using open source EDA tool

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