Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 3, No. 1, March : 2024

A MAJORITY LOGIC GATES BASED NANO COMMUNICATION NETWORK WITH PARITY ESTIMATION

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Abstract
The nano communication system finds applications in various fields, including biomedical devices, Internet of Things (IoT) sensors, environmental monitoring systems, industrial automation, and smart infrastructure. Existing CMOS-based systems encounter challenges such as limited bandwidth, high power consumption, and susceptibility to noise and interference, hindering their performance in nano-scale communication environments. So, the Majority Logic Gates (MLGs) based Turbo Encoder in Nano Communication Networks (TE-NCN) with Parity Estimation presents a novel approach to enhance data transmission efficiency in nano-scale communication networks. The proposed TE-NCN system addresses these limitations by leveraging MLG-based encoding techniques and parity estimation algorithms to improve data reliability, minimize power consumption, and enhance communication robustness in nano-scale networks. Through comprehensive simulations and experiments, we demonstrate the effectiveness of our proposed methodology in achieving higher data transmission rates, lower power consumption, and improved reliability in nano-scale communication networks. By integrating MLG-based Turbo Encoding and Parity Estimation into nano communication systems, the TE-NCN system opens up new possibilities for efficient and reliable data transmission in diverse applications, contributing to the advancement of nano-scale communication technology..
Keywords: Turbo Codes, Maximum-a-Posteriori Algorithm, ML-RSC, Interleaver, Vivado

1. Introduction

In the present scenarios, data transferring between the systems plays a vital role as the technologies are increasing day-by-day and the number of users is simultaneously increasing. This wide usage leads to major issues in the digital communication systems and results in data corruption. It's very necessary for telecommunication to reduce data corruption by providing a suitable solution to the errors occurred in the communication process. One such method that decodes the process by simultaneously correcting the process effectively is Turbo algorithm. For decoding the convolution codes Turbo algorithm is the highest recognizable algorithm. This algorithm may be described with software as well as hardware implementations. To engage well organized communications efficient data is presented by the digital systems. Data corruption is the important issue confronted by the digital communication systems. To decrease data corruptions error correcting codes is the best technique. Al most all communication systems followed it because it's power to decode efficiently, even Turbo algorithm needs very typical hardware. While the decoding operation is in advance, the functioning obstructions can be eliminated, so that an improved method, Adaptive Turbo Algorithm is used. The decoding of codes can be done very fast, as this algorithm is very effective in high-speed functions. Convolution codes are used to gain possible code sequences AVA uses maximum – likelihood decoding process. This research mainly centers on the grandness of Turbo algorithm in the practical applications with the VHDL code. This research not only helps the students related to the communications, but it also helps the people who are in the field of decoders as it is one of the efficient methods for reducing the errors while communication procedure is in advance. Here, VHDL code is used to implement the Turbo algorithm in a proper way. Apart from various codes, researcher selected VHDL code for this research as it offers the high capability in designing the electronic systems. Apart from students and the businesspeople, one can easily understand and analyze the Turbo algorithm concepts and can gain more knowledge on the VHDL code and the tools that are

used in this research.

2.Literature survey

Akshaya, V., K. N. Sreehari, and Anu Chalil (2020)[1], proposed a Very Large Scale Integration (VLSI) architecture for the implementation of Turbo decoder. Soft-in-soft out decoders, interleavers and deinterleavers is used in the decoder side which employs Maximum-a-Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this paper uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. The Turbo encoding and decoding is done using Octave, Xilinx Vivado, Cadence tools. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC).Timing analysis has been done and GDSII file has been generated.Zhan, Ming (2021)[2], proposed a reverse calculation based low memory turbo decoder architecture by partitioning the trellis diagram and simplifying the max* operator. The designed forward state metrics calculation architecture is merged with two classical decoding schemes. Through field programmable gate array (FPGA) hardware implementation, the state metrics cache (SMC) capacity is reduced by 65%, the power dissipation of the reverse calculation architecture is significantly reduced for all tested clock frequencies, and the decoding performance is not affected as compared with classical decoding schemes. The proposed reverse calculation architecture is an effective technique to achieve better decoding performance for power-constrained applications.

Kumar, N.Sai Vamsi and G.Lakshmi Bharath (2020)[3], designed and implemented Turbo encoder to be an embedded module in the in-vehicle system (IVS) chip. Field programmable gate array (FPGA) is employed to develop the Turbo encoder module. Both serial and parallel computations for the encoding technique are studied. The two design methods are presented and analyzed. Developing the parallel computation method, it is shown that both chip size and processing time are improved. The logic utilization is enhanced by 73% and the processing time is reduced by 58%. The Turbo encoder module is designed, simulated, and synthesized using Xilinx tools. Xilinx Zynq-7000 is employed as an FPGA device to implement the developed module. The Turbo encoder module is designed to be a part of the IVS chip on a single programmable device. Weith offer, Stefan (2020)[4], presented recent findings on the implementation of ultra-high throughput Turbo decoders. They illustrated how functional parallelization at the iteration level can achieve a throughput of several hundred Gb/s in 28 nm technology. Our results show that, by spatially parallelizing the half-iteration stages of fully pipelined iteration unrolled decoders into X-windows of size 32, an area reduction of 40% can be achieved. We further evaluate the area savings through further reduction of the X-window size. Lastly, we show how the area complexity and the throughput of the fully pipelined iteration unrolled architecture scale to larger frame sizes. They considered the same target bit error rate performance for all frame sizes and highlight the direct correlation to area consumption.

Paidmalla, Nagaraju, and Tummapala Lalitha Prasanna (2021) [5], designed and evaluated of area efficient pipelined turbo encoder and decoder is implemented. Turbo coding is very effective technique for correcting errors. These codes widely used in communication systems. Wireless communications (3G & 4G) includes turbo codes within it for accurate error correction. Earlier, the polar codes are implemented using 8 bits, so polar decoder is restricted by the inherent iterative process to compile the data at a higher rate. High decoding accuracy is the major flaw of polar coding implementation. Hence in this work, implementing 64-bit turbo encoder and decoder to compile the data at higher rate with reduced area and delay. The system is implemented and correlated in Application Specific Integrated Circuit (ASIC). At last compared with existed system, proposed system gives effective outcome in terms of delay and area.Rangachari, Sundarrajan, and Nitin Chandrachoodan (2020) [6], proposed a new state encoding mechanism as well as an organization of memory blocks that enables this power reduction, and quantify the effects. When combined with other schemes for early termination, the overall energy consumed per decoding

operation can be reduced by between 10-20%.

Ali, Amer T., and Dhafir Abdul Fatah Alneema (2020) [7] , proposed a new design of turbo decoder with one MAP decoder and it was designed with and without parallelism using different window technique in HLS tool which it is not explored previously. These designs were implemented for different frame size in this work. A comp-arison in latency and resource utilization where done and how a tradeoff done between these two parameters to reach the specific design that we need. The new design produces better results.Shrimali, Yanita, and Janki Ballabh Sharma (2021) [8] , proposed architecture, in order to achieve high throughput and low complexity, efficient Log-MAP turbo encoder/decoder and pipelined FFT processor is employed. Single delay feedback-based pipelined memoryless FFT/IFFT processor helps in achieving improved area and power efficiency, whereas high speed and good error correction capacity are obtained by Log-MAP turbo decoder. Simulation results obtained using Xilinx ISE Design suite are compared with state of the art architectures verifies the efficiency of the proposed system.Verma, Anuj, and Rahul Shrestha (2020) [9], proposed VLSI architecture of LDPC decoder processes quasi-cyclic LDPC encoded information which is received as log-likelihood ratios (LLRs) from soft demodulator at the receiver side. It achieved the adequate bit-error-rate (BER) of 10−6 between 2 to 4 dB of bit-energy to noise-power-spectral-density (Eb/N0) with 10 decoding iterations for various code rates like 1/3, 2/5, 1/2, 2/3, 3/4, 5/6, and 8/9. The VLSI architecture of 5G new-radio LDPC decoder has been field-programmable logic-array (FPGA) prototyped and its implementation results are compared with state-of the-art designs where the proposed LDPC decoder shows lower hardware utilization up to 87%. To the best of our knowledge, this is the first VLSI-architecture of LDPC decoder reported for 5G new-radio compliant to the specifications of enhanced mobile broadband (eMBB).

Le Gal, Bertrand, and Christophe Jego (2020) [10] , a new turbo decoder parallelization approach is proposed for x86 multi-core processors. It provides both: high-throughput and low-latency performances. In comparison with all CPU- and GPU-related works, the following results are observed: shorter processing latency, higher throughput, and lower energy consumption. Regarding to the best state-of-the-art x86 software implementations, 1.5 × to 2 × throughput improvements are reached, whereas a latency reduction of 50 × and an energy reduction of 2 × are observed.Dheeb, Khadija Omran, and Bayan Sabbar (2020) [11], presented an implementation of LTE turbo decoding using the Log- Maximum a posteriori (MAP) algorithm with reduced number of required cycles approximately by 75% based on serial to parallel operation. Additionally, an improvement for this algorithm based on polynomial regression function is done to reduce the implementation complexity. These system implementations, are designed with 40 bit block size of the input using Xilinx System Generator (XSG) to show its applicability in real time using two approaches; Hardware Co-Simulation and HDL Netlist based on three devices, Xilinx Kintex- 7, Spartan- 6 and Artix-7.Boudaoud, Abdelghani, Mustapha El Haroussi, and Elhassane Abdelmounim (2020) [12], presented the contribution of the insertion of a Turbo-type channel decoder in a MIMO chain. This MIMO chain is based on Orthogonal Space-Time Block Code (OSTBC). Alamouti proposed two structures, based on the OSTBC code and having two transmitting antennas: the first structure has a single receiving antenna, that is OSTBC 2 × 1 and the second one has two receiving antennas that is OSTBC 2 × 2. The turbo-decoder is based on the Difference Set Codes-One Step Majority Logic Decodable (DSC-OSMLD); it is the DSC (21, 11) code. After the introduction of this turbo decoder in the two Alamouti's structures, performance are noted and compared in terms of the Bit Error Rate (BER) versus the Signal-to-Noise Ratio (SNR). The obtained results show that the addition of a one receiving antenna to the 2 × 1 OSTBC structure provides a decoding gain equal to 1 dB, while the insertion of the proposed turbo decoder brings a gain of 5.5 dB at the first iteration only.

Joseph, Senoj, R. Kirubakkar, and M. Mariammal (2021) [13], demonstrated An error could have occurred at the recipient end around a communication system once text is read from intermediate nodes. The Turbo Coder is used to get the originally transmitted data. Turbo code is an error - correcting code which now, when compared to some of the other error correction codes, has such a

high error correction rate. The Turbo code is used in many different fields. NASA uses them for its communication with space. It has an encoder including a decoder. Two Recursive Convolutional Encoders and an Interleaver create the encoder. Salija, P(2020) [14], proposed A novel reliability-based turbo decoding algorithm that addresses the performance improvement of short block length turbo codes. Simulation results show a coding gain of 2.45 dB at BER of 10−3 for short length codewords. The proposed decoding algorithm has low computational complexity compared to the conventional iterative decoding algorithm. The relatively lower computational complexity and the conspicuous improvement in BER performance make the method quite attractive.Le, Vinh Hoang Son (2020) [15], proposed a new soft-input soft-output decoding algorithm particularly suited for low-complexity high-radix turbo decoding, called local soft-output Viterbi algorithm (local SOVA). The local SOVA uses the forward and backward state metric recursions just as the conventional Max-Log-MAP algorithm does and produces soft outputs using the SOVA update rules. The proposed local SOVA exhibits a lower computational complexity than the Max-Log-MAP algorithm when employed for high-radix decoding to increase throughput, while having the same error correction performance even when used in a turbo decoding process.

3. Proposed methodology

Architecture of Turbo Coder Turbo encoder and decoder together comprises the Turbo coder architecture as shown in Figure 1. Two identical Majority Logic Based Recursive convolutional encoders (ML-RSC) and a pseudorandom interleaver constitute the turbo encoder as shown in Figure 2. The LTE employs a 1/3 rate parallel concatenated turbo code. Each ML-RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The ML-RSC1 and ML-RSC2 encoder outputs along with systematic input comprise the output of turbo encoder, that is, a 24-bit output is generated. This will be transmitted through the channel to the Turbo decoder.

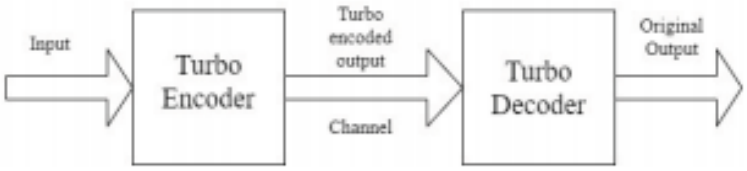

Figure 1 Proposed block diagram.

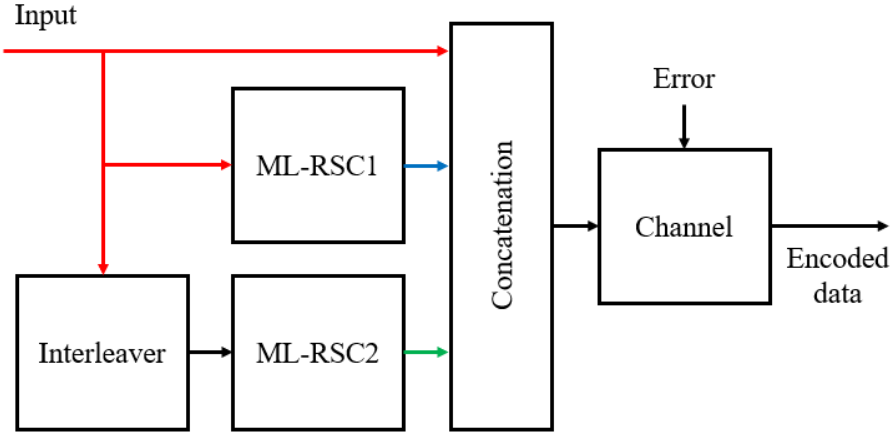

Figure 2. Turbo encoder operation.

A standard turbo decoder block diagram is shown in Figure 3 that contains two modules of TE-NCN decoders together with two pseudorandom interleavers and a pseudorandom deinterleaver. The usually used method of turbo code decoding is carried out using the BCJR algorithm. The

fundamental and basic idea behind the turbo decoding algorithm is the iteration between the two TE-NCN part decoders which is illustrated in Figure 3. It comprises a pair of decoders, those which work simultaneously to refine and upgrade the estimate of the original information bits. The first and second TE-NCN decoder, respectively, decodes the convolutional code generated by the first or second CE. A turbo-iteration corresponds to one pass of the first component decoder which is followed by a pass of the second component decoder.

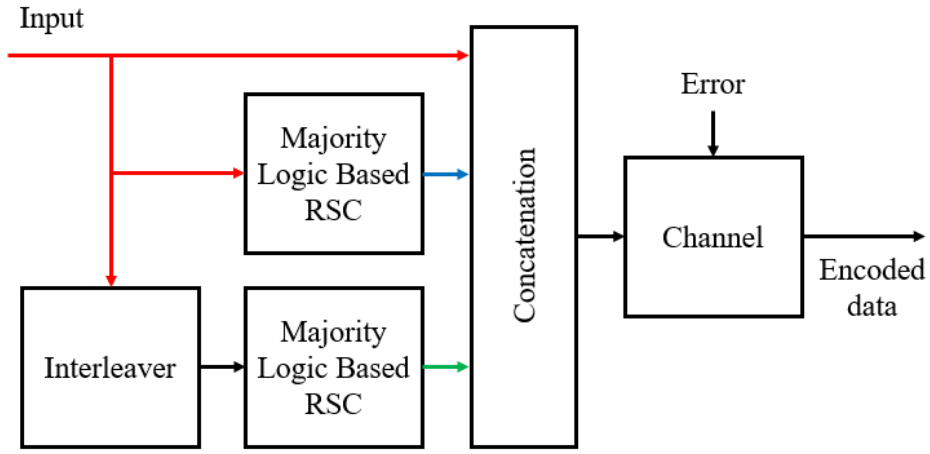

Figure 3. Turbo Decoder Block diagram

3.1 TE-NCN Decoder

The signal which is received at the input of TE-NCN decoder is the real (soft)value of that signal. An estimate of each input bit The decoder then generates an approximation for each data bit expressing the probability that the transmitted data bit is equal to one. The maximum a-posteriori (MAP) algorithm is used in the turbo-decoder under consideration in this paper for the TE-NCN component decoder. The MAP algorithm never restricts the set of bit estimates to correspond strictly to a valid path through the trellis. Therefore, the results produced by a Viterbi decoder that recognizes the most likely true path through the trellis should differ from those generated by that. 1) The MAP Algorithm: The MAP algorithm minimizes the likelihood of bit error by using the entire sequence that was obtained to figure out the most likely bit at each trellis point. Consider a frame of N coded symbols consisting of m bits and the channel output received by the decoder as y. For every dsym i, a MAP decoder provides a 2m a posteriori probability.

3.2 Interleaver

Choosing the interleaver is a significant part of the turbo code design. Interleavers scramble data in a pseudorandom order to lessen the resemblance between adjacent bits at the input of the convolutional encoder. The interleaver is shown in Figure 4 is used on both the encoder part and the decoder part. It produces a long block of data on the encoder side, while it compares two TE-NCN decoders' output in the decoder portion and helps to fix the error. Pseudo-random deinterleaver functions in a complimentary manner of pseudo-random interleaver.

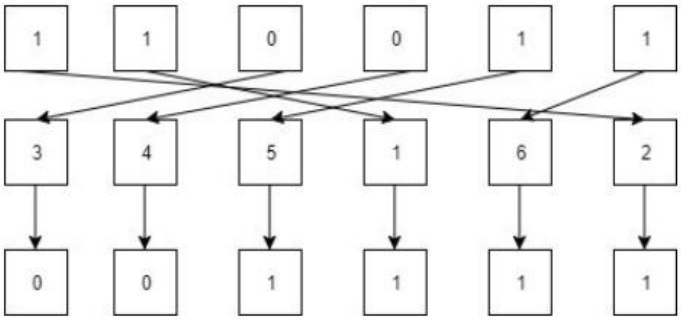

Figure 4. interleaver block diagram.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 3, No. 1, March : 2024

4. Results and discussion

The simulation results will do by using in Xilinx ISE. The timing, power and synthesis reports are listed below.

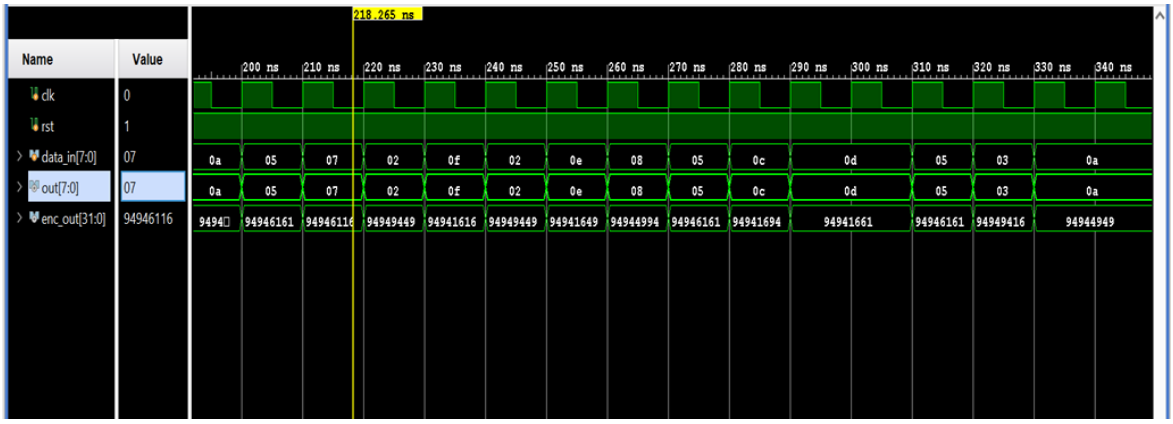

Figure 5. Simulation outcome

Resource	Utilization	Available	Utilization %
LUT	12	101400	0.01
IO	48	285	16.84

Figure 6 Design summary.

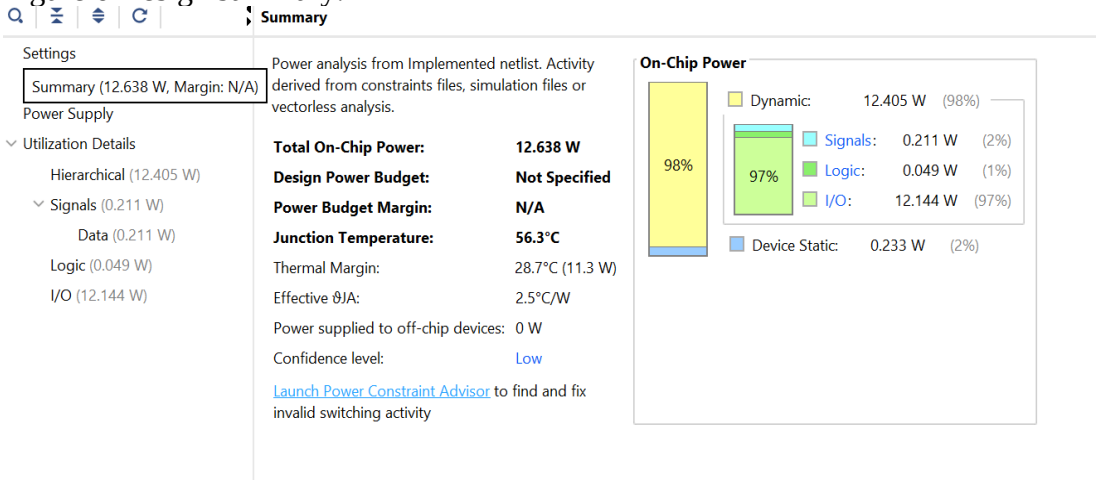

Figure 7. Power summary

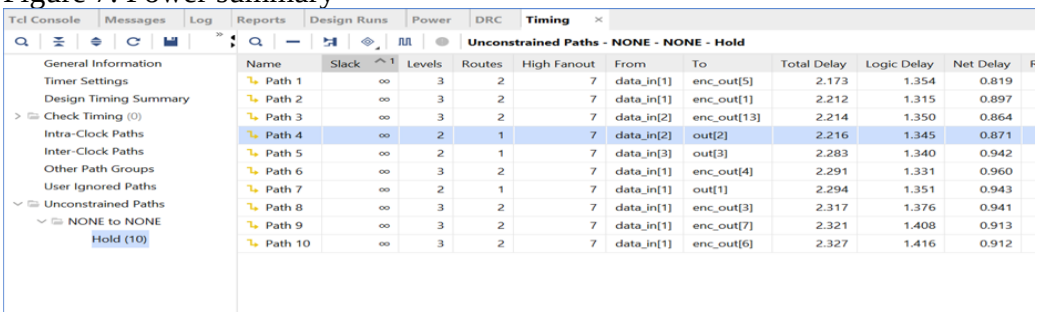

Figure 8. Time summary**.**

5.Conclusion

Turbo algorithm is conceived more interesting and challenging for this research topic, it is considered, and it has wide variety of applications in digital communications field. This research helps to generate more profits by the developers using Turbo algorithm. Anyone besides students can

easily analyze these Turbo algorithm concepts and can gain more knowledge about it. This research mainly concerned with implementation of Turbo algorithm using Verilog coding. Turbo algorithm has many advantages like low power consumption and main advantage is error correcting using Verilog. The main advantage of Turbo algorithm is the description will be low even in the presence of more errors and the algorithm works more effectively. Another advantage of using this Turbo algorithm is due to its cost effectiveness.

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