Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 3, March : 2023

DESIGNANDIMPLEMENTATIONOFADVANCEDTRAFFICLIGHTCONTROLLERSYSTEMUSINGFPGA

[1]Pamula Syam, [2]V.Maaduri, [3] Dr.G.Jagadeswar Reddy, [4]Dibbalakati Ramesh
[1,2,3]Assistant Professor, [4]Student, Dept. of Electronics & Communication Engineering,
Newton's Institute of Engineering, Macherla, Andhra Pradesh, India.

Abstract
The purpose of the article is to suggest ways to reduce traffic congestion and vehicle wait times at traffic signals. Road congestion, particularly in contemporary cities, is getting worse every day due to an increase in the number of vehicles on the road.One of the drawbacks of using a microcontroller or microprocessor is that they operate on a set schedule, following a program that does not allow for real-time adjustment. The proposed system uses an FPGA and traffic sensors to control traffic according to requirements. This means that the designer can modify the program as needed, which decreases waiting times. The amount of I/O ports and performance of FPGA implementation are superior to those of ASIC and microcontrollers, and it is less expensive to implement FPGA than ASIC design.
Keywords: FPGA, Xilinx Spartan3,Traffic Light Controller, VHDL.

Introduction

Since there are more cars on the road, there is a growing daily traffic problem, particularly in urban cities.The existing traffic system's limited resources, such as its TLC microcontroller or CPU, are causing road users to travel and wait longer on average. The goal of this project's Advanced TrafficLight System is to reduce how long cars must wait at traffic signals. Fieldprogrammable gate arrays, or FPGAs, are widely employed in electrical systems to enable quick prototyping and conceptual design verification, particularly in situations where the tiny quantity of a standard IC makes its mass manufacture prohibitively expensive. Field Programmable Gate Arrays (FPGAs) are being used to execute many electronic system designs that were previously constructed in traditional silicon VLSI. This system concept minimizes waiting times for road users by employing FPGA to control traffic on four roads around-the-clock.HardwareDescription language in Verilog HDL is used to implement the design. An FPGA is an integrated circuit with a user-programmable array of identical logic cells. In every device, it offers RAM memory along with high density logic.The TLC system is coded using Verilog HDL. Because building a VHDL is challenging due to the tightly typed language that requires source code integration, Verilog HDL is utilized instead.The traffic light control system operates according to a predetermined timetable that involves precisely switching between the red, green, and yellow lights. A certain switching mechanism is used to construct this traffic light sequence, which aids in controlling the traffic light system on a road in a predetermined order.

LiteratureSurvey

An adaptive TLC that tailored the number of signals for various junctions and a user-defined number of junctions was presented by Surabhi S. et al. [9] in 2014.The proposed system prototype is made with an FPGA, and standard TLCs rely mostly on software design flow and are constructed according to the finite state paradigm. To achieve more robustness, the hardware design has been modeled utilizing the structural style of VHDL programming. The Intelligent TLC system was proposed by V. V. Dabahde et al. [10] in 2015 with the aim of reducing the time vans must wait at traffic lights. The proposed system reduces the amount of time spent waiting at a crossroads by utilizing the FPGA platform and traffic sensors to regulate traffic according to traffic flow. ALTERA Cyclone II-FPGA has been used to implement and test the system in hardware with good results.The system is far more advantageous than the thrilling TLC. Using VHDL and FPGA, Ali Kareem Abdulrazzaq [11] created an intelligent TLC system in 2016. Moreover, consideration

has been given to a number of functional levels, including the motion sensor handling section, special request implementation, standby control signal addition, and overloaded traffic design. The system function was tested and simulated using ModelSim.P. Giri Prasadetal et al. [12] created an intelligent transportation system (ITS) in 2017 and used FPGA to develop it using VHDL. It uses sensors to determine the amount of traffic on each road. Traffic on the road can be managed by controlling the signal timing using the traffic status. IR sensors were positioned at each specific intersection to determine the traffic density and provide the current traffic situation there. The system's functionality was tested and simulated using Model Sim. We suggested a smart TLC system in 2019 [13], based on the FPGA Spartan 3E, which is programmable in VHDL language.There are four different sorts of intersections that are controlled according to the type of traffic: heavy (major road) or light (side road). There is now a button for pedestrian requests and a sensor to detect traffic on the side street.Additionally, the design has controls for manual traffic light regulation.Four manually adjustable timing parameters are available for the junction controller.Using Chip-Scope and the Xilinx ISE 14.7i software environment, the system 3 has been successfully verified. Compared to other systems, the suggested method is inexpensive and easy to operate.Finally, the current paper is extended to this one.

Survey On Traffic Light Control System

Numerous citiesTraffic Light Controllers (TLCs) rely on microprocessors and microcontrollers.These TLC systems with microcontrollers and microprocessors have limitations since they rely on pre-defined hardware that follows a predetermined program and lacks real-time modification flexibility. This program is fixed; the designer cannot reprogramme or erase it.The waiting period is longer because of the set intervals between the green, orange, and red signals. If vehicles are waiting longer than the fuel loss also occurs. Because of this, we must put in place an innovative system for traffic control so that users can save time.An application-specific integrated circuit may be used to implement a traffic light controller. FPGA is less expensive than ASIC design.The majority of TLCs that have been constructed on FPGA are basic models that serve as illustrations of FSM. Both PLDs and CPLDs, or complex programmable logic devices, can be used to construct traffic light control systems. Only tiny PLDs, such as PALs and GALs, which are comparable to a hundred logic gates, are accessible. Therefore, PLDs, which result in additional cars on the road, do not regulate the traffic signal control system.

TLC systems also use Complex Programmable Logic Devices (CPLDs). CPLD with a high number of logic gatesThousands or even hundreds of thousands of logic gates can now be replaced by CPLDS. However, CPLDs are not very memory-rich. Devices with low memory require a large number of flipflops, which complicates system design. When response times for different frequencies were compared, it was found that PLD was performing twice as well as CPLD.At the nanosecond level, the reaction with regard to clock revealed that the PLD's delay response is twice as large as the CLD's delay response. If a traffic system needs to react quickly, CPLD might be the best option. However, in order to test and build more complex circuits, the CPLD is not very effective due to its small number of gates.

CPLDs offering thousands to tens of thousands of logic gates.FPGA is the ideal substitute for CPLd. While CPLD and FPGA share many characteristics, FPGA offers a greater selection of logic gates. FPGAs are often greater than CPLD, with a range of tens of thousands to several million.Fast speed, a large number of input/output ports, and performance are just a few of the many benefits that FPGA has over microcontrollers and are crucial for TLC design.FPGAs are well-known for their large volume, low cost applications and provide excellent substitutes for fixed-logic gate arrays.In addition to being extremely affordable, the FPGA incorporates numerous architectural elements linked to expensive programmable logic. These beneficial aspects, such as integrated functionality and low cost, have made FPGA an amazing offer.

Field Programmable GateArray (FPGA):

The term "field-programmable" refers to the fact that a field-programmable gate array (FPGA) is a semiconductor device that allows the designer to modify it after it is manufactured. FPGAs are programmed using a logic circuit schematic or source code written in a hardware description language (HDL). The

designer can reprogramme this software as needed.In the event that the user programs the FPGA, they can also update or modify the software. A FPGA implemented program demonstrates how the chip or kit operates. They can be used to accomplish every logical function that an ASIC (application-specific integrated circuit) is capable of, but for many applications, it is advantageous to be able to alter the functionality after shipment. Field-programmable gate arrays, or FPGAs, are widely employed in electrical systems where the mask-production of a custom integrated circuit becomes prohibitively expensive due to its tiny quantity. They are also utilized in rapid prototyping and verification of conceptual design.Spartan-3EFPGA has been used to implement the system in hardware. Fig. 1 depicts the FPGA design flow.As per that, begin with the circuit description, where every circuit is created using logic gates and Hardware Description Language (HDL). After functional description, synthesis, and post-synthesis simulation were carried out.

Following that, a time simulation is carried out, a produced file is downloaded to the target device, which in this case is an FPGA kit. Using HDLs, one can perform design or circuit description, which is then followed by functional simulation and synthesis.The target device (FPGA) downloads the generated file once the design flow is carried through to the timing simulation.Since they can be used for so many different purposes, FPGAs have become increasingly popular during the past ten years. Random logic, combining several SPLDs, device controllers, communication encoding and filtering, and small to medium-sized systems with SRAM blocks are a few examples of common uses. Prototyping concepts that are eventually realized as big arrays and the simulation of entire massive hardware systems are two more intriguing uses for FPGAs.

Verilog Hardware Description Language (HDL)

Programs for electronic chips are written in Verilog, a language for hardware description. Electronic devices that do not share the underlying architecture of a computer employ this language. Verilog is a relatively new computer language that uses C's coding conventions. Weaktyping is used in Verilog, in contrast to strongly typed languages such as VHDL.It's the delicate situation.Verilog is case sensitive; if the case used differs from what it was previously, it will not recognize the variable. Verilog is generally simpler to understand than VHDL. Part of the reason for this is that most programmers are familiar with the conventions employed in Verilog because of the widespread use of the C programming language. began as a modeling language for highly effective digital logic simulators that were event-driven.subsequently forced into service as a language definition for logic synthesis. These days, VHDL and Verilog HDL are the two most widely used languages in digital hardware design. Almost all chips, such as FPGA and ASIC, are developed partially using one of these two languages. blends behavioral and structural modeling approaches.

Xilinx

System is programmed using XilinxISE tools, and this code is dumped in an FPGA development kit using Verilog HDL. The ISE program asks you to migrate your project when you open a project file from an earlier release. The software automatically upgrades your project file to the most recent version whether you click Backup and migrate or migrate just. You are unable to open your converted project in earlier ISE software versions. You might need to update the core if your design contains IP modules that were made with Xilinx Platform Studio (XPS) or CORE Generator software and you need to make changes to these modules.However, updates are not necessary and the existing net list is used during implementation if the core net list is present and you do not need to edit the core.

Hardware Implementation

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 3, March : 2023

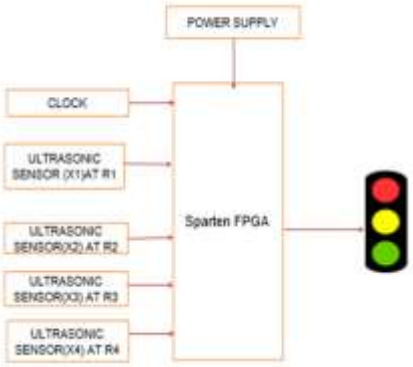


Figure.1. TLC Structure

The layout of the four roads (square) that served as the basis for the suggested system's design is depicted in Figure 2. There are four traffic signals in this structure. North Road, East Road, South Road, and West Road are the four traffic lanes that are represented by the road structure. Each road has its own unique traffic signal system, consisting of conventional yellow, green, and red lights.Light Traffic
Controller can be designed by starting withcertain assumptions. Initially Red signal is ON in NorthEast,WestandSouthdirectionis ON withGreensignal.

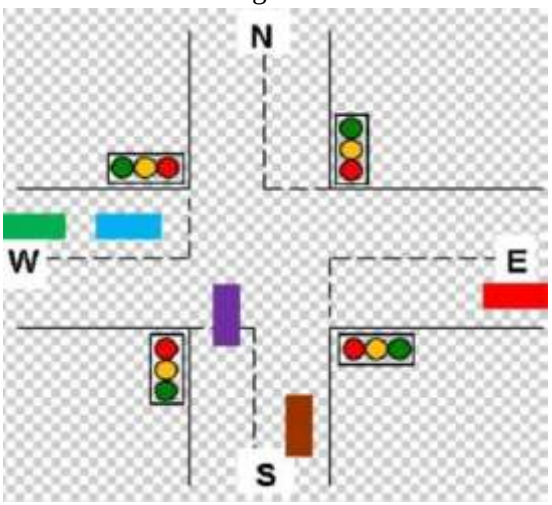


Fig.2.Fourroad structure of TLC

There are four traffic light signals, in the below figure whichare to be controlled. These four signalshavesamepriorityastheyallaremainroads.NowwhentheSensor(X3)ismadehighthesouthtrafficwill be allowed to move and traffic in all theremaining directions are stopped. Later the traffic in alltheotherdirectionisallowedtomoveinthe sequence.

State Description

The sequence of traffic is as shown in Figure4 fist North rode allow to move the traffic after that Eastrode allowtraffic to reach their place . After east South rode allowmoving the traffic on rode andthen West rode allow to movethe vehicles. The advantage of this particular Traffic LightControllerprogram is that modification can be done easilyas per the requirements i.e., suppose the traffic onmainroadandthesideroadcanbecontrolledbychangingthestatesaccordingly,whenthemainroadtraffic is heavy as compared to the side road traffic at that time the timesimulation of main road islarge than side rode means green light glowing time of main side rode is large than side rode becausenumber of vehicles are more than side rode. TheTLC states shown in Figure3 which works on thechangingofthesensorinputs.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 3, March : 2023

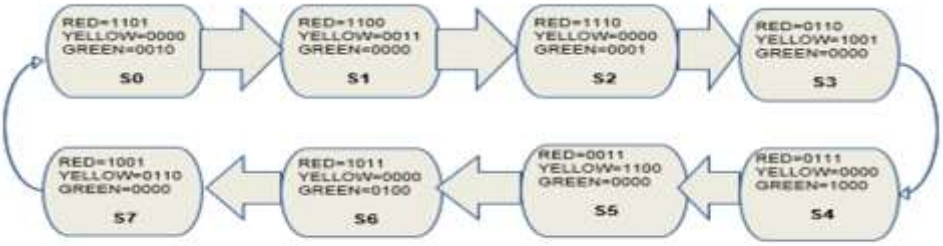


Fig 3.State diagram of TLC

Initially green light in south direction will be ON for fewseconds and red signal light in all otherdirectionsnamelywest,northandeastwillbeON.Whenthesensorsatroad3i.eX3=1thesouthroadis still with green signal and whenever the sensors senses no traffic i.e, X3=0 then the state goes tonext state which is state S0 to S1. The nextroad 4 i.e west gets the next priority and hence the signalat west and south turns to yellow indicating the change in the state from S1 to S2 and the remainingroadsarestillleftwithredsignals.NowagainthesensorX4=1thewestroadindicatesthetrafficthenthegreen signalispresentinwestandtherestoftheroadsareredonly.IfsensorX4=0thenitchangestonext state.HerethestatechangesfromS2to S3.Thenextroad4i.enorthgetsthenext priorityandhence the signal at west and north turns to yellow indicating the change in the state S3 to S4 and theremaining roads are still left with red signals. Now again the sensor X1=1 the north road indicates thetraffic then the green signal is present in north and the rest of the roads are red only. Ifsensor X1=0then it changes to next state. Here the state changes from S4 to S5. The nextroad 4 i.e east gets thenext priority and hence the signal at east and north turns to yellow indicating the change in the stateS5 to S6 and the remaining roads are still left with red signals.Now again the sensor X2=1 the eastroad indicates the traffic then the green signal is present in east and the rest of the roads are red only.Ifsensor X4=0 then it changes to next state. Here the state changes from S6 to S7. This sequencerepeatsandthetrafficflowwillbecontrolledbyassigning timeperiodsinallthefourdirections.

Simulation Results

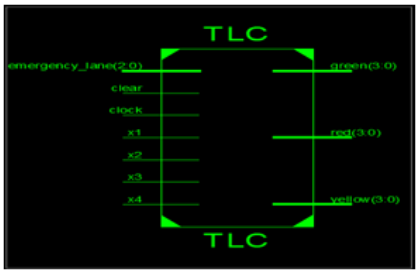
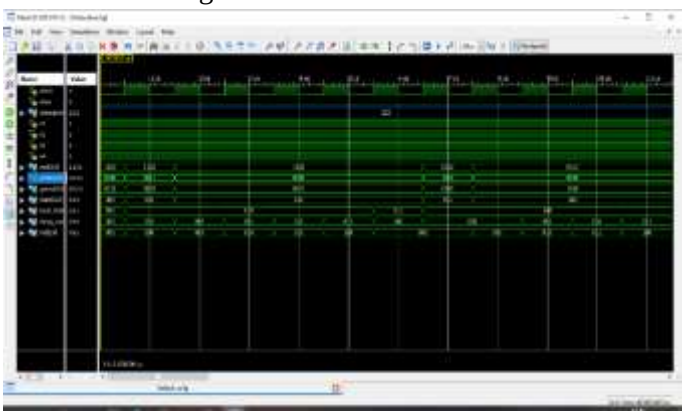


Fig5.RTL schematic of TLC



Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 3, March : 2023

Fig.6.when applying only sensor and clock, clear input value

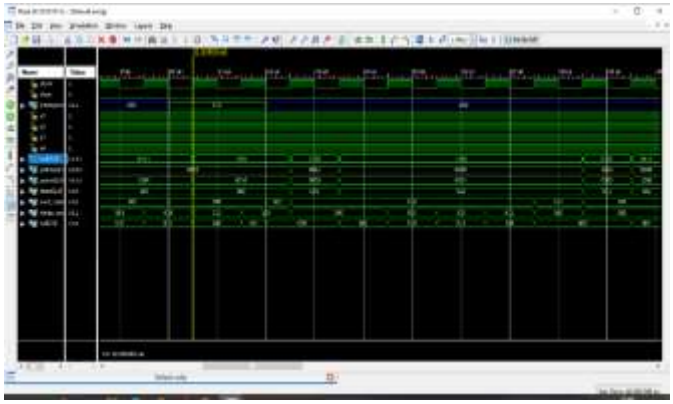


Fig. 7. By applyin gemergency lane value input with remaining inputs

Conclusion

The suggested solution uses an advanced traffic light control system to manage complex traffic in contemporary cities. Because this system makes use of FPGA, it is advanced. FPGA is a device that the user or designer can modify. The ability for designers to easily reprogramme the program at any time is a highly useful application of FPGA.The user can alter the application to suit their needs. Code is generated and circuit descriptions are done using Verilog HDL. Traffic-related issues are becoming increasingly significant nowadays, as a result of which the number of accidents in modern cities is rising quickly.Road users lose crucial time due to inadequate management in the TLC system.To address these drawbacks, we require a somewhat sophisticated TLC system. FPGA is a great substitute for the conventional TLC systems that used microcontrollers with set timing intervals. This FPGA-equipped four-rode TLC structure can handle any traffic-related complexity. Compared to microcontroller and ASIC designs, FPGA has various advantages, including lower costs.

References

1. ParagBurhade,Shubbam sonar, Onkarkulkarani Implementation of advanced traffic light ontrolsystemusingFPGA.April2020IJIRTVolume11ISSIN:2349-6002.Wayne Wolf,FPGA-BasedSystemDesign,PrenticeHall,2005.
2. Taehee Han; Chiho Lin, “Design of an intelligence traffic lightcontroller (ITLC) with VHDL”,Proceedings2002IEEERegion10.
3. M. Vreeken, J. van Veenen, J. A. Koopman, “Simulation and optimization of traffic in a city”,IEEEWieringIntelligentVehiclesSymposium,14-17June 2004,pp.453–458.
4. Malik J. Ojha, “Design of a VLSI FPGA integrated circuit”, Dept. of Eng., Denver Univ., CO,USA, Technical, Professional and Student Development Workshop, 2005 IEEE Region 5 and IEEE aDenverSection,7-8April2005.
5. A. Raza, A. Kumar, E. Chaudhary, “Traffic Light Controller Using VHDL”, International JournalofModernTrendsinEngineering and Research(IJMTER),Vol.04,Issue4,PP.57-62,April2017.
6. T. Royani, J. Haddadnia, M. Alipoor, “Control of Traffic Light in Isolated Intersections UsingFuzzy Neural Network and Genetic Algorithm”, International Journal of Computer and ElectricalEngineering,Vol.5,No.1,PP.142-146,Feb.2013.