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DESIGN AND IMPLEMENTATION OF HIGH SPEED AND LOW AREA QCA BASED SERIAL PARALLEL MULTIPLIER

[1]Mrs. D. Suvarna Kumari,[2]Anumalisetty Shanmukhi Satyaveni, [3] Bugata Sandhya Rani, [4] Dasari Poorna Chandrika,
[1]Assistant Professor, [2,3,4,5] B.Tech,[1,2,3,4,5]Department of Electronics and Communication Engineering, Vignan's Institute of Engineering for Women, Duvvada, Visakhapatnam, India

ABSTRACT
This paper unveils a unique and groundbreaking design of a serial-parallel multiplier utilizing Quantum-dot Cellular Automata (QCA) technology. The plan put forth upholds a harmonious blend of serial and parallel processing techniques to achieve efficient multiplication operations. Introducing an innovative 4-bit Serial parallel multiplier framework, consisting of an excessive 229 QCA cells. The expansion leads to an 8-bit Serial parallel multiplier configuration with a whopping 470 QCA cells using XOR gate and a bit-serial adder. Leveraging the exceptional attributes of QCA, such as its high-speed and low-power features, to obtain compactness and efficiency in execution. Extensive performance scrutiny illustrates the effectiveness of this design in offering high-speed multiplication operations while keeping power consumption as well as energy dissipation at a minimum. The scalability of this design renders it suitable for incorporation into larger systems, catering to a variety of computing applications demanding effective multiplication capabilities.

Keywords:
Serial-parallel multiplier(SPM), XOR gate, bit-serial adder(BSA), QCADesigner.

INTRODUCTION
Quantum dot cellular automata (QCA) is a promising nanotechnology for computing, based on quantum dots – tiny semiconductor particles. QCA leverages the quantum properties of these dots to perform computations, potentially enabling faster and more energy-efficient electronics compared to traditional CMOS technology. With its potential for high-density, low-power computing, QCA has garnered significant interest for applications in areas like data storage, cryptography, and beyond.

The fundamental piece of QCA tech is a QCA cell, a square nanostructure stuffed with four quantum dots, and a pair of movable electrons, who have the capability to switch their position between dots. Because of Coulomb interaction, electrons encounter mutual repulsion and positioned diagonally from each other. More strictly, an individual cell must be in any of the two energy states, called cell polarization and represented as P = +1(binary 1) and P= -1(binary 0)[1],[2]. Besides, in order to execute logical operations and signal propagation, semiconductor QCAs have four-phases of clocking schemes with a 90° phase shift to each other [3].

QCA technology not only offers a novel designing pragmatic but also facilitates a revolutionary computing architecture. Up-to-dates, several elementary logic gates have been successfully fabricated and tested [4][5]. Moreover, some complex designs including memory unit [6], arithmetic logic unit (ALU) [7], [8] and microprocessor [9] have been reported. However, the physical implementation of such design is not still possible because of the complex structural trade-off. More precisely, multilayer design has significant geometric complexity in terms of physical implementation. So, single-layered majority gate is designed and is considered as the best for physical implementation [10].

LITERATURE SURVEY
[1] Binfeng Yang and Sonia Afrooz, A New Coplanar Design of Multiplier Based on Nanoscale Quantum-Dot Cellular Automata. 2019. A new 2 × 2 array multiplier circuit in QCA by employing an efficient structure of full adder is designed and implemented. The simulation results have demonstrated that the 2 × 2 multiplier leads to less cell count and area as the prime designing factors.

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Summary: From this journal, I have considered that the concept of QCA array multiplier consists of 493 cells and 0.72 μm², area which requires more number of cells.

[2] Iman Edrisi Arani and Abdalhossein Rezai, Novel circuit design of serial parallel multiplier in quantum-dot cellular automata technology.2018. A novel serial-parallel QCA multiplier circuit is evaluated which is efficiently designed based on full-adder circuit and simulation results are observed. Summary: From this journal article, it is observed that 4-bit SPM utilizes 264 cells with occupancy 0.27 μm², area. This design is Computationally expensive.

[3] K Raja Sekar, R Marshal and G Lakshminarayanan, High speed Serial parallel multiplier in Quantum-Dot Cellular Automata. 2022. SPM is an efficient circuit used in multiple applications. It has efficient clocking scheme designed without using shift registers is analyzed. Summary: From this article, 4-bit SPM consists of 237 cells with area occupancy of 0.23 μm², but, for this design there is no provision to store input and output.

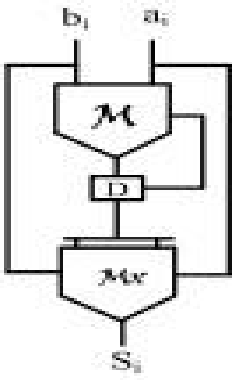
[4] Ali Newaz Bahar and Khan A. Wahild, Design of QCA - Serial Parallel Multiplier (QSPM) with Energy Dissipation Analysis. 2020. Here, the XOR gate is modified into E shape for better simulation results and to achieve reduced in cell count along with area. Summary: From this article, it is observed that the occupancy of 229 cells and 0.243 μm², area with increased energy dissipation and time delay.

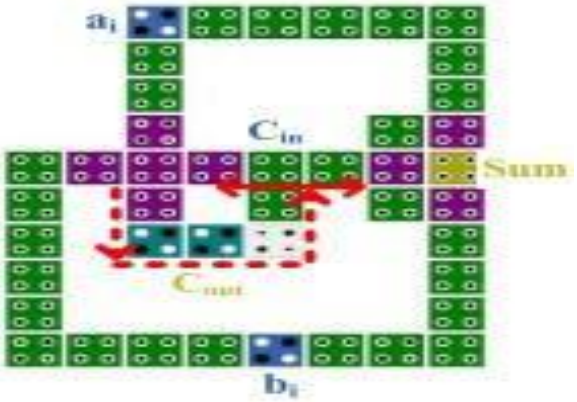
EXISTING METHOD

The four distinct clock zones within QCA cells signify the delay of the specific circuit design. Employing a 3-input XOR gate and a bit-serial adder with internally embedded Cin and Cout functions effectively reduces circuit complexity.

(a)

(b)





(c) (c)

Fig: (a) clock zones (b) 3-input XOR gate (c) schematic diagram of the bit-serial adder

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$$Sum = a_i b_i C_{in} + a_i \overline{b_i}\,\overline{C_{in}} + a_i b_i \overline{C_{in}} + \overline{a_i}\,\overline{b_i} C_{in}$$
$$= M(\overline{M}(a_i, b_i, C_{in}), M(a_i, b_i, \overline{C_{in}}), C_{in})$$

….eq(i)

$$C_{out} = M(a_i, b_i, C_{in})$$

….eq(ii)

Simulation results were thoroughly analyzed. Leveraging the XOR gate and adder.

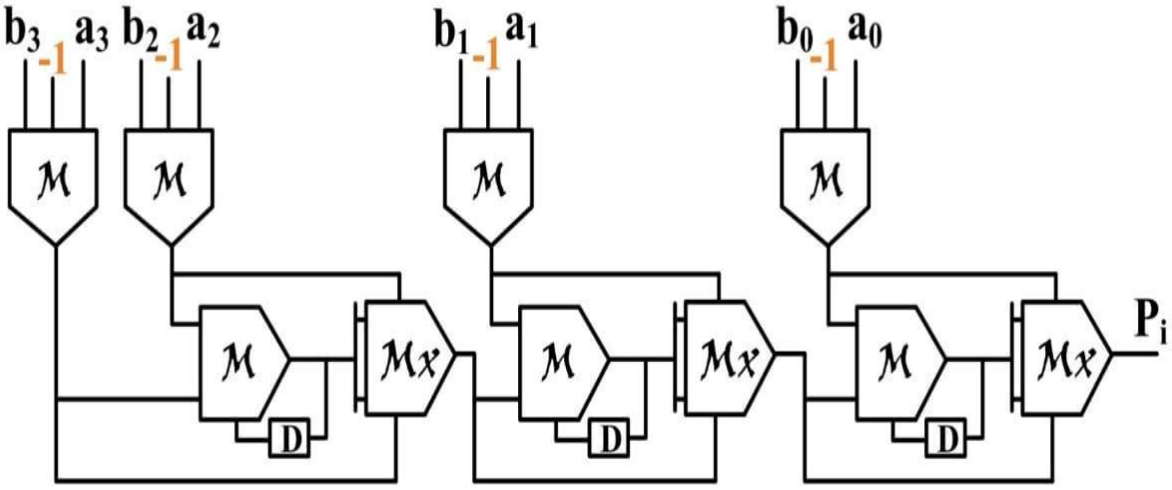

Figure.1. Schematic diagram of 4-bit SPM

In this setup, we utilize different components: M for Majority gate, Mx for Multiplexer designed with XOR gate and adder, and D for delay. The operation involves a 4-bit input represented by 'ai' and 'bi' with a polarization of '-1', executing a serial parallel multiplier operation, with the output obtained sequentially as 'Pi'.

Where, i =0,1,2,3. Hence it is a 4 bit.

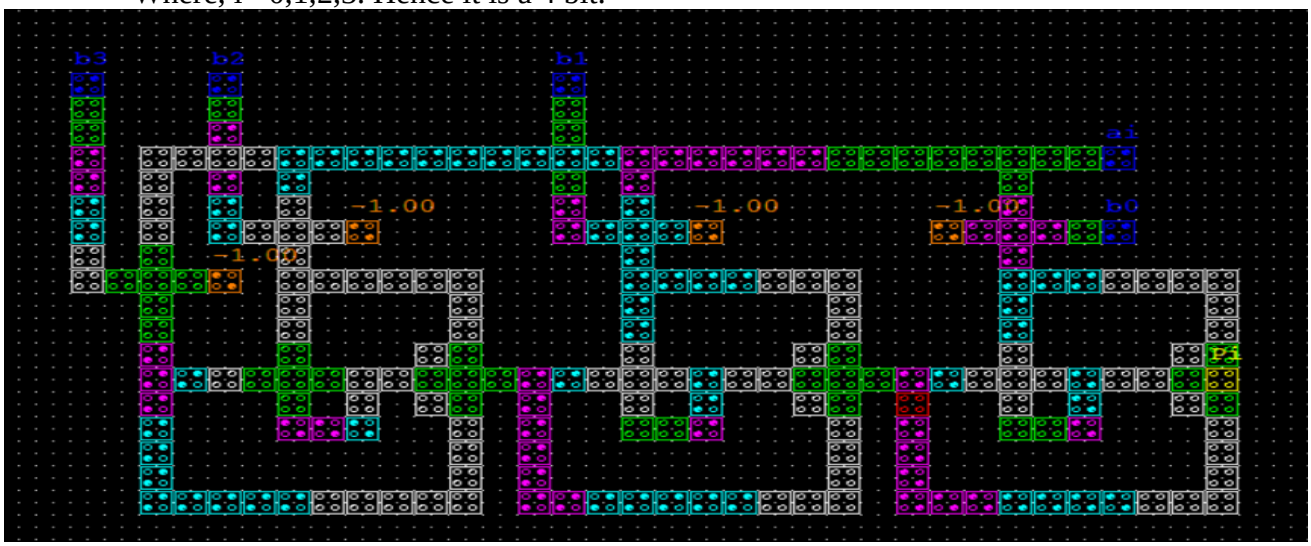

Figure.2. A 4-bit SPM QCA design

A 4-bit Serial parallel multiplier is engineered, considering parameters such as cell count, area and energy dissipation. The below figure represents the binary output of 4bit SPM.

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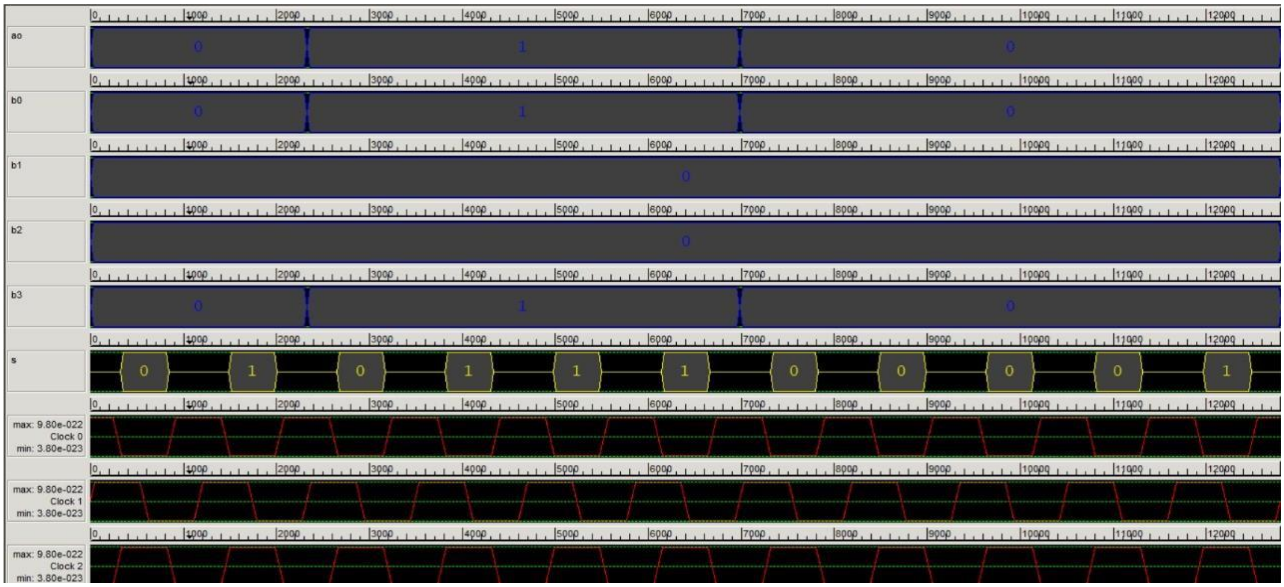

Figure.3. Simulation results of 4-bit SPM

PROPOSED METHOD

To construct the proposed multiplier network, six clock zone feedback loops are employed to internally link the carry-in and carry-out. The schematic block diagram and QCA circuit design of a 8-bit SPM are depicted, with 'a' denoting the serial input, and the serial product 'Pi' emerging after 1.25 clock cycles. In this setup, the logical "AND" operation necessitates a (D-1) clock delay, while the carry-out and sum of a full adder require only two clock zones (D-2) delay. Although wires typically don't introduce clock delays, longer wire lengths may incur some delay. Additionally, to synchronize operations, signals on the top and bottom lines are delayed by one

$$y_i = \sum_{j=0}^{n-1} b_j a_{i-j}$$

……eq(iii)

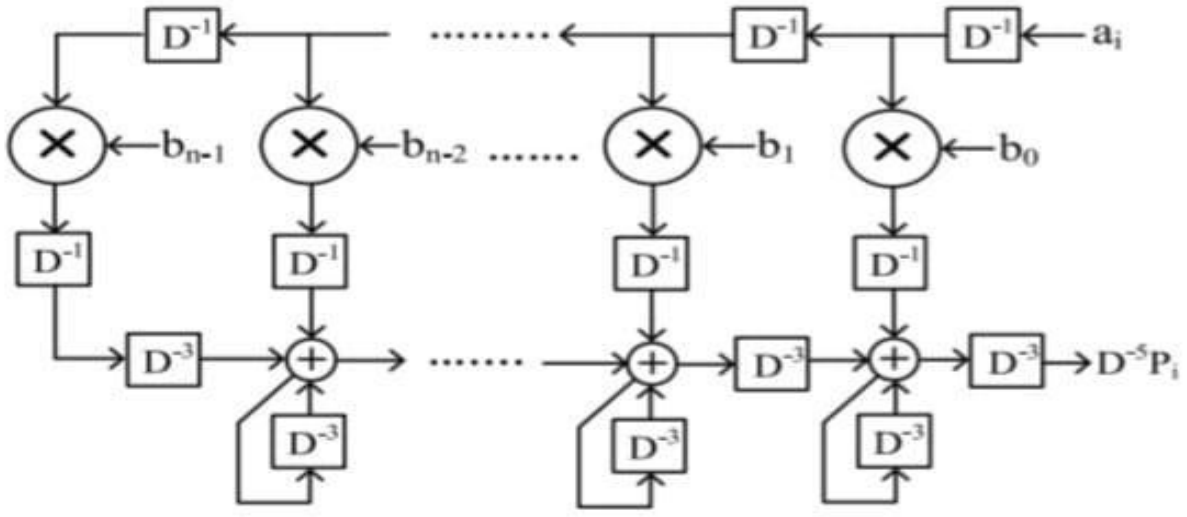

Figure.4. Proposed SPM network for QCA

clock cycle. According to the no., of bits the design increases the delays to acquire the particular simulation result accurately.

THE DESIGN STRUCTURE OF THE SPM

The design structure of an 8-bit serial-parallel multiplier employs cells distributed across four clock zones, each representing a distinct delay. These clocks cycle through four states: switch, hold, release, and relax.

During the switch state, QCA cells actively transfer charge or information, performing computational tasks such as logic gates or memory functions by manipulating quantum states. In the hold state, QCA cells maintain their current charge or information without actively transferring it, crucial for retaining data during intermediate computations. The release state involves a controlled discharge of charge or information from the QCA cell, occurring after a computational operation or as part of a data transmission process. Finally, the relax state sees the QCA cell returning to its stable or equilibrium state after completing a computational operation or releasing charge. This ensures the stability of the QCA array, preparing it for subsequent operations at the nanoscale level. QCA wire used in design process such as Low Power Consumption: Nowadays, QCA wires offer really low power consumption compare to traditional CMOS technology, making them really attractive for energy-efficient designs. They work amazingly well.

High-Speed Operation: QCA wires can operate at high speeds, enabling really rapid data transmission and processing, which is super essential for modern computing applications.

Small Size: QCA wires can be fabricated at the nanoscale, allowing for the creation of compact and densely integrated circuits. This small size is particularly advantageous for applications where space is limited, like in portable devices or embedded systems.

Parallel Processing: QCA wires enable parallel processing, where multiple operations can be performed simultaneously. This parallelism can significantly enhance the overall performance of the system, especially for tasks that involve large amounts of data processing.

Scalability: QCA wires are inherently scalable, meaning that they can be easily scaled down to smaller sizes as technology advances. This scalability ensures that QCA-based designs remain relevant and competitive in the ever-evolving field of nanoelectronics.

SPM is designed with each clock delay of 1.25 in the order of clocks zones and the output is received in a sequential manner and the simulation result is analyzed and the particular multiplication operation is performed with minimal cell count of 470 with 0.498 μm^2, area which is a efficient and less complex. Hence, the delay is reduced simultaneously with the reduction of cells.

RESULT ANALYSIS

The schematic circuits of the serial parallel multiplier discussed above are simulated in QCADesigner tool using QCA technology. The 8-bit SPM is simulated with the total simulation time 7.00e-011 sec, the clock amplitude factor 2.0, relative permittivity 12.9. The cell count, area, latency and crossover type of the different multipliers are compared for best utilization. The high-speed, low power and less energy dissipation SPM is designed and used in distinct applications.

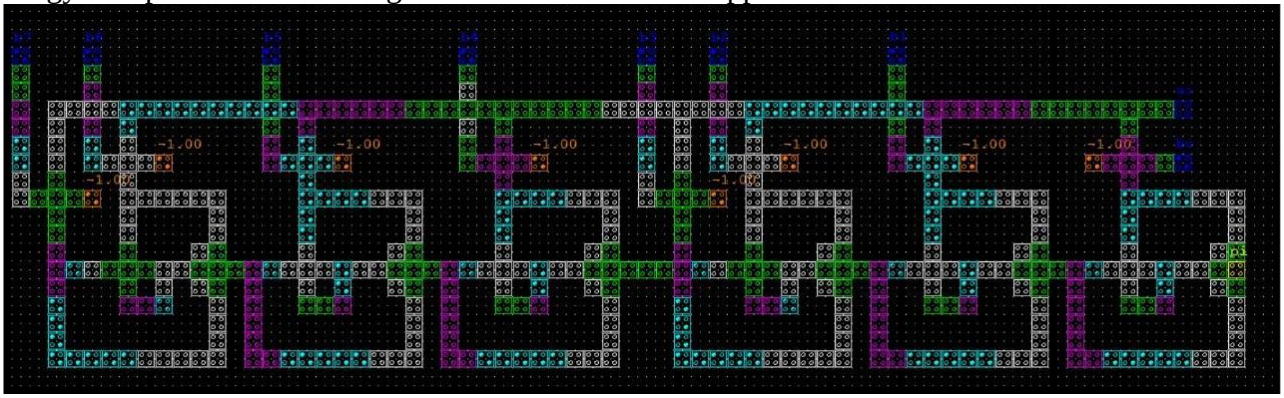

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Figure.5. Proposed 8-bit SPM

This multiplier is used in applications such as digital signal processing, image processing, cryptography, and communication systems. They are particularly useful when dealing with large numbers or complex computations where parallel processing can significantly speed up the operation.

Table.1. Simulation parameters of coherence vector engine

Parameter	Value
Cell Width	18 nm
Cell Hight	18 nm
Relative Permittivity	12.9
Clock High	9.8 e^{-22} J
Clock Low	3.8 e^{-23} J
Clock Amplitude Factor	2
Time Step	1.00 e^{-11} s
Relaxation Time	1.00 e^{-16} s
Simulation Time	80 e^{-12} s
Radius of Effect	80 nm

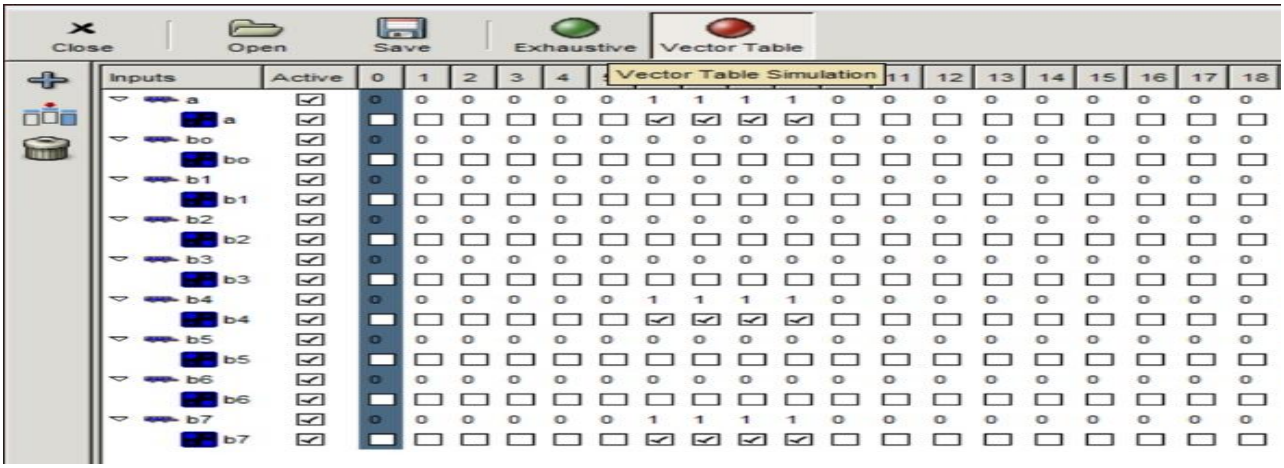

Fig:(d)

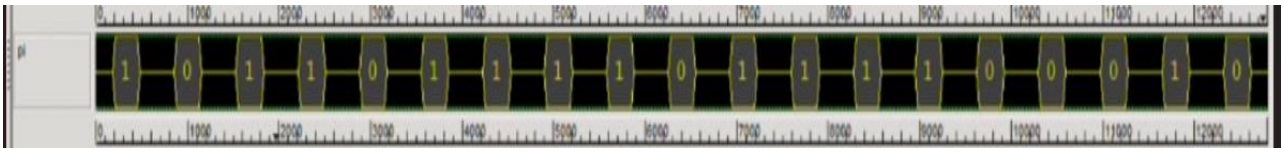

Fig:(e)

Figure: (d), (e) Represents the vector input table for 8-bit SPM and simulation result of it.

Table 2: Comparative Analysis of the proposed 8-bit SPM with others

Word	Multiplier	Cell count	Area(μm²)	Latency (clock cycle)	Crossover Type
4 - bit	Cho et al. [7]	406	0.493	1	Multilayer
	Zhang et al [8]	329	0.299	1	Multilayer
	Ali et al [1]	229	0.243	1.25	Coplanar
8-bit	Cho et al. [7]	903	0.996	1	Multilayer
	Zhang et al [8]	749	0.736	1	Multilayer
	Ali et al [1]	529	0.557	1.25	Coplanar
	Proposed	470	0.498	1.25	Coplanar

CONCLUSION

In this paper, a new expandable 8-bit SPM using XOR gate and bit-serial adder (BSA) is presented. To validate the efficiency of the proposed BSA module, various bit size multipliers have been

presented and evaluated. The simulation results show that the reported BSA and SPM operate with higher efficiency and achieved a notable improvement in terms of cell count and occupied area. In addition, the proposed SPM has 80% lower design cost over the existing design, which demonstrates the advantage of the proposed design.

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