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DESIGN AND IMPLEMENTATION OF PSHA BY USING COPFA FOR LOW- POWER APPLICATIONS IN 7-NANOMETER FINFET TECHNOLOGY

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ABSTRACT
This paper presents a comprehensive analysis of a novel carry output predictable full adder (COPFA) and a four-bit path selectable hybrid adder (PSHA) designed by FinFET 7 nm technology aimed at enhancing the performance of arithmetic circuits with improved speed and power efficiency. The COPFA introduces a predictability mechanism for the carry output, significantly optimizing carry propagation delay. When the predict bit is activated, the carry output is efficiently determined by the logical AND of input bits A and B, while accurately computing the sum. The four-bit path selectable hybrid adder integrates the COPFA, a modified full adder, and a multiplexer to dynamically choose the most efficient carry propagation path based on input conditions. This adaptability results in substantial performance improvements, making the PSHA ideal for application-specific integrated circuits and digital signal processors (DSPs). The design proves particularly beneficial for arithmetic-intensive applications such as image processing, cryptography, and network packet processing, owing to its enhanced speed and power efficiency. Simulations conducted using Microwind 3.9.4 demonstrates that the proposed COPFA and PSHA outperforms conventional methods in terms of area, power, and delay metrics. This innovative adder design represents a significant advancement in high-performance computing hardware.

Keywords: Carry output predictable full adder, Path selectable hybrid adder, Carry propagation delay, Power dissipation, Finfield-effect transistor.

I. Introduction
In contemporary digital design, prioritizing energy and power efficiency holds significant importance [1]. VLSI-based integrated circuits serve as the backbone for the majority of real-time applications found in portable and handheld devices utilized in everyday life [2,3]. Full additions represent fundamental operations utilized in implementing multi-bit adder's functions. Various designs for the full adder are developed employing CMOS technology, utilizing diverse combinations of design strategies [4]. In the realm of digital electronics and computer engineering, binary addition forms the backbone of numerous computational processes. A fundamental component facilitating this operation is the full adder, a digital circuit that computes the sum of three one-bit numbers two operand bits and a carry bit producing a sum and a carry output [5]. While the basic full adder design serves its purpose effectively, advancements in computational demands necessitate enhancements to address performance, particularly the delay associated with carry propagation [6]. Traditional full adders often struggle with these delays, impacting the overall speed of arithmetic operations, which is critical in high performance computing environments [7]. The carry output predictable full adder emerges as a pivotal innovation aimed at optimizing binary addition efficiency [8]. By incorporating mechanisms to predict the carry output based on specific conditions or input combinations, COPFA significantly mitigates the delays inherent in traditional full adder designs [9]. This predictability in the carry output not only streamlines the addition process but also elevates the overall performance of arithmetic circuits, making it exceptionally beneficial for applications where speed is of paramount importance [10]. The architecture and operational principles of the carry output predictable full adder, exploring its design intricacies and the impact on carry propagation delay reduction. Through a comprehensive analysis, we highlight the advantages of COPFA in enhancing the computational speed and efficiency

of digital systems, underscoring its potential to revolutionize arithmetic circuit performance in high-speed applications [11]. In digital electronics and computer engineering, efficient adder circuit design is crucial for computational system performance, particularly within arithmetic logic units [12, 13]. Traditional adders like ripple carry and carry-lookahead adders involve trade-offs in speed, power consumption, and complexity. The 4-bit path selectable hybrid adder mitigates these issues by dynamically selecting the optimal path for carry propagation and sum generation based on input conditions, optimizing speed and power efficiency [14]. This adder combines a modified full adder, a carry output predictable full adder and a multiplexer to handle various input scenarios, enhancing adaptability for modern digital systems. this paper explores its architecture and principles, demonstrating its potential to significantly improve computational speed and power efficiency [15].

II. Literature

Nayeri et al. [16] introduce an approximate full adder tailored for DSP applications, featuring optimized operations. A carry selection operation precedes the analysis of the final sum. Mamaghani et al. [17] introduced a radiation-hardened majority-based magnetic full adder, crafted through gate-level refinement to significantly enhance power consumption while mitigating induced noise levels. Vendhan et al. [18] presents hybrid FinFET full adder (HFFA) structures employing parallel prefix techniques. However, HFFA entails additional path delays for multi-bit additions, along with a transistor count of 16. Furthermore, a Hybrid FinFET Adder (HFA) is devised utilizing HFFA modules, resulting in increased power consumption. Bastani et al. [19] developed additionally, the imprecise minority-based CNFET full adder as a solution to the challenges posed by HFFA. Furthermore, leveraging IMC-FA modules, the imprecise minority-based CNFET Adder is also formulated.

Mahboob et al. [20] developed a CNTFET technology offering a potential reduction in power dissipation compared to FinFET, albeit susceptible to overlapping issues at the junction, leveraging ternary logic alongside CNTFET technology, the CNTFET ternary full adder is devised. Additionally, the multibit CNTFET ternary adder (CTA) is formulated, employing CTFA modules to mitigate junction overlapping concerns. Nonetheless, challenges arise concerning gate-drain synchronization within the adder architecture. Florance et al. [21] engineered the MFA and RCA employing MSL. Enhancements are imperative in the areas of area, delay, and power metrics for these tests.

III. Carry output predictable full adder design

To enhance accuracy and scalability, the carry output predictable full adder is proposed. The design of COPFA introduces a mechanism where the carry output can be predicted to optimize performance. When the predict, bit is set to 0, the COPFA operates as a standard full adder (FA), processing the inputs to produce a sum and carry output in the traditional manner. However, when the predict, bit is set to 1, the carry output (Cout) is predicted by performing a logical AND operation on the two operand bits, A and B. In this prediction mode, the sum (S) is generated accurately, while the carry output is efficiently predicted, thereby reducing the delay associated with carry propagation and enhancing the overall performance of the arithmetic circuit.

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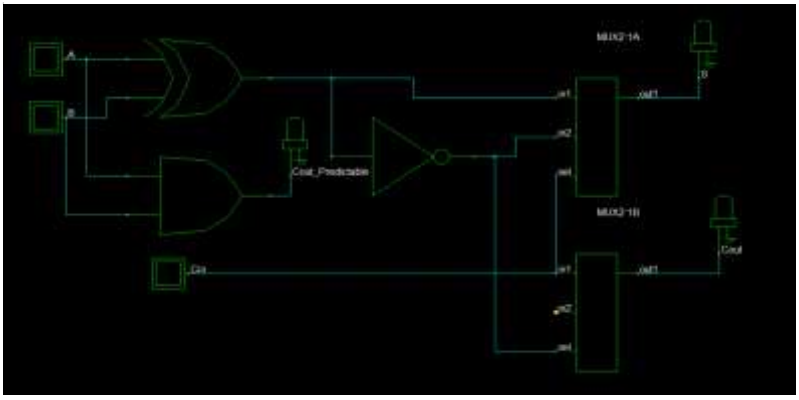

Figure1(a): Gate level figure of carry output predictable full adder

In Fig.1(a) the diagram illustrates the design of a carry output predictable full adder, which optimizes binary addition by predicting the carry output. Key components include operand bits A and B, carry input Cin, an AND gate for generating Cout_Predictable, and an OR gate for generating the sum S. A NOT gate and multiplexers (MUX2:1A and MUX2:1B) manage the selection between traditional and prediction modes. When the predict bit is 0, COPFA operates as a standard full adder; when the predict bit is 1, it predicts Cout using an AND operation on A and B, while accurately generating S. This design reduces carry propagation delay, enhancing speed and efficiency, making COPFA ideal for high-speed arithmetic operations.

3.1 Truth Table of carry output predictable full adder taken as reference

Table 1: Operational truth table of carry output predictable full adder

A	B	Cin	S(COPFA)	Cout_Predictable	Cout (COPFA)
0	0	0	0	x	0
0	0	1	1	x	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	x	1
1	1	1	1	x	1

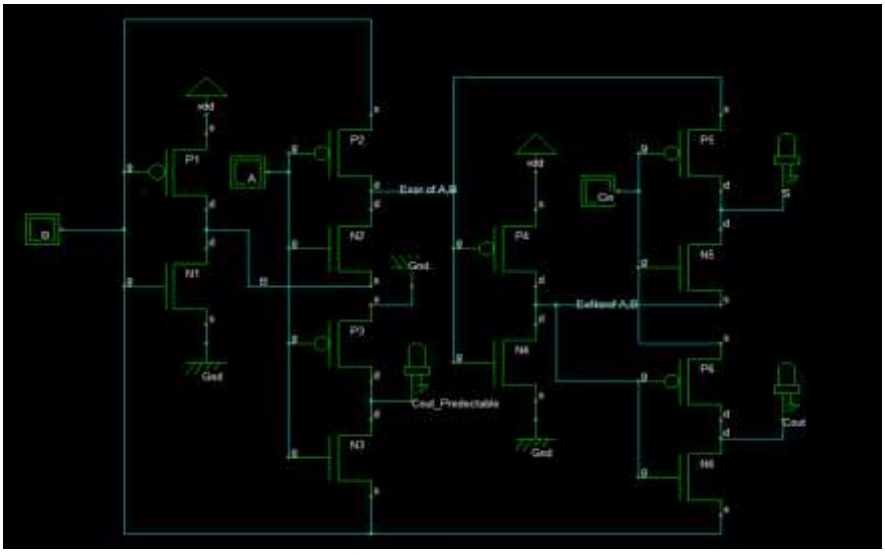

Figure 1(b): Schematic diagram of carry output predictable full adder FinFET_Circuit_7nm

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In Fig.1(b) when the A, B, and Cin inputs are binary zeros as represented in table 1, switches N1 to N5 and P6 are open, while switches P1 to P5 and N6 are closed. This configuration ensures that the LED's are off. In the schematic, a zero binary signal is applied to the gate terminal of the PMOS FinFET transistor. Since P1's source is connected to VDD = 0.8V, no charge carriers flow despite the channel being formed shown as closed, preventing signal transmission through the PMOS transistor P1. However, channels are formed in other PMOS transistors P5 and N6, allowing the binary low signal zero to pass through. This low binary signal reaches the LED's (S and Cout), but it is significantly lower than the threshold voltage required to light up the LED's, resulting in both LED's remaining off.

3.2 Backend layout of carry output predictable full adder

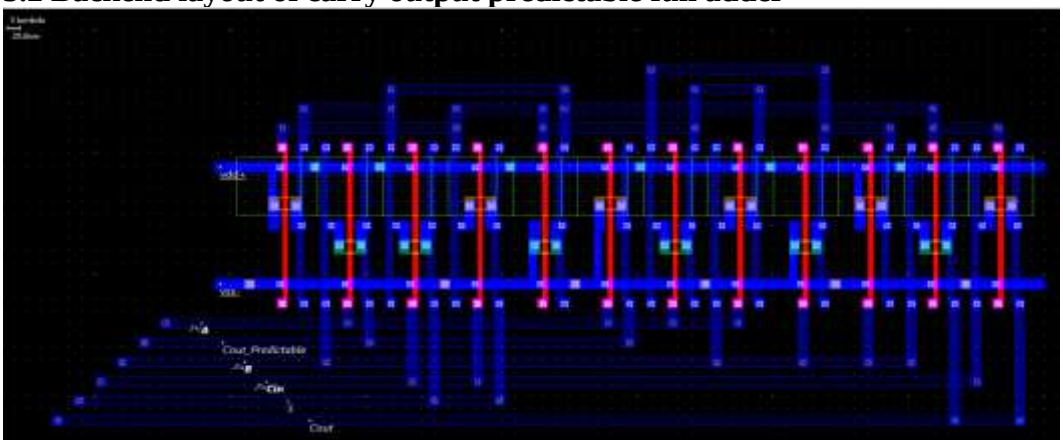

Figure 1(c): Backend layout of carry output predictable full adder

In Fig.1(c) backend layout the black background emphasizes components and connections. Blue lines represent interconnections guiding signals. Red shapes likely represent individual components or modules. Labels ("Video," "Sync," "Cout Predictable," "+5V," "-5V") provide insights into their functions. The intricate blue network enables seamless signal flow.

4.0 4-bit path selectable hybrid adder

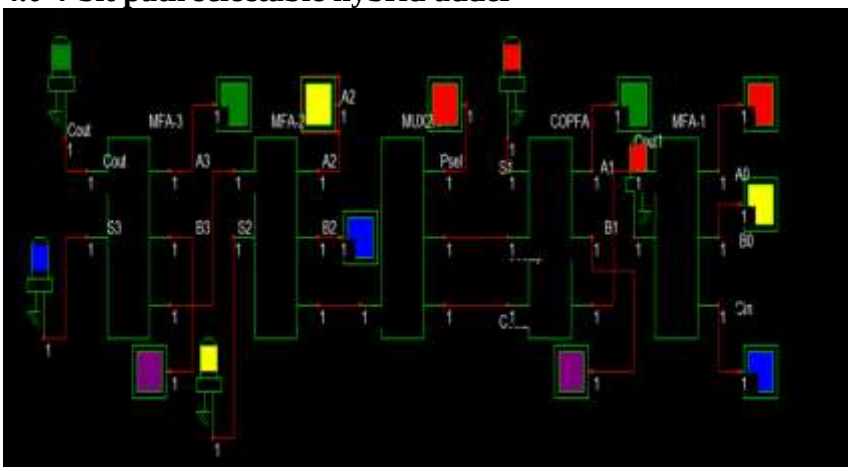

Figure 2(a): Executing truth table and observing the transistors behaviour

In Fig.2(a) the 4-bit path selectable hybrid adder is an advanced adder circuit designed to optimize performance by dynamically selecting the most efficient path for carry propagation and sum generation based on input conditions. This capability allows for enhanced speed and reduced power consumption, essential for modern computational requirements. The adder evaluates the input bits to determine whether to prioritize speed or power efficiency for the carry signal's propagation, with the selection mechanism either predefined based on conditions like the number of '1's in the input or decided

dynamically during operation. This sophisticated adder design integrates the modified full adder, carry output predictable full adder, and a multiplexer to achieve optimal performance. The accompanying schematic diagram visually represents the system using abstract symbols and lines to illustrate component connections and interactions. Key components include MFA.1 mixing component labelled MIX indicating signal combination, and COPFA 1. The term "Prdt" likely refers to a product or output of the system. When the inputs are given as high out is also high. The diagram's connections, marked by differently coloured lines (green, red, and blue), signify various signal types such as power, control, or data. Vertical lines with horizontal dashes probably indicate power sources or ground connections. Symbols such as switches (S1, S2) and connectors (A0-A3, B0-B3) suggest elements of control, signal processing, and power distribution within the system.

4.1 Backend layout of 4-bit path selectable hybrid adder

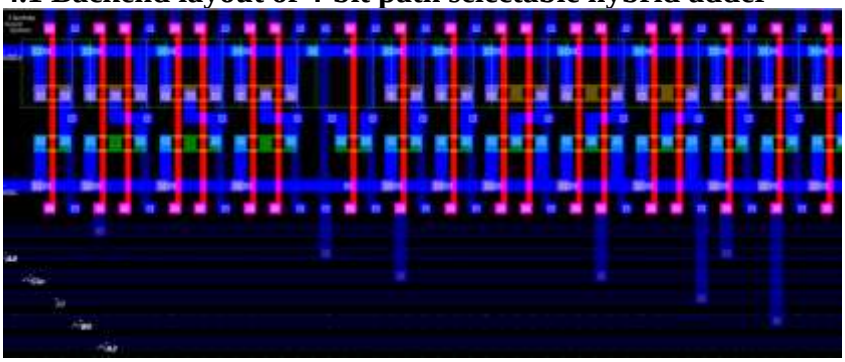

Figure 2(b): Backend layout of 4-bit Path selectable hybrid adder

In Fig.2(b) the layout diagram represents the physical implementation of a 4-bit path selectable hybrid adder, showcasing the arrangement of transistors and interconnections on an integrated circuit (IC). It includes multiple-coloured layers representing different materials used in IC fabrication, such as metal layers (blue, red, green) for routing power, signals, and ground connections, and polysilicon and diffusion regions (pink and yellow) forming MOSFETs Via (small squares/rectangles) connects different layers. Labels like A0, A2, B0, Cin, and S0 denote input and output signals of the adder circuit. The repetitive grid-like structure suggests modularity typical of adders, ensuring efficient signal routing and minimal delay. The layout integrates components like the modified full adder, carry output predictable full adder, and multiplexers, essential for the hybrid adder's dynamic path selection mechanism, providing a detailed view crucial for verifying the design before fabrication.

IV. Results

A comprehensive simulation performance study of suggested adders is presented utilizing a wide variety of parameters. In addition, to perform the proposed carry output predictable full adder and 4-bit path selectable hybrid adder is compared with the performance of traditional adders using a variety of parameters. The Microwind 3. 9.4 software tool is used in the process of designing and simulating the different designs.

4.1 Frontend timing diagram of carry output predictable full adder using 7-nm technology

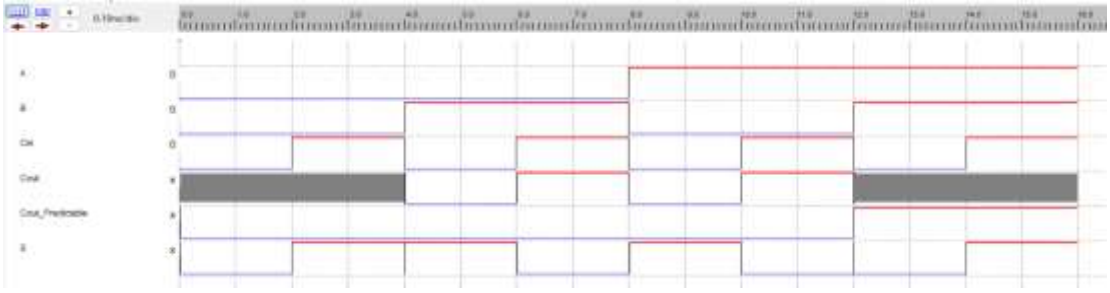

Figure 3(a): Frontend timing diagram of carry output predictable full adder using 7-nm technology

In Fig. 3(a) a timing diagram is a graphical tool that illustrates the behaviour of digital circuits over time, showing how signals change state relative to each other. For the Carry Output Predictable Full Adder, the timing diagram includes signal lines for inputs (A, B, C_in), outputs (C_out, S), and the predictable carry output (C_out Predictable). The x-axis represents time, with signal transitions at specific intervals, where high (1) and low (0) states are depicted. The diagram captures COPFA's operation, processing inputs to produce the sum (S) and carry out (C_out), highlighting the predictable carry output to reduce carry propagation delay. This enhances performance, making COPFA suitable for high-speed arithmetic applications. Simulating the circuit provides further insights into its timing and efficiency.

4.2 Backend layout timing diagram of carry output predictable full adder using 7-nm technology

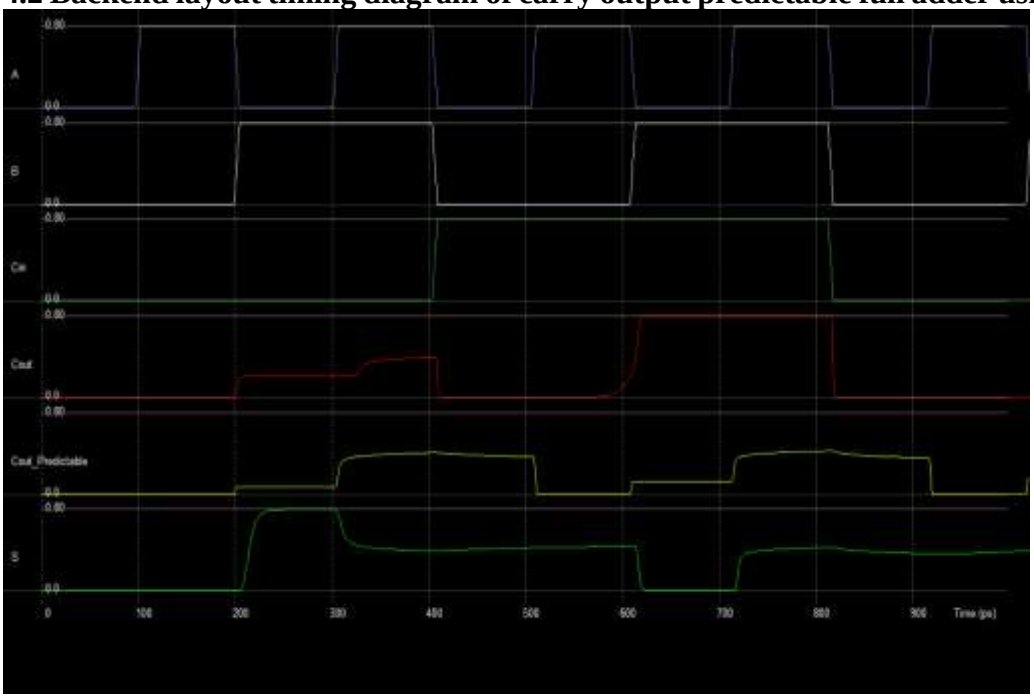

Figure 3(b): Backend layout timing diagram of carry output predictable full adder using 7-nm technology

In Fig.3(b) the timing diagram depicts the operation of a backend carry output predictable full adder. It shows how the inputs A, B, and Cin (carry-in) change over time and how these changes affect the outputs S (sum), Cout (carry-out), and Cout_Predictable. Initially, all inputs and outputs are low. As Cin transitions from 0 to 1, S also changes to 1 while both Cout and Cout_Predictable remain low. Subsequent changes in A and B inputs cause S, Cout, and Cout_Predictable to update according to the rules of binary addition, reflecting the sum and carry outputs accurately. The outputs Cout and Cout_Predictable stay synchronized, indicating predictable behaviour. This Fig.3(b) illustrates the typical full adder functionality with clear and predictable carry output behaviour.

4.3 COPFA Power Dissipation

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Table 2: Carry output predictable full adder power dissipation

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* Microwind Version 3.9, parametric analysis of
"E:\Thinkific_Courses\phd_work_vlsi\Phd_Work\COPFA\COPFA_FinFet_7nm.MSK"
* generated on 13-05-2024, 22:14:23
vdd(V)   power(mWatt)
0.000 0.000
0.050 0.000
0.100 0.000
0.150 0.000
0.200 0.000
0.250 0.000
0.300 0.000
0.350 0.000
0.400 0.000
0.450 0.001
0.500 0.001
0.550 0.002
0.600 0.002
0.650 0.002
0.700 0.003
0.750 0.004
```

The table 2 represents the results of a parametric analysis conducted using Microwind version 3.9.4 on a 7nm FinFET design. The analysis shows the power consumption (in milliwatts) at various supply voltages (Vdd, in volts). At lower voltages (0.000 to 0.300 V), the power consumption is negligible (0.000 mW), while it starts increasing at higher voltages, reaching up to 0.004 mW at 0.750 V. This indicates a nonlinear relationship between supply voltage and power consumption in the FinFET design.

5.0 Frontend timing diagram of 4-bit path selectable hybrid adder using 7-nm technology

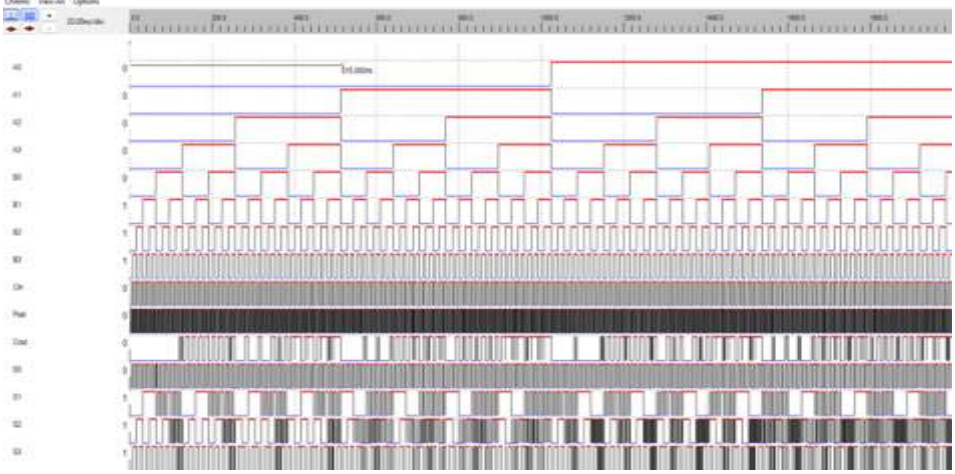

Figure 4(a): Frontend timing diagram of 4-bit path selectable hybrid adder using 7-nm technology

In Fig.4(a) the provided timing diagram illustrates the behaviour of various signals in a digital circuit over time, offering a detailed view essential for understanding and verifying the functionality of the 4-bit path selectable hybrid adder, The signals A0 to A3 and B0 to B3 likely represent the bits of two 4-bit input operands, A and B, respectively, with their distinct patterns showing how these operands vary during operation. The Cin signal, representing the carry input for the adder, toggles frequently, suggesting it is tested under various conditions, including 0 and 1. Psel, probably the path selection signal, changes less frequently than the inputs, indicating a slower rate of alteration in the path selection logic compared to the inputs. The sum outputs (S0 to S3) reflect the results of adding the corresponding bits of A and B, including the carry-in bit, while the Cout signal represents the carry output from the adder, showing the carry-out resulting from the addition operation and any propagated carry. The timing diagram effectively visualizes how the input A, B, and Cin, along with the path selection signal Psel, influence the resulting sum outputs (S0 to S3) and the carry Outputs (Cout), there by confirming the adder's adaptive performance and efficiency in carry propagation and sum generation.

5.1 Backend layout timing diagram of 4-bit path selectable hybrid adder using 7-nm technology

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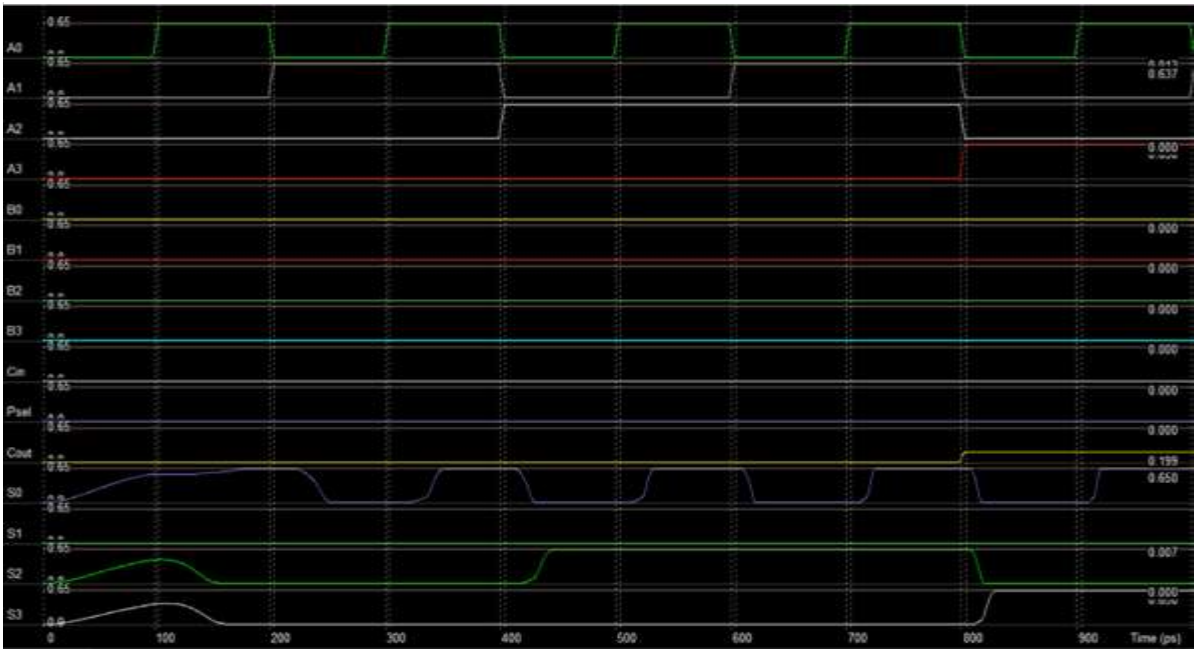

Figure 4(b): Backend layout timing diagram of 4-bit path selectable hybrid adder using 7-nm technology

In Fig.4(b) the timing diagram shown illustrates the behaviour of various signals in a digital circuit over time. Each row corresponds to a specific signal, with the horizontal axis representing time. The signals A0 to A3 and B0 to B3 are data inputs that toggle between high (logic 1) and low (logic 0) states. The Cin signal remains low, acting as the carry-in input. Psel is a control signal, likely used to select between different data paths or operations, possibly for a multiplexer. The Cout signal shows the carry-out result of an arithmetic operation, While S0 to S3 are outputs that change in response to the inputs and control signals, indicating the results of a decoding or selection process. This diagram provides crucial insights into the circuit. Dynamic behaviour allowing engineers to verify its correct operation and identify any timing- related issues.

5.2 4-bit path selectable hybrid adder power consumption

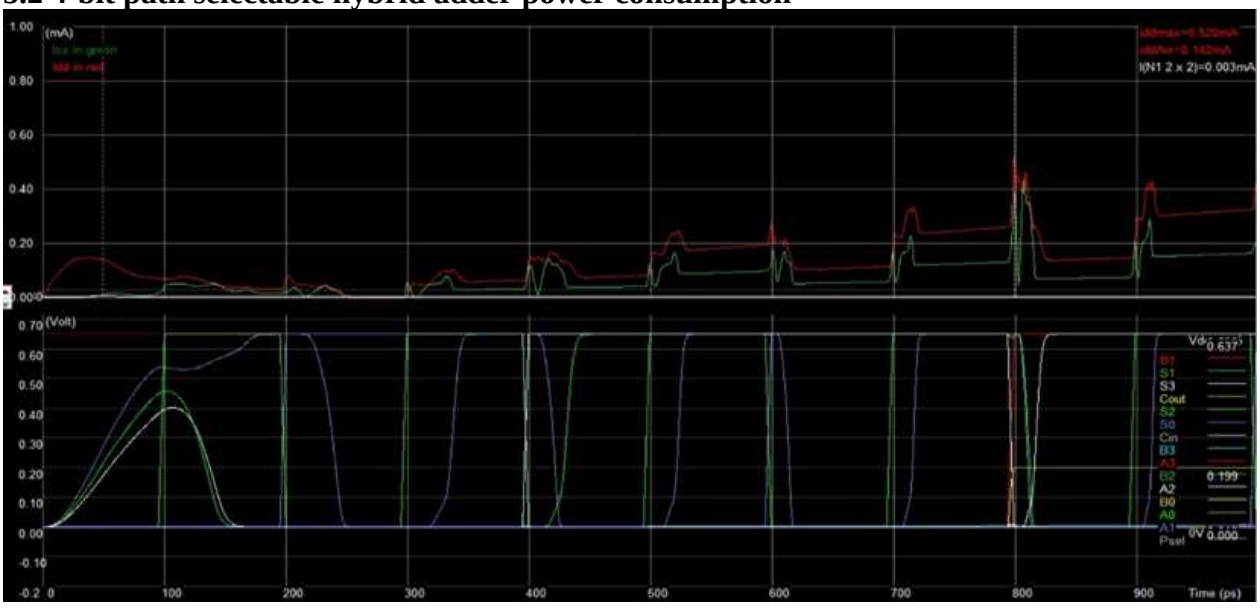

Figure 4(c): 4-bit path selectable hybrid adder power consumption

In Fig.4(c) the timing diagram illustrates the power consumption of a digital circuit, showing voltage signal transitions and corresponding current consumption over time. Key points include the input signals A0, A1, A2, A3, Cin, and Psel, and output signals S0, S1, S2, S3, and Cout. The green line (Iss)

represents steady- state supply current, while the red line (Idd) indicates dynamic current, reflecting power consumed during switching activities. Significant peaks in Idd correspond to signal transitions, highlighting higher power consumption during these periods. Static power consumption (Iss) is relatively stable, whereas dynamic power consumption (Idd) is predominant and fluctuates with switching events, understanding these patterns is essential for optimizing circuit power efficiency.

V. Conclusion

The proposed carry output predictable full adder introduces an innovative approach to enhance the accuracy and scalability of binary addition by predicting the carry output. This design offers two modes of operation, a traditional full adder mode and a prediction mode that optimizes performance by using a logical AND operation on the operand bits A and B to predict the carry output. The predict mode significantly reduces carry propagation delay, thus improving the overall speed and efficiency of arithmetic operations. The 4-bit path selectable hybrid adder further advances this concept by dynamically selecting the optimal path for carry propagation based on input conditions, balancing speed and power efficiency. Simulation studies using Microwind 3.9.4 software confirm that these designs COPFA and PSHA outperform traditional adders in various performance metrics like area, power, and delay metrics. The detailed timing diagrams illustrate the predictable behaviour and efficiency gains of these adders, making them suitable for high-speed computational applications.

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