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DESIGN OF LOW-POWER FULL ADDER USING 7-NANOMETER FINFET TECHNOLOGY

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ABSTRACT
The exponential growth of portable electronic devices has driven significant research in low-power VLSI systems. As chip density and power consumption increase, advancements in semiconductor manufacturing are crucial. This paper presents a design and performance comparison of a full adder implemented with FinFET transistors at the 7nm node, vital for microprocessors, DSPs, and ASICs. Employing XOR/XNOR logic gates with titanium nitride gates and hafnium oxide-silicon oxide insulators, the study compares a traditional full adder (ten FinFETs) with a modified version (eight transistors) two XNOR gates and one multiplexer. Simulations using Microwind FinFET 7nm technology at Vdd = 0.8V demonstrate that the modified design achieves a rise delay of 3.74 ps, fall delay of 1.10 ps, and power dissipation of 0.012 mW, outperforming the traditional design's 9.50 ps rise delay, 1.165 ps fall delay, and 0.072 mW power dissipation. These results highlight FinFET-based designs' potential in meeting stringent power and performance requirements, paving the way for future VLSI advancements performed better than conventional methods in terms of area, power, delay metrics.
Keywords: Finfield-effect transistor, Full adder, Modified full adder, Area, Delay, Rise delay, Fall delay, Power dissipation, Microwind 3.9.4.

I. Introduction
The semiconductor industry has made substantial strides over the past two decades, marked by the transition to 7-nanometer FinFET technology. This evolution has been driven by the need for smaller, faster, and more energy-efficient integrated circuits, crucial for modern applications such as artificial intelligence and high-performance computing [1,2]. The 7nm technology offers significant benefits over previous nodes, including superior channel control, reduced leakage currents, and improved scalability. These advancements have resulted in substantial improvements in power, performance, and area metrics, with power consumption reductions exceeding 50%, performance gains of 20-50%, and a fourfold increase in density [1]. Such enhancements justify the shift to smaller technology nodes despite the rising design and manufacturing costs, laying the groundwork for future developments in 5nm, 3.5nm, 2nm, and even 1.5nm technologies.
The study of full adder designs using 7nm FinFET technology, including the traditional 10- transistor full adder, the modified full adder (MFA), reveals notable performance differences. The MFA, with 8 FinFET transistors per full adder, demonstrates superior efficiency with faster rise and fall delays and significantly lower power dissipation compared to its traditional counterparts. This design leverages advanced features like hafnium-based oxides as insulators to optimize transistor performance through higher dielectric constants and optimized channel operation [3,4]. Furthermore, showcases enhanced performance and reduced power consumption, highlighting significant advancements in digital arithmetic circuitry. These findings underscore the importance of optimizing digital circuits for speed and energy efficiency, particularly in high-performance computing and power-constrained applications such as portable electronic devices [5,6].

II. Literature
The literature review comprehensively explores the evolution of semiconductor technology, focusing on advancements in transistor design, power efficiency, and integration density across various

technology nodes highlights the pivotal role of FinFET technology at 7nm nodes in outperforming traditional planar transistors. Leading semiconductor foundries such as Intel, TSMC, and Samsung are renowned for their pioneering advancements in technology, paving the way for future nodes like 5nm, 3.5nm, 2nm, and 1.5nm. They have progressed from 180nm to 5nm, incorporating key innovations such as copper interconnects, strained silicon, low k dielectrics, high-k metal gates, and EUV lithography. The review addresses economic challenges of scaling down, emphasizing the importance of high IC unit costs and volumes to justify investments. Additionally, it underscores the significance of EOT in semiconductor fabrication, particularly in Microwind simulations, for optimizing gate capacitance and minimizing leakage currents, thus providing valuable insights for researchers and practitioners.The various conventional designs for full adders and their respective drawbacks. Nikoubin, T. [7] developed a full adder with 14 transistors utilizing 32-nm FinFET technology, as well as a 4-bit RCA adder. While this design demonstrated potential, it encountered efficiency challenges. Srinivasu, B. et al. [8] developed design incorporating a 2-to-1 multiplexer using CNTFET technology with 12 transistors was proposed, alongside a hybrid adder combining a 4-bit RCA and parallel prefix adders. However, this design encountered issues related to power consumption. Malik, et al. [9] developed hybrid designs combining CMOS and gate diffusion input logic, as detailed in encountered significant power consumption. Wang, G. et al. [10] developed a full adder using Spin Field-Effect Transistor with variable channel length, a multi-gate transistor model. G. Liu et al. [11] developed a memristor logic-based carry look-ahead adder using hybrid-CMOS and MRL universal gates faced higher power consumption issues. Mamaghani et al. [12] developed another hybrid full adder, utilizing magnetic tunnel junction and FinFET technology with 30 transistors, was explored. However, when tested on 7-nm FinFET technology, it exhibited high power consumption and delay. R. R. Vallabhuni, et al. [13] developed an 8-bit Manchester carry chain adder, implemented using 32-nm FinFET technology, struggled with limited energy resources and a high transistor count. E. Ramkumar et al. [14] a one-bit full adder using FinFET and gate diffusion input technology was developed with multiplexer logic capable of parallel addition operations but suffered from high noise levels. T. Priyanka et al. [15] developed a gate diffusion input technology-based full adder in reduced the number of transistors to eight but faced accuracy issues. K. S. Sanjay et al. [16] developed 10-transistor CNTFET-based full adder and experienced higher delays and power consumption. D. A. Nirmal, [17] implemented basic circuits utilizing flexible nanoparticle based organic electronics faced significant challenges, including high area and delay consumption, as well as heat generation issues at the transistor level . Overall, these conventional designs highlight ongoing challenges with power efficiency, delay, area, noise, and heat generation, indicating the need for further optimization in full adder design.

III. Full adder design

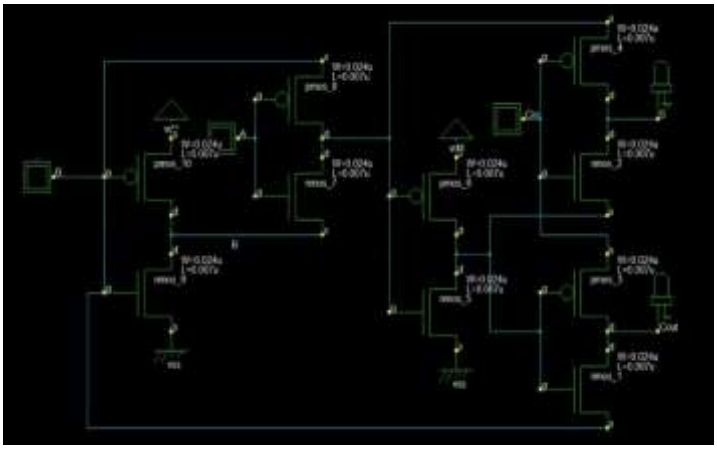

Figure 1(a): Schematic diagram of 10 transistors behaviour full adder.

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In Fig. 1(a) full-adder circuit design leverages 10 FinFET transistors, renowned for their enhanced performance characteristics such as reduced leakage current and improved control over short-channel effects. This circuit incorporates both XOR and XNOR logic operations to compute the sum output (S) and carry-out (Cout), respectively. Each FinFET transistor in the circuit has a channel width of 0.024 micrometres and a channel length of 0.007 micrometres, influencing its threshold voltage and current-carrying capability. Operating at a supply voltage (Vdd) of 0.8 volts, the circuit's performance, power efficiency, and speed are influenced by this parameter. The equations governing the full-adder behaviour encapsulate the XOR and XNOR operations, defining how the inputs (A, B, and Cin) are combined to produce the sum output and carry-out. Together, these design aspects highlight the meticulous consideration of transistor technology, logic operations, dimensions, and voltage supply crucial for the efficient implementation of binary addition in digital logic circuit. The equations governing the full adder is S = A ⊕ B ⊕ C and Cout = A. B + C (A ⊕ B).

3.1The full adder operation is analysed by taking truth table as reference

Table 1: Operational truth table of full adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

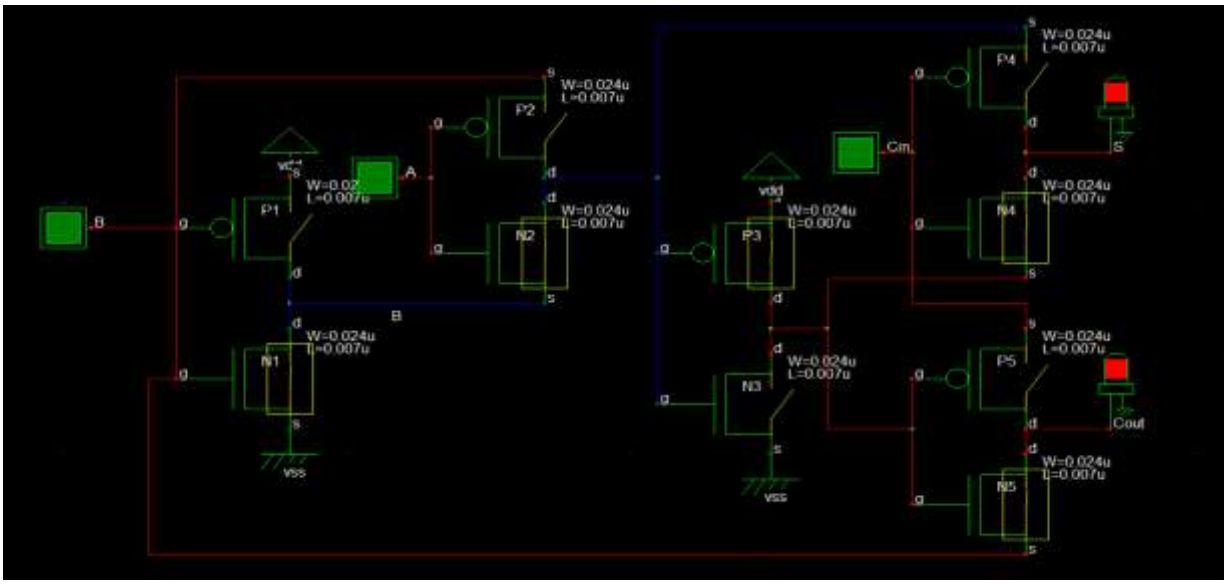

Figure 1(b): Executing eight row of truth table and observing the transistors behaviour.

In Fig. 1(b) the operation of full adder is analysed by taking truth table as shown in table 1 here, eighth row is taken as reference. When the inputs A, B, and Cin are all binary ones, specific switches (P3, N1, N2, N4, N5) are closed while others (N3, P1, P2, P4, P5) are open, indicating that the LED's are in the on state. In this scenario, when a binary signal of 'one' is applied to the gate terminal of the PMOS FinFET transistor charge carriers do not flow through P1, but channels are formed in the N4 and N5 transistors, allowing the passage of signals as binary high (one) signals are applied to their source terminals. As the high binary signal passes to the LED's and exceeds the LED bulbs threshold

voltage, both LED bulbs will glow, satisfying the eighth row of the truth table. This configuration ensures that signals pass through certain transistors while others remain open, controlling the flow of signals through the circuit and determining the LED state.

3.2 Backend layout of 10 transistor full adder using 7-nm technology

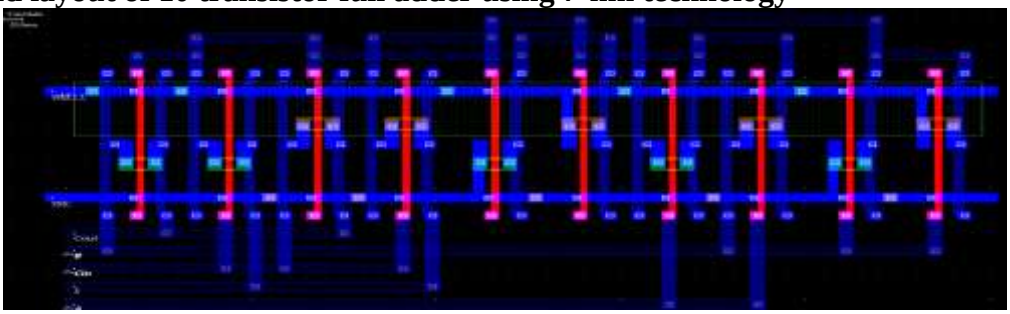

Figure1(c) Backend layout of 10 transistor full adder using 7-nm technology

In Fig. 1(c) the backend phase of the 10-transistor full adder design aims to compute both power consumption and delay. the grid-like arrangement of logic gates and input labels in the diagram suggests a structured approach to signal processing. With inputs like "Lambda" and "2n-1" and a 4-bit binary output labelled "S" the circuit likely performs arithmetic or data manipulation operations. However, its precise function relies on the specific logic gates and interconnections employed, reflecting its intended application.

Single Bit Modified Full Adder Design (MFA)

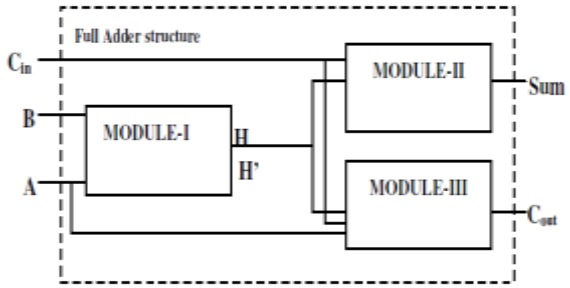

Figure 2(a): Single bit modified full adder design (MFA).

In Fig. 2(a) the function of a modified full adder is based on the following equations. Given three single-bit inputs A, B, and Cin, generates two single-bit outputs, Sum and Cout. These are represented as follows: S=(A⊕B)⊕Cin and Cout=(A·B)+(Cin·(A⊕B)). A structured approach for implementing a single-bit full adder using XOR/XNOR logic has been formulated with decomposition of full adder cell into smaller cells, we can be rewritten as S = H XOR Cin = H. Cin' + H'. Cin, Cout = A.H' +Cin.H where H is the half sum (A XOR B) and H' is the compliment of H.

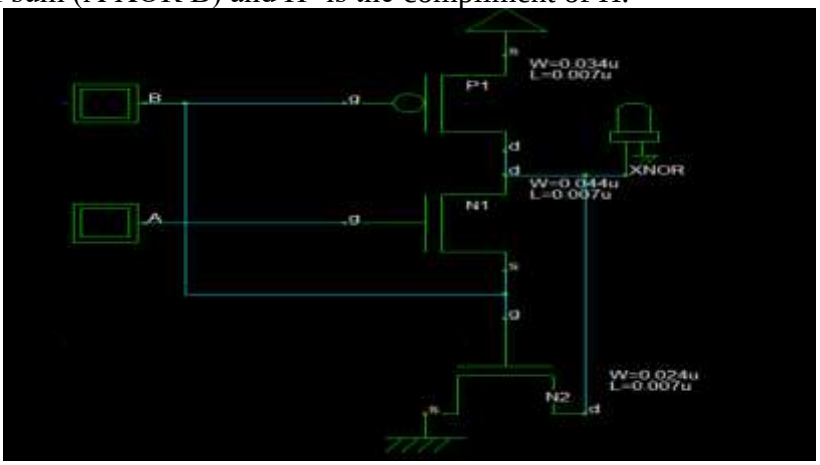

Figure 2(b): Schematic diagram of an XNOR gate.

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In Fig. 2(b) the proposed design of an XNOR circuit uses three transistors in 7 nm technology. The gate lengths of all three FinFET transistors are 0.007 µm. The gate widths are as follows: N1 is 0.044 µm, N2 is 0.024 µm, and P1 is 0.034 µm. This efficient design leverages the small dimensions of 7 nm technology to achieve a compact and effective XNOR circuit.

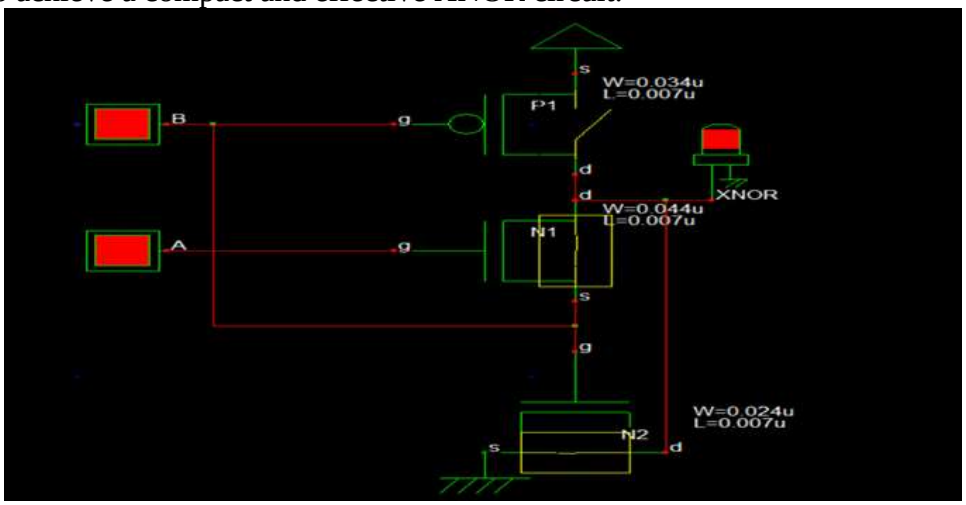

Figure 2(c): Executing XNOR truth table by taking A=B=1, XNOR=1 and observing the transistors behaviour.

In Fig. 2(c) the image shows a schematic of an XNOR gate designed with three FinFET transistors in 7 nm technology. The transistors include P1 (PMOS) with a width of 0.034 µm and length of 0.007 µm, N1 (NMOS) with a width of 0.044 µm and length of 0.007 µm, and N2 (NMOS) with a width of 0.024 µm and length of 0.007 µm. Inputs A and B are connected to the gates of P1 and N1, and N2, respectively. P1's source is linked to the supply voltage, its drain to N1's drain, N1's source to N2's drain, and N2's source to ground. The XNOR gate output is taken from the junction of N1 and P1's drains. This configuration enables the XNOR function, outputting high when inputs are identical and high. This compact design ensures minimal area and power usage while maintaining effective XNOR logic operation, leveraging the advantages of FinFET technology.

4.1 Modified Full Adder Structure

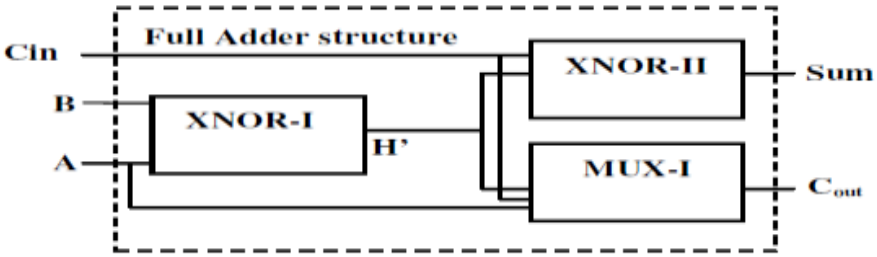

Figure 2(d): Modified full adder structure

The proposed modified full adder circuit utilizes a combination of two XNOR gates and a multiplexer block, as illustrated in the accompanying block diagram. The Sum output (S) is generated through the use of two XNOR gates, while the Carry-out (Cout) is produced by a multiplexer block consisting of two transistors. This single bit modified full adder is implemented utilizing the proposed XNOR gates, each comprising eight transistors, as depicted in the provided Fig. 2(d) for the multiplexer section, typical transistor dimensions have been utilized, with NMOS transistors having a width (Wn) of 0.024µm and PMOS transistors a width (Wp) of 0.034µm, both featuring a gate length of 0.007µm. Simulations of the circuit were conducted using the Microwind FinFET 7nm technology, with a supply voltage (Vdd) of 0.8 volts. This implementation demonstrates the efficiency and compactness of the design, leveraging advanced FinFET technology to achieve high performance with reduced power consumption.

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4.2 Transistor level schematic diagram of modified 8 transistor full adder

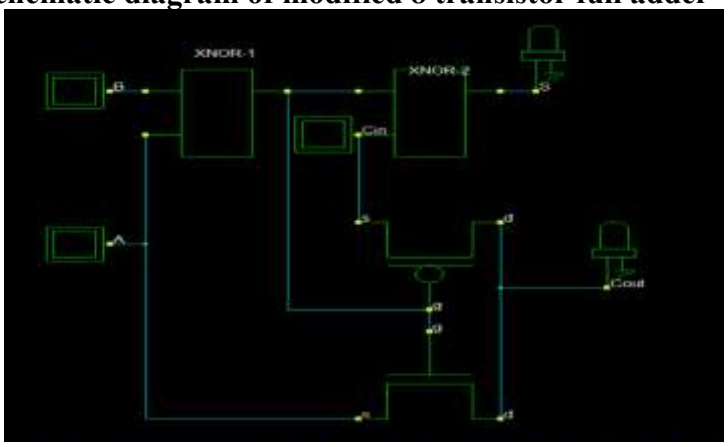


Figure 2(e): Transistor level schematic diagram of modified 8 transistor full adder

In Fig. 2(e) the transistor-level schematic diagram of a modified 8-transistor full adder, featuring a combination of PMOS transistors and NMOS transistors (P1, P2, P3, N1, N2, N3, N4, and N5). The design incorporates inputs A, B, and Cin, alongside outputs Sum and Cout. The XNOR gate, formed by transistors P1, N1, and N2, generates an intermediate signal used to calculate the Sum. The Sum output is further refined using transistors P2, N3, and N4, while the Cout output is derived using transistors P3 and N5. This efficient layout minimizes transistor count while ensuring the correct functionality of the full adder, effectively handling the sum and carry-out operations based on the inputs.

4.3 The 8-transistor full adder operation is analysed by taking truth table as reference

Table 2: Operational truth table of 8 transistor modified full adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

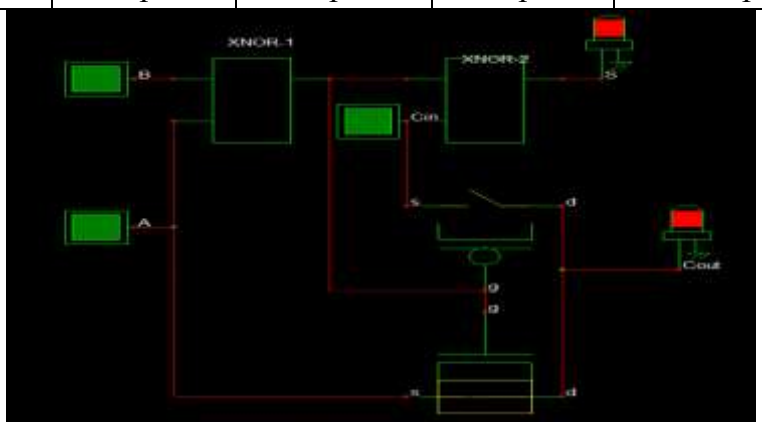


Figure 2(f): Executing truth table and observing the transistors behaviour of 8 transistor modified full adder design

In Fig. 2(f) the provided schematic diagram illustrates a modified full adder circuit designed to compute the sum (S) and carry-out (Cout) for inputs A=1, B=1, and Cin=1. The circuit comprises two XNOR gates and a multiplexer block. The first XNOR gate (XNOR-1) takes inputs A and B and outputs the XNOR of these inputs. For A=1 and B=1, the output of XNOR-1 is 1. This output, along

with Cin =1, is fed into the second XNOR gate (XNOR-2), which also produces an output of 1. Thus, the sum output (S) is 1. The multiplexer block, which is responsible for generating the carry-out (Cout), takes the same inputs A=1, B=1, and Cin=1. Given these inputs, the multiplexer transistors are configured to handle the carry operation, producing a carry-out of 1. Therefore, with the inputs A=1, B=1, and Cin=1, the full adder circuit outputs a sum (S) of 1 and a carry-out (Cout) of 1. This schematic effectively demonstrates the functionality of the full adder, confirming that it accurately computes the sum and carry-out as 1 and 1, respectively, for the given inputs.

4.4 Backend layout of 8 transistor full adder using 7-nm technology

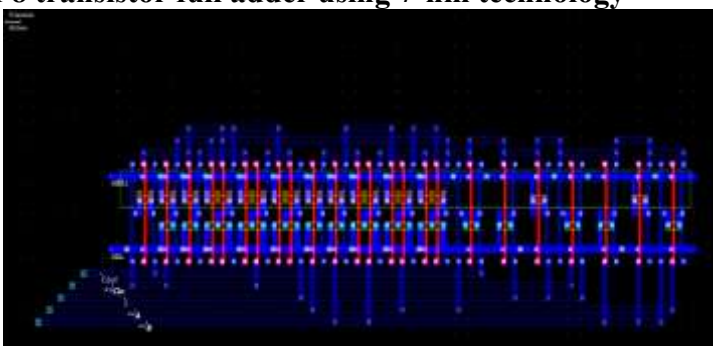


Figure 2(g): Backend layout of 8 transistor full adder using 7-nm technology

In Fig. 2(g) the layout diagram of an 8-transistor full adder represents the physical arrangement of PMOS (p-channel metal-oxide-semiconductor) and NMOS (n-channel metal-oxide-semiconductor) transistors on a semiconductor material, which is crucial for designing and fabricating digital circuits that perform arithmetic operations like addition. This specific full adder configuration employs four PMOS and four NMOS transistors to compute the sum (S) and carry-out (Cout) of three inputs: A, B, and the carry-in (Cin). The diagram includes detailed labels and connections, such as the power supply connection (Vdd), ground connection (Gnd), and the inputs (A, B, and Cin). The outputs are the sum (S) and carry-out (Cout), with specified voltage levels for each. The sum output reaches a high level of approximately 1.97V and a low level of around 0.24V, while the carry out output has a minimum high level of 3.2V and a maximum low level of 0.32V. This layout as shown in Fig. 2(g) provides an idealized view, and actual implementations may differ due to process variations and other factors, highlighting the complexity and precision required in semiconductor design and fabrication.

IV. Results

A comprehensive simulation performance study of suggested adders is presented utilizing a wide variety of parameters. In addition, to perform the proposed full adder and modified full adder is compared with the performance of traditional adders using a variety of parameters. The Microwind 3.9.4 software tool is used in the process of designing and simulating the different designs.

4.1 Timing diagram of 10 transistor full adder using 7-nm technology

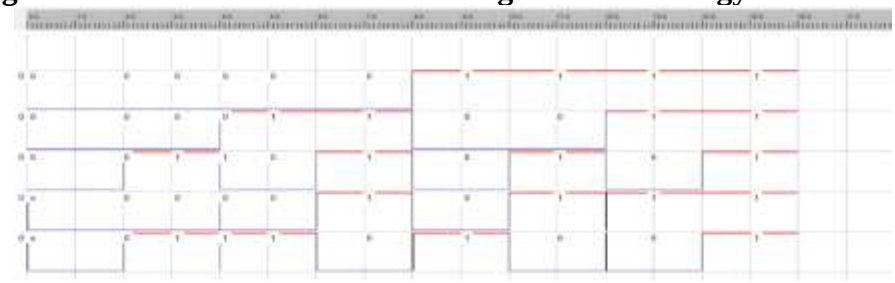


Figure 3(a): Timing diagram of 10 transistor full adder using 7-nm technology

The timing diagram of a 10-transistor full adder circuit Fig.3(a) provides valuable insights into the dynamic behaviour of inputs and outputs over time during addition operations. By observing

transitions between high and low states in signal lines representing inputs (such as Cin, A, B) and outputs (Sum, Cout), engineers can analyse critical points and propagation delays within the circuit. This understanding is crucial for optimizing performance and ensuring accurate computation in digital systems. Academic research, such as the study titled “Development of a low-power 10-transistor full adder utilizing gate diffusion input technique for enhanced energy efficiency in arithmetic applications" offers further insights into low-power full adder designs, emphasizing energy efficiency and performance characteristics. Additionally, educational resources on adder design provide valuable guidance for engineers seeking to develop efficient and reliable digital circuits for arithmetic applications.

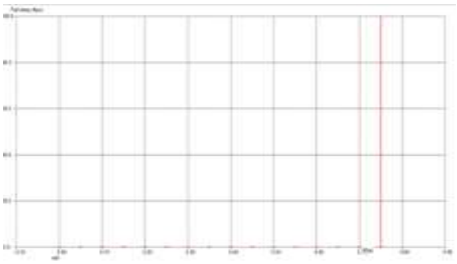
4.2 Backend layout timing diagram of 10 transistor full adder using 7-nm technology

Figure 3(b): Backend layout timing diagram of 10 transistor full adder using 7-nm technology

The timing diagram Fig.3(b) illustrates signal transitions and voltage levels over time in a 10-transistor full adder circuit utilizing 7-nanometer technology. Each signal line, including A, B, Cin, Cout, and S, is represented with markers indicating transitions from low to high voltage or vice versa. These transitions occur at specific time points, revealing how inputs influence outputs and identifying propagation delays within the circuit. The voltage levels range from -0.10V (low) to +1.00V (high), providing insights into the binary sum output (S) and its 4-bit representation. Overall, the diagram offers valuable insights into the dynamic behaviour of digital signals in the context of arithmetic operations, aiding in the analysis and optimization of digital systems.

4.3 Rise delay and fall delay from signal a to ground (vss) measured on the sum output (s)

Graph1(a): Rise delay

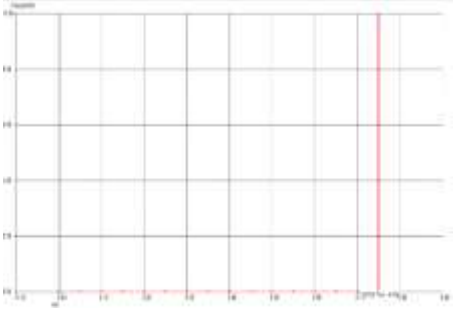


Graph 1(b): Fall delay

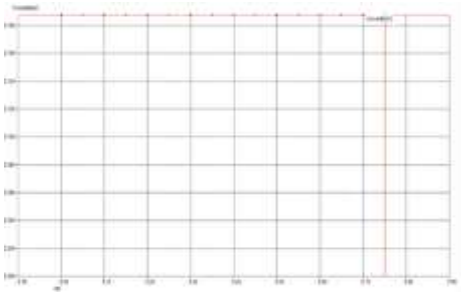
The Graph 1(a) "Rise delay [ns]" measures rise time delay in nanoseconds (ns), with the horizontal axis ranging from 0.00 to 0.90 and a label phi [0] at the far right. The vertical axis spans from 0 to 3000 ns in 500 ns increments, indicating delay values. A red vertical band between 0.85 and 0.90 highlights a specific range of interest. This graph1(a), underscores the importance of rise delay in timing-sensitive digital circuits, where components exhibit varying delay characteristics, and phi [0] likely denotes a critical parameter or condition affecting the delay.The Graph: 1(b**)** "Fall delay [ps]" measures fall time delay in picoseconds (ps), with the horizontal axis labelled "vdd" for supply voltage and the vertical axis indicating delay. A red vertical band near "0.90" highlights a specific range of interest. The graph suggests how fall delay varies with supply voltage, crucial for timing-sensitive

digital circuits with varying delay characteristics. The label "phi [0]" likely denotes a specific condition or parameter relevant to the fall delay behaviour.

4.4 Power dissipation in nanowatt and crosstalk amplitude



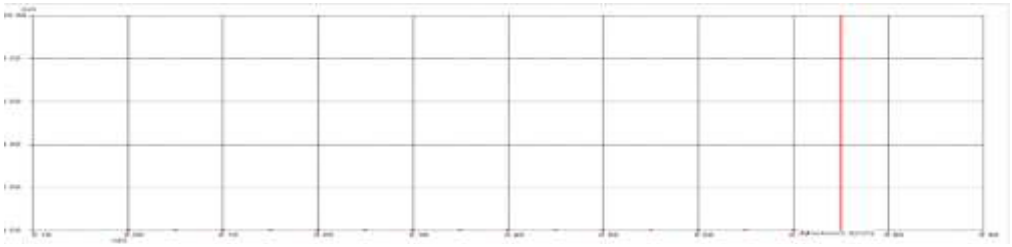
Graph: 1(c) Power dissipation (nW)



Graph: 1(d) Crosstalk amplitude (V)

The graph 1(c), mislabelled as “Fall delay [ps],” should depict power dissipation in milliwatts (mW) against supply voltage (vdd) in volts. A red vertical band labelled at CMOS 7nm - B Max” highlights a critical range around 0.90V. This graph likely illustrates how power dissipation varies with supply voltage, crucial for designing energy-efficient circuits. Understanding this relationship is essential for optimizing performance and minimizing power consumption in 7nm CMOS technology. In graph 1(d), the "Crosstalk (V)” shows crosstalk voltage in volts versus supply voltage (vdd) from -0.10V to 0.90V, with the vertical axis up to 0.18V. Red dots indicate crosstalk voltage remains around 0.18V across various vdd values. A red vertical band between 0.85V and 0.90V highlights a critical range of interest. This suggests stable crosstalk voltage but emphasizes the need for attention within this range, crucial for maintaining signal integrity in high-frequency or sensitive electronic circuit applications.

4.5 Maximum Idd current



Graph:1(e) Maximum Idd current

The graph 1(e) titled "Maximum Idd (mA)" illustrates the maximum current (in milliamperes) relative to the supply voltage (vdd), ranging from -0.10V to 0.90V. The red dots near the baseline indicate very low and consistent current values across the vdd range. A highlighted vertical band around 0.80V to 0.90V marks a critical region where the current peaks are of particular interest. This suggests a critical operating range where monitoring maximum current is essential for preventing excessive current that could damage circuit components. Overall, the graph underscores the importance of understanding current behaviour for designing reliable and efficient electronic circuits.

5.0 Timing diagram for single bit 8 transistor full adder

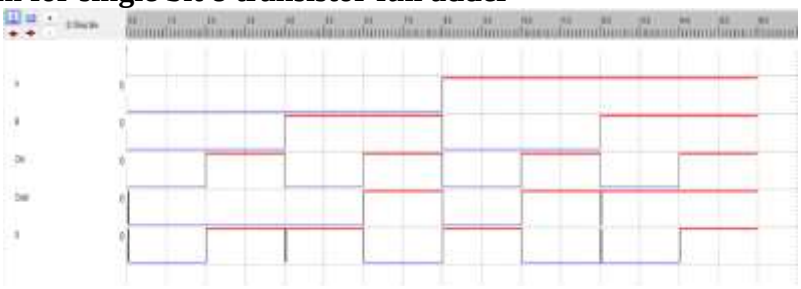


Figure 4(a): Timing diagram for single bit 8 transistor full adder

The timing diagram of Fig. 4(a) for a single-bit 8 transistor full adder shows how inputs (A, B, Cin) and outputs (Cout, S) vary over time, illustrating the adder's dynamic behaviour. Inputs are single-bit

values to be added with a carry input, and outputs include the sum and carry output. The diagram depicts signal changes and the resulting propagation delays, essential for ensuring the adder meets timing constraints and functions correctly in digital circuits.

5.1 Timing diagram of backend lay out of 8 transistor full adder using 7-nm technology

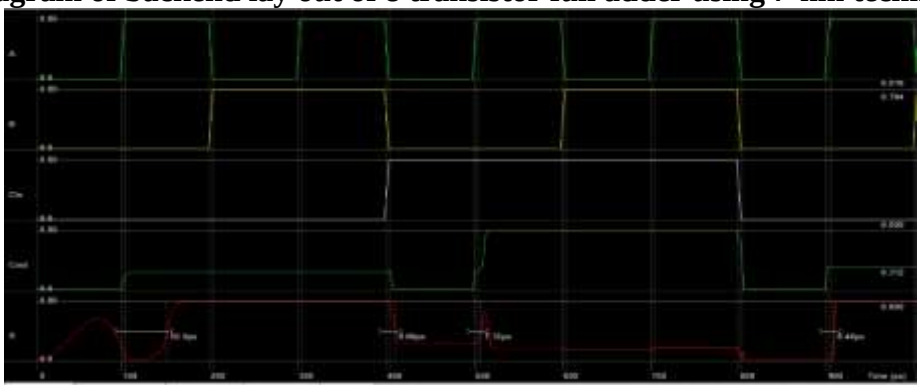
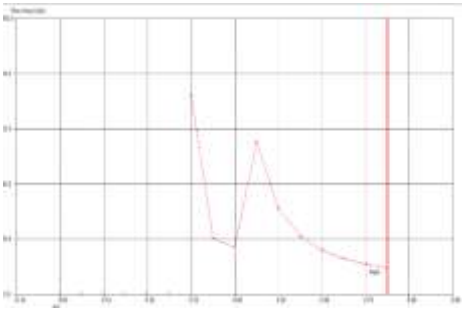


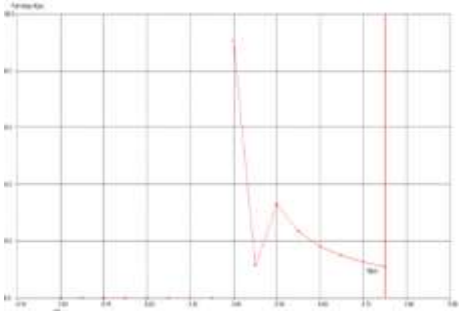
Figure 4(b): Timing diagram of backend lay out of 8 transistor full adder using 7-nm technology

The timing diagram and backend layout of an 8-transistor full adder using 7-nanometer technology as shown in Fig. 4(b) illustrate the critical role this circuit plays in arithmetic operations within digital systems. The timing diagram visualizes how input signals (A, B, and Cin) and output signals (Cout and S) transition over time, highlighting the interactions and delays inherent in the circuit. The backend layout showcases the physical arrangement of the transistors and interconnections, optimized for efficient routing, minimal area, and proper electrical connectivity. Utilizing 7-nm technology ensures smaller feature sizes, reduced power consumption, and faster operation, with design goals focused on minimizing power consumption, optimizing area, and balancing speed with reliability. This design provides a compact, efficient, and high-performance solution for digital arithmetic operations.

5.2 Rise delay at output (s) and fall delay time (ps)



Graph: 2(a) Rise delay at output (s)



2(b) Fall delay time (ps)

In digital circuits, as shown in graph 2(a) rise delay measures the time for a signal to transition from low (0) to high (1) after crossing a threshold, affecting overall signal propagation speed and circuit performance. Gate delays are specified in formats like single delay, separate rise and fall delays, and three delays including turn-off transitions. These delays can be minimum, typical, or maximum to meet specific design requirements. Properly defining these delays ensures a balance between speed and reliability in digital designs. The graph 2(b) represents "Fall delay (ps)" which shows the relationship between fall delay and vdd, with fall delay being the time for a signal to transition from high to low, crucial for high-speed digital circuits. The graph depicts a sharp dip near 0.10, peaking above 5 around 0.20, and gradually declining towards zero near 0.90. Two vertical red shaded areas between 0.50-0.60 and at the x-axis end highlight critical regions impacting fall delay. Engineers can use this data to optimize vdd, minimizing fall delay to enhance circuit performance and achieve efficient, reliable designs.

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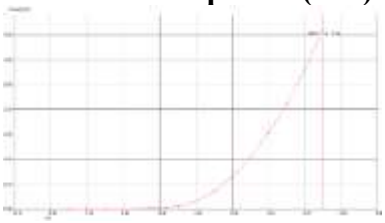
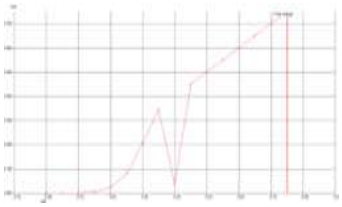
5.3 Power dissipation (mw) and output voltage at "S" port in volts

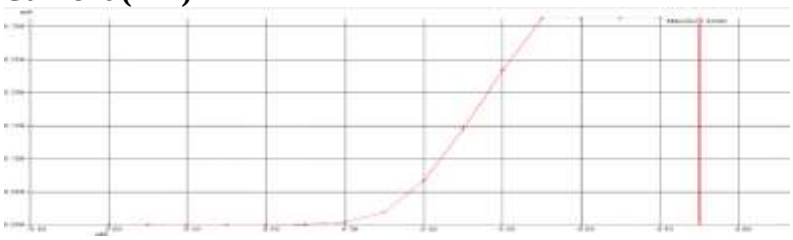




Graph: 2(c) Power dissipation (mW) 2(d) Output voltage (v) at "S" port

The graph 2(c) illustrates power dissipation (mW) versus supply voltage (vdd), with the curve starting near the origin and steepening significantly as vdd increases, indicating a non-linear relationship. This pertains to CMOS 7nm technology, highlighting the importance of efficient voltage selection to minimize power dissipation. Understanding this relationship is crucial for engineers to design energy-efficient circuits by optimizing vdd for desired performance while reducing power consumption. Proper voltage optimization ensures both efficiency and performance in advanced electronic designs. The graph 2(d) shows the dynamic behaviour of the output voltage at the S port over time, with the horizontal axis for time (t) and the vertical axis for voltage (Volt). The red line starts at 10 volts at t=0.00, dips to 20 volts at t=0.20, rises sharply to over 60 volts after t=0.40, and peaks at 70 volts between t=0.80 and t=0.90. A red vertical band labelled "Final voltage" marks the region where the voltage stabilizes at around 70 volts. Understanding these fluctuations is crucial for engineers to optimize circuit performance and ensure reliable system operation.

5.4 Maximum Idd Current (mA)



Graph: 2(e) Maximum Idd Current (mA)

The graph 2(e) depicts the behaviour of the maximum drain-source current (Idd) in milliamperes (mA) relative to an unspecified parameter on the x-axis, which ranges from 0.00 to 0.80. The vertical axis indicates current in mA. Starting at the origin (0,0), the red curve rises gradually at first, then steeply after passing the 0.50 mark on the x-axis, indicating that Idd reaches its peak value. The vertical red line labelled "Maximum Idd" marks the point where the current attains its maximum. This peak current is critical for determining the safe operating limits of a device, as exceeding it can result in device failure or damage. Engineers utilize such graphs to design circuits that operate within these safe current boundaries, ensuring reliability and preventing potential damage.

5.5 Comparison of parameters between full adder and modified full adder

Full adder	Modified full adder
It is designed by using 10 Finfet transistors in 7nm technology	It is designed by using 8 Finfet transistors (two XNOR gates and one Mux) in 7 nm technology
Rise delay in Ps measured at output S with respect to vdd (0.75 v) = 9.50 ps	Rise delay in Ps measured at output S with respect to vdd (0.75 v) = 3.74 ps
Fall delay in Ps measured at output S with respect to vdd (0.75 v) = 1.165 ps	Fall delay in Ps measured at output S with respect to vdd (0.75 v) = 1.10 ps
Power dissipation with respect to vdd (0.75v) at the output S = 0.072 mWatt	Power dissipation with respect to vdd (0.75v) at the output S = 0.012 mWatt

V. Conclusion

The design and simulation of a 10-transistor full-adder circuit using 7 nm FinFET technology demonstrates significant advancements in digital circuit performance, power efficiency, and speed. By

leveraging FinFETs' reduced leakage current and improved control over short-channel effects, the circuit achieves efficient binary addition with minimal power consumption and area usage. Key metrics show that the modified full-adder achieves a rise delay of 3.74 ps, a fall delay of 1.10 ps, and a power dissipation of 0.012 mW, outperforming traditional designs significantly. These findings highlight the potential of FinFET technology in enhancing the performance and efficiency of digital arithmetic circuits, paving the way for more advanced computational systems.

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