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DESIGN OF JOINT RECONFIGURABLE HYBRID ADDERS USING CARRY OUTPUT PREDICTABLE FULL ADDERS

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Abstract
Adders are fundamental components utilized in a variety of applications, including digital signal processors (DSPs) based on integrated circuits, as well as arithmetic and logical units, serving as essential building blocks (ALUs). In the past, adders were produced using complementary metal oxide semiconductor (CMOS) and field-effect transistor (FET) technologies, leading to an escalation in the total count of transistors and a corresponding rise in power consumption. The study's main objective is to develop hybrid adders using FinFET and graphene nano-ribbon field-effect transistor (GnrFET) based nanotechnologies due to the drawbacks of conventional adders made with complementary metal oxide semiconductor (CMOS) and field-effect transistor (FET) technologies, which led to an upsurge in the overall transistor count and power consumption. As a result, the primary focus of this study is on the creation of hybrid adders by making use of FinFET and graphene nano-ribbon field effect transistor (GnrFET) based nanotechnologies. By implementing a multiplexer logic-based carry output predictable full adder (COPFA) with efficient selection of carry-outputs, the delays caused by sum estimation were significantly reduced during the initial stages of development. The time required for carry-output selection was significantly reduced, leading to the development of a Path Selectable Reconfigurable Hybrid Adder (PSRHA) that allows for the selection of high-speed and low-speed carry propagation channels through the COPFA module. The COPFA module yielded several findings, including a TEC of 0.9077nJ, TC of 51.038 nA, COFD of 1.038 ps, SFD of 15.223ns, and an APC of 1.3184 nw. Moreover, the PSRHA module produced TEC values of 0.09121nJ, TC values of 3.19587 nA, COFD values of 19.7847 ps, SFD values of 25.0352ns, and APC values of 25.0352nw. The simulations showed that compared to conventional methods, the suggested COPFA and PSRHA performed better in power, delay, and energy metrics.

Keywords: Fin field-effect transistor, Graphene nano-ribbon field effect transistor, Subtractor, Full adder, Adder, Power, Delay, Energy reduction.

1. Introduction

For the past 50 years, Moore's law scaling, particularly through the use of Complementary Metal Oxide Semiconductor (CMOS) technology, has been the primary driving force behind the remarkable advancements in integrated circuits. Although there is disagreement about whether we have already reached or are approaching the end of Moore's law, there are unmistakable signs that certain constraints are starting to manifest. The constraints of two-dimensional (2D) lithography have been reached, and the processor clock frequency, a significant indicator of performance, has hit a plateau. Furthermore, the regular pattern of doubling integration density has slowed down in 14 nm and 10 nm CMOS, ultimately leading to a plateau in the field, as reported in [1, 2, 3]. For the past decade, research efforts under the name "Beyond CMOS" have been underway to identify an alternative device with superior properties to CMOS. The research encompasses various devices that resemble CMOS, such as tunnel FETs, GaN TFETs, Graphene ribbon pn junctions, and Ferroelectric FETs, as indicated in [4]. Additionally, the research covers a range of other devices such as quantum-dot cellular automata (QCA), nanomagnet logic, resistance-switching devices including Resistive RAM, Phase Change Memory, and Conductive Bridge RAM, spin-based devices, as well as plasmonic-based devices, as

mentioned in [5]. Recent benchmarking studies indicate that, in terms of the critical aspects of computing such as energy consumption, latency, and area, none of the post-CMOS devices evaluated in [4,6] were found to outperform CMOS.

Despite having desirable qualities like low-voltage operation and non-volatility, certain post-CMOS devices were disregarded. It is expected that post-CMOS devices will enhance computational fabrics that rely on CMOS technology rather than completely replacing it. Approximate computing is gaining popularity as a feasible low-power substitute for precise computing in practical applications of digital signal processing, which form the basis of modern electronics, computer, and communication engineering. This is particularly evident in applications that demand significant processing power. Regardless of whether it pertains to big data analytics, software engineering, neuromorphic computing, hardware implementation of deep neural networks for machine learning and artificial intelligence, or memory systems for multicore processors [7], approximate computing continues to hold relevance.

Graphics processing units that consume low power [8]. The design of electronic systems with ultra-low power consumption can involve utilizing sub-threshold operation of devices.[9]; The aim of achieving greater computing efficiency can be pursued through various means. [10], approximate computing is increasingly being used in a variety of contexts. Approximate computing leverages the inherent error resistance present in realistic multimedia applications to optimize efficiency. Although approximate computing covers both hardware and software, the focus of this research area is primarily on designing approximate hardware. Within this field, the majority of research efforts have centered around developing approximate logic circuits and arithmetic circuits, such as adders and multipliers. The construction of a rough adder is the topic of discussion in this section. While the current research offers several approximate adders that are suitable for implementation using application specific integrated circuits (ASICs), only a limited number of these adders are also appropriate for use with field programmable gate arrays (FPGAs). It is improbable that numerous approximate adders discussed in the literature could outperform a native accurate FPGA adder of comparable size when implemented on an FPGA, as FPGAs contain precise arithmetic units, including adders and multipliers, that are optimized for both speed and area. The reason for this is that FPGAs contain precise arithmetic units, such as adders and multipliers.

2. Related work

Using 18nm FinFET technology, R. R. Vallabhun and colleagues [10] offered a variety of different and efficient solutions for d-latch. When compared with flip flops, the initial designing of locks is characterized by a high degree of flexibility. When compared to planar CMOS, the FinFET technology provides a number of benefits, including a lower power consumption and a lower leakage current. Additionally, The Cadence virtuoso tool is used to construct and simulate the circuits while using FinFET spectral models. In conclusion, in contrast to more conventional D-Latch designs, the latches described here make use of FinFET, this leads to a reduction in both power consumption and power delay product.

P. A. Gowri Sankar, et al. [11] proposed a newly developed arithmetic circuit, which operates on ternary logic and is characterized by high performance and low power consumption, is realized using double-gate (DG) FinFETs and field-effect transistors based on graphene nanoribbons (GNRs). This new circuit would be able to perform ternary logic arithmetic in a more efficient manner (GNRFET). In the beginning, the suggested ternary combinational circuits have been simulated using HSPICE. by employing the conventional 32nm DG-FinFET and GNRFET technologies. In conclusion, based on the results of extensive simulations, it has been found that graphene field-effect transistor-based ternary logic arithmetic circuits exhibit superior performance in terms of power consumption, latency, and power delay product (PDP) compared to the DG FinFET technology. More efficient manner (GNRFET). In the beginning, the suggested ternary combinational circuits have been simulated using

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D. R. Premachand and colleagues [12] came up with a novel approach to the construction of complete adders that makes use of GDIcell. In CMOS logic circuits, the source and substrate terminals of P-type and N-type Metal Oxide Semiconductors are typically connected to the supply voltage VDD and GND, respectively**.** In the beginning, the work that is being suggested employs a lower total number of transistors, a simpler design, and a smaller amount of silicon surface (chip area) for its logic circuits. A full adder (TG) utilizes a CMOS transmission gate for its design, implementation, and simulation. By comparing the total number of transistors used in each of the three designs, pass transistor logic (PTL) together with gate diffusion input (GDI) approach may be determined. Ten transistors are needed for the implementation of a full adder using the GDI approach for design. For the purpose of schematic capture and simulation of entire adder circuits, the Tanner EDA tool version 3.1 is used.

D. R. Premachand and colleagues [13] came up with a novel approach to the construction of complete adders that makes use of GDIcell. In conclusion, the work that has been presented employs a lower total number of transistors, a simpler design, and a smaller amount of silicon surface (chip area) for its logic circuits. CMOS Transmission gate is used in the design, implementation, and simulation of a full adder (TG). By comparing the total number of transistors used in each of the three designs, pass transistor logic (PTL) together with gate diffusion input (GDI) approach may be determined. The design of a complete adder using the GDI approach requires ten transistors. For the purpose of schematic capture and simulation of entire adder circuits, the Tanner EDA tool version 3.1 is used.

S. Sarkar et al. [14] introduced the Modified Gate Diffusion Input (m-GDI) technology is used to assist in the design of a low-power multi-bit hybrid adder. In addition to this, they offered a comparison analysis between a variety of different adders and the methods of implementation that they used. The results of the simulation were acquired by utilizing DSCH 3.8, and the design is now being validated and simulated using Verilog HDL in the environment provided by Xilinx ISE 14.7. The purpose of this modification is to enhance device speed, decrease power consumption, and improve space efficiency. Adders are one of the necessary components of any digital system, which means that to put these modifications into effect, our first priority must be to develop a power-efficient adder that is capable of calculating a number of bits within a certain amount of time.

K. D. Shinde and colleagues [15] proposed a comparative analysis is suggested for the design of a 1-bit full adder, which evaluates both conventional techniques and new techniques. Using Virtuoso and ADE environment at GPDK 45nm technology, the design and simulation of a 1-bit full adder is performed on Cadence Design Suite 6.1.5, with PMOS and NMOS devices having constant width and length. The study concludes with a comparison of the various designs of 1-bit full adders in terms of gate count, delay, power, and power delay product is shown.

Using CMOS, Complementary Pass Transistor Logic (CPL), and Double Pass Transistor Logic (DPL) logics, S. Nagaraj and colleagues [16] Various types of adders such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Incremental Adder, Carry Skip Adder, Carry Select Adder, and Conditional Sum Adder have been constructed and analyzed using CMOS, Complementary Pass Transistor Logic (CPL), and Double Pass Transistor Logic (DPL) technologies for both 16-bit and 32-bit adders. The performance metrics such as speed, area, and power consumption are compared among these different adders. Additionally, Carry Incremental Adder and Carry Skip Adder have been designed.

[17] High speed adder circuits developed by D. S. Rashmi and colleagues. Several adders, including Ripple Carry Adder, Kogge Stone Adder, and Brent Kung Adder, have been designed and modeled using CMOS and GDI logic. A comparative study is then carried out.The simulation results are employed to confirm the functionality of high-speed adders and investigate key performance metrics

such as power consumption, delay, and power-delay product. With the findings that were acquired and the analysis that was done, based on the speed and power metrics, it is clear that KSA is the most efficient choice.

S. Lakshmi, et al. [18] introduced a unique 1-bit energy efficient hybrid adder. In the beginning, the proposed model incorporates a hybrid design comprising of complementary metal oxide semiconductors, pass transistors, and modified gate diffusion input logics (CMOS-PT-MGDI). This is done so that it will have both a low power consumption and a fast speed. The performance characteristics of 1-bit full adders, including their power consumption, latency, and area, were examined, and summarized. Cadence Virtuoso was used for the implementation of each circuit, and 90nm technology with a 1.2V supply was used.

A novel method for the construction of low power digital circuits called GDI (Gate Diffusion Input) was suggested by S. Malipatil and his colleagues [19]. At first, this technology makes it possible to minimize the amount of space that digital circuits take up and the amount of power they need. This design utilizes three transistors to construct an XOR gate, while a CMOS full adder is built by combining two 3T XOR gates with a 2T Mux gate. In this article, a complete adder is developed by making use of eight transistors, and voltage scaling is also accomplished by lowering the supply voltage. With this entire adder design, we are able to achieve a power consumption of 4.604 microwatts and a total area of 144 micrometers.

A unique implementation of an 8-bit adder architecture using the modified Gate Diffusion Input (m-GDI) technique was developed by G. Nayan and colleagues [20]. The key constituent components of the adder include the partial full adder, the 1-bit full adder, the 4-bit ripple carry adder (RCA), and the 4-bit carry look ahead adder (CLA) at the outset. In comparison to a typical CMOS design, the adder architecture that has been presented requires 35% less power, 71% less latency, and 70% less space than the old design. In conclusion, the suggested adder has been built using the Cadence Virtuoso Tool and the 180nm manufacturing process.

Liu, et al. [21] suggested There are two distinct varieties of carry-lookahead adders (CLA), both of which are based on a hybrid CMOS-memristor construction. The first one is based on MRL logic, while the second one is an upgraded version that is implemented by an MRL universal gate (MRLUG). As the proposed design method requires fewer memristors and CMOSs compared to IMP-based or CMOS-based CLAs, it leads to a reduction in circuit size and power consumption. The proposed CLAs have been confirmed by theoretical analyses and simulations.

The Ternary Half Adder (THA) circuit was suggested by S. Vidhya Dharan and colleagues [22]. When compared to the typical CMOS designs that are already out there, the suggested Ternary Half Adder (THA) circuit that was constructed utilizing CMOS permits a 52% reduction in the total number of transistors. Constructed using CNFET, the THA exhibits a latency of 27 picoseconds, which is 87% lower than its CMOS counterparts, while consuming 2.4 picowatts of power, 11% less than CMOS alternatives. On the other hand, the CGOT THA has a latency of just 101 picoseconds, which is 51% lower than a comparable CMOS design, and it uses only 1.26 microwatts of power, which is 53% less than CMOS in the ultra-low power domain. In conclusion, when compared to the CMOS THA, the proposed CNFET and CGOT THA circuits show an overall drop in Power Delay Products (PDPs) that is 88% lower and 77% lower, respectively, then the CMOS THA.

Hasan et al. [23] suggested a hybrid Full Adder (FA) cell that makes use of a mix of the Gate Diffusion Input (GDI) technology, the Transmission Gate (TG), and conventional Static CMOS (C-CMOS) logic. To evaluate different performance metrics, a simulation was performed using Cadence Virtuoso in the 65 nm technology at the initial stage. Furthermore, this study includes a comparative evaluation of the suggested FA design with 13 currently available state-of-the-art FAs to analyse the performance enhancements achieved by the proposed FA. The purpose of this research is to observe the improvements in performance obtained by the proposed FA. Furthermore, to assess the performance of these adders and determine their applicability in larger structures, both the proposed and existing

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FAs were combined to form 4-bit, 8-bit, 16-bit, and 32-bit adders. In conclusion, the design that was suggested demonstrated outstanding performance both when operating in single cell mode and while operating in cascaded mode. Transmission Gate (TG) and hybrid CMOS Field Avalanche designs were suggested by Mewada et al. [24]. The introduction of this research paper outlines a newly developed design technique called "triplet design". The purpose of this design approach is to enhance the performance of TG and hybrid CMOS FA designs in chain and tree architectures, without requiring the use of buffers. Furthermore, this study introduces two novel hybrid CMOS FA designs that are specifically suitable for the triplet design approach. In order to construct 4-, 8-, and 16-bit Ripple Carry Adders (RCA) and multipliers, we selected to use six distinct FA designs (TG and hybrid CMOS FAs). Additionally, we investigated the potential for improvement in PDP by using a triplet design technique.

3. Proposed method

Adders, being the fundamental building blocks of any integrated circuit, play a crucial role in determining the performance of numerous applications, and their effectiveness is crucial to the overall success of such applications. This section provides in-depth information about the implementation of fundamental full adders, such as MFA and COPFA. The carry selection logic attributes of MFA and COPFA were utilized in developing an additional 4-bit PSHA module. To ensure optimal performance, both FinFET and GnrFET technologies are utilized in the design process of every adder. The generation of advanced carry-output is not achievable through the MFA operation, which could potentially cause a delay in the production of sums. As a result, COPFA was designed with the capabilities of improved carry generation achieved by prediction operations. Also, the COPFA, which was created with the help of GnrFET and FinFET technology, is a key component for all of the adders

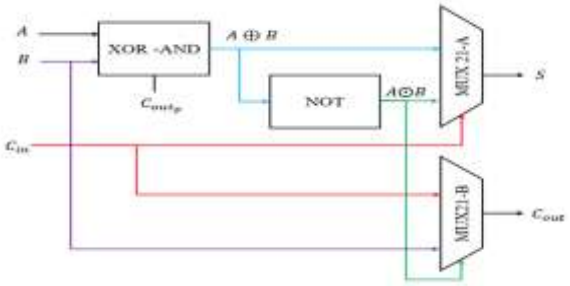

Figure 1. Block diagram of COPFA

The operational diagram of COPFA is presented in Figure 1, which contains A,B,C_in as one-bit inputs S,Cout and carry-out predicted (C(outp)) as one-bit outputs. The value of C(outp) is produced by performing an AND operation between the values of A and B, which is a useful technique for efficiently generating sums in multi-stage addition processes. The estimation of C(outp) is faster than that of the regular Cout and is particularly advantageous for generating sums in cascade systems. The sum and carry-out values produced by the COPFA are similar to those generated by the MFA.

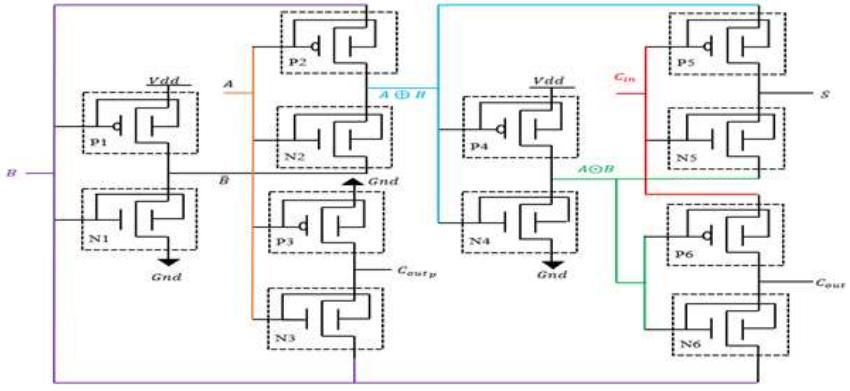

Figure 2. FinFET modelling of COPFA

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Figure 2 illustrates the FinFET-based transistor level layout of the COPFA architecture, which includes an equal number of N-MOS FinFETs and P-MOS FinFETs. The combination of P1-N1 FinFETs is responsible for performing the inverter operation on the input signal B, resulting in the generation of its complement, $\overline{B}$. The combination of P2-N2 FinFETs executes the XOR operation on A and B, resulting in the output A⊕B. The P3-N3 FinFETs combination performs the AND operation between A and B, which produces the output C(outp). The combination of P4-N4 FinFETs functions as an inverter for the output A⊕B, resulting in the output A⊙B. The P5-N5 FinFETs combination acts as a 2:1 MUX with A⊕B and A⊙B as the data inputs and Cin as the selection input, ultimately producing the output sum. Similarly, the P6-N6 FinFETs combination functions as a 2:1 MUX with Cin and B as the data inputs and A⊙B as the selection input, ultimately producing the carry-output.

The block diagram of a 4-bit PSHA is presented in Figure 3, depicting the inclusion of manual carry selection operation carried out using Psel. In this design, the MUX21 component is enhanced to enable the selection between regular carry out (Cout) and predicted carry out (C(outp) using Psel.

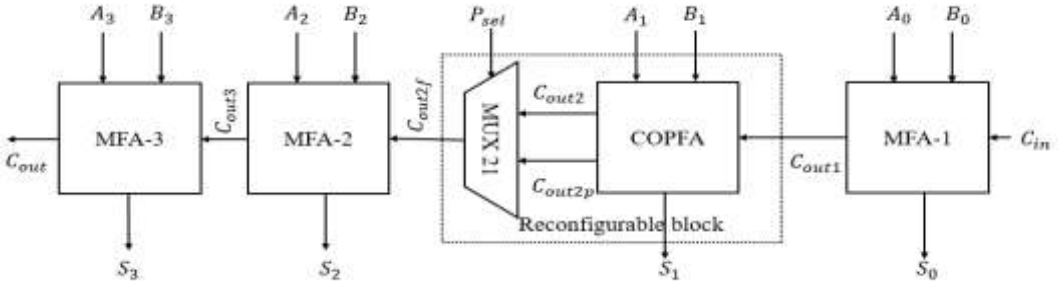

Figure 3. Proposed 4-bit PSHA.

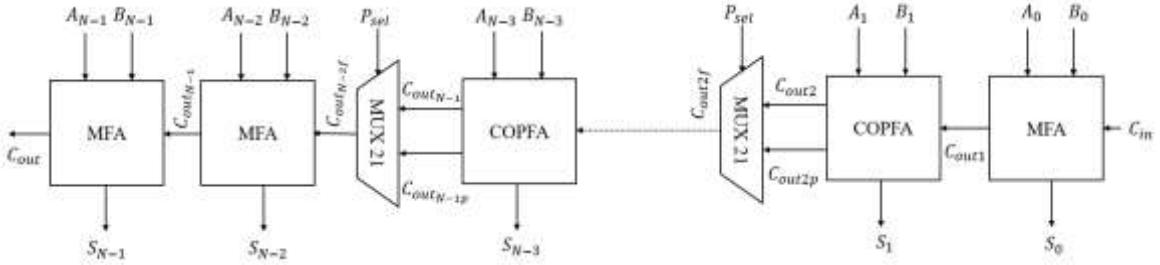

Figure 4. Proposed N-bit PSRHA.

The block diagram depicted in Figure 4 represents an N-bit PSRHA, which operates in a similar fashion to the PSHA, but with N bits of input and output. Initially, the inputs A0, B0, and Cin are fed into MFA-1, resulting in the production of output signals S0 and Cout1. Next, the inputs A1, B1, and Cout1 are fed into the COPFA module, which generates the output signals S1, Cout2, and Cout2p. Furthermore, the output signal Cout2 is used as data input-0, Cout2p is used as data input-1, and Psel is employed as the selection input for the MUX21 . In this system, when Psel is set to zero, the MUX21 component selects Cout2 as the output signal, resulting in the production of Cout2f through the high-delay path. Similarly, when Psel is set to one, the MUX21 component selects Cout2p as the output signal, leading to the generation of Cout2f via the low-delay path. Afterwards, the inputs A2, B2, and Cout2f are fed into MFA-2, resulting in the production of output signals S2 and Cout3. Finally, the inputs A3, B3, and Cout3 are fed into MFA-3, resulting in the production of output signals S3 and Cout, which serve as the final output signals of the N-bit PSRHA. The PSRHA is constructed by replicating the MUX21 and COPFA modules multiple times to enable the processing of N-bit inputs and generation of corresponding N-bit outputs.

4. Results

In the next part, a comprehensive simulation performance study of suggested adders is presented utilizing a wide variety of parameters. The effectiveness of the proposed MFA, COPFA, and 4-bit

PSHA is evaluated and compared to traditional adders by analyzing a range of performance metrics. The HSPICE software tool is used in the process of designing and simulating the different designs, and Table 1 provides an overview of the simulation environment data that are utilized by the HSPICE tool.

Table 1. Simulation properties.

Parameter	Value
Fin FET technologies	$7nm, 10nm, 14nm, 16nm\ and\ 20nm$
Channel Length (L)	$7nm, 10nm, 14nm, 16nm\ and\ 20nm$
Thickness of front or back gate oxide	$1.2nm$
fin Thickness (Si)	$4\ nm$
fin height (h_{fin})	$7nm, 10nm, 14nm, 16nm\ and\ 20nm$
Work function	$4.5eV/4.9eV$
Power supply (V DD)	$1\ V$
Channel doping	$2\ x\ 10^{20}\ cm^{-3}$
Source/ Drain doping	$2\ x\ 10^{20}\ cm^{-3}$

4.1 Performance evaluation

The performance of the proposed system is evaluated using various performance metrics, including PD, TC, SPC, TEC, SNM, COFD, CORD, SFD, SRD, and APC. In Table 2, a comparison is made between the features of the proposed COPFA and those of conventional full adders, such as MFA [21], CTFA [19], IMC-FA [18], HFFA [17], and RHMFA [16]. Traditional full adders lacked the ability to select the high-speed carry output path, resulting in higher path delays compared to the proposed adders. The power consumption of conventional full adders is higher than that of CMOS full adders because conventional full adders have a greater number of transistors and are implemented using CMOS. The suggested COPFA module lowered by TEC by 24.44%, TC by 23.692%, COFD by 57.06%, SFD by 23.0578%, and APC by 23.08% in compared to standard MFA [21].

Table 2. Proposed COPFA Comparison with conventional full adders.

Method	COPFA	MFA [21]	CTFA [19]	IMC-FA [18]	HFFA [17]	RHMFA [16]
TEC (nJ)	0.9077	1.2013	5.089908	25.45166	31.93173	38.33638
TC (nA)	5.2231	6.8448	29.00142	30.00008	34.15361	41.72174
COFD (ps)	1.0385	2.4185	10.24718	46.05195	50.23387	52.85658
SFD (ns)	15.223	19.785	83.82905	84.50273	84.65102	92.32847
APC (nw)	1.3184	1.714	2.262218	8.384	10.3798	12.00003

Table 2.1. Percentage improvement of COPFA comparison with conventional full adders

Method	MFA [21]	CTFA [19]	IMC-FA [18]	HFFA [17]	RHMFA [16]
TEC (%)	24.4402	82.1667	96.4336	97.1574	97.6323
TC (%)	23.6924	81.9902	82.5897	84.707	87.4811
COFD (%)	57.0602	89.8655	97.7449	97.9327	98.0352

SFD (%)	23.0579	81.8404	81.9852	82.0168	83.5121
APC (%)	23.0805	41.7209	84.2748	87.2984	89.0134

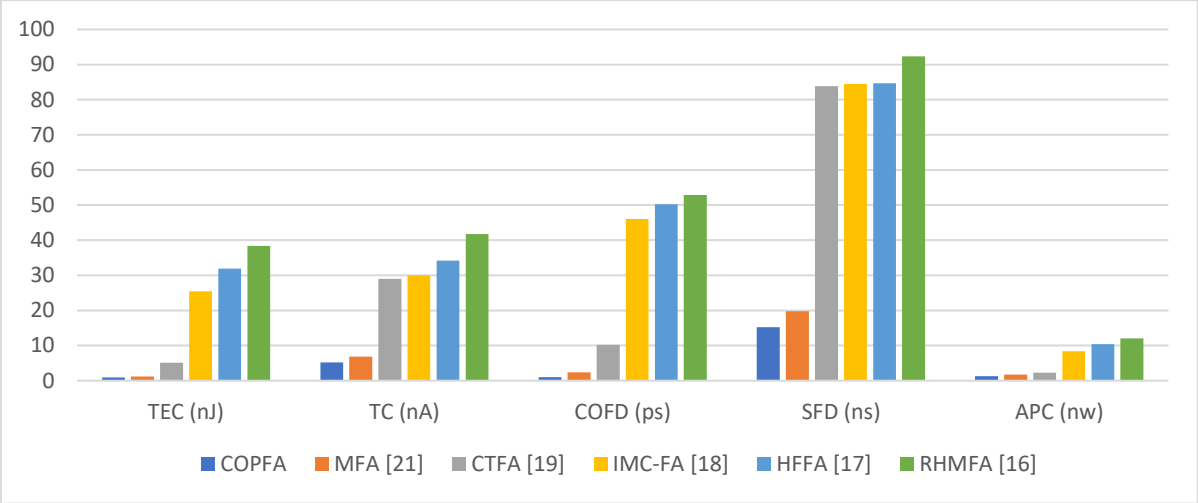

Figure 5. Parameters of hardware resource using proposed and conventional full adders

Table 3 compares the performance of the proposed PSHA with that of conventional adders, such as RCA [19], CTA [20], IMCA [18], and HFA [17]. The proposed PSHA outperformed traditional adders in terms of power, delay, and area metrics due to the high-speed carry-out selection provided by COPFA, which was not available in traditional adders. When compared to traditional RCA [19], the COPFA module that was presented had the effect of lowering TEC by 31.93%, TC by 29.03%, COFD by 29.07%, SFD by 28.98%, and APC by 29.08%.

Table 3. Proposed PSHA Comparison with existing adders.

Method	PSHA	RCA [19]	CTA [20]	IMCA [18]	HFA [17]
TEC (nJ)	0.09121	0.134	9.060036	45.30395	56.83848
TC (nA)	3.19587	4.555	51.62253	53.40014	60.79343
COFD (ps)	19.7847	27.897	18.23998	81.97247	89.41629
SFD (ns)	25.0352	35.268	149.2157	150.4149	150.6788
APC (nw)	2.74026	3.864	4.026748	14.92352	18.47604

Table 3.1. Percentage of PSHA in comparison with conventional full adders.

Method	RCA [19]	CTA [20]	IMCA [18]	HFA [17]
TEC (%)	31.9328	98.9933	99.7987	99.8395
TC (%)	29.8382	93.8092	34.0152	99.8395
COFD (%)	29.0795	8.468869	75.8642	77.8735
SFD (%)	29.0144	83.2221	83.3559	83.3851
APC (%)	29.0823	31.9486	81.638	85.1686

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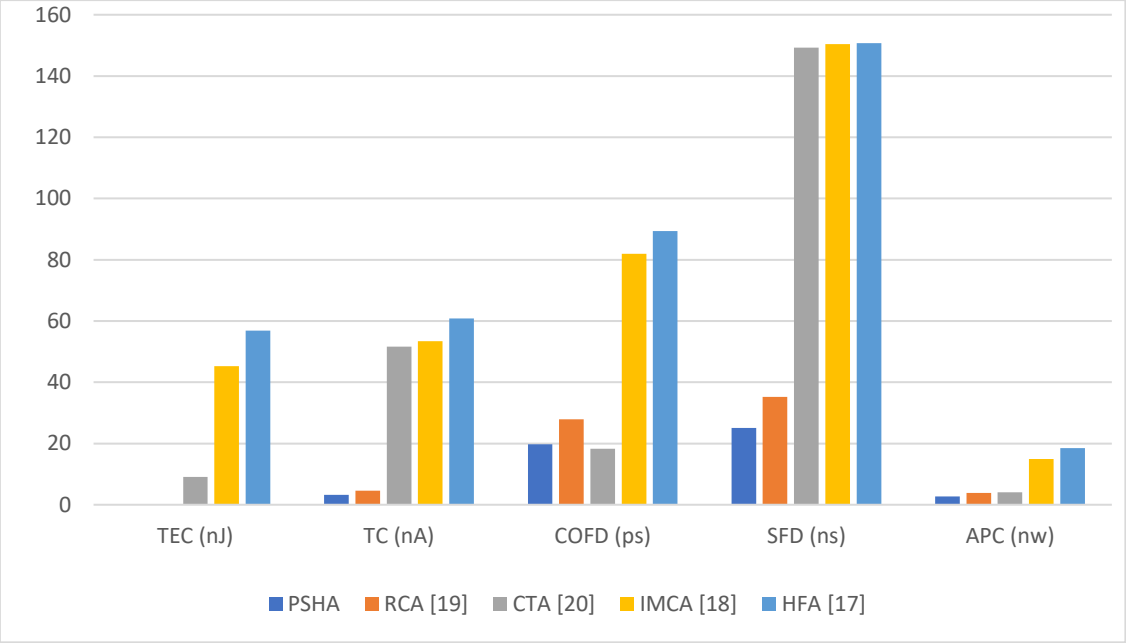

Figure 6. Parameters of hardware resource using proposed and existing adders

5. Conclusion

In this article, designs for COPFA, PSRHA MFA, that make use of FinFET and GnrFET technology are proposed. The COPFA was designed with multiplexer selection logic that enables the user to choose between the sum output with minimal delays or the high-speed carry output. Then, PSRHA was constructed by utilizing the COPFA module. This module, which allows for a speedy selection of carry-outputs, has reduced the amount of time that routes are delayed as well as the amount of power that is used. The results that were acquired using the COPFA module were as follows: TEC of 0.9077nJ, TC of 51.038nA, COFD of 1.038 ps, SFD of 15.223ns, APC of 1.3184 nw. Likewise, the PSRHA module generated TEC values of 0.09121nJ, TC values of 3.19587 nA , COFD values of 19.7847 ps . SFD values of 25.0352ns, APC values of 25.0352nw. In addition, the standard adders are beaten by the proposed MFA, COPFA, and PSRHA in terms of metrics for delay, power, and energy. However, the primary focus of this investigation is on the evolution of adder modules alone; real-time applications such as ALUs are not taken into consideration. Therefore, advanced ALU operations may be achieved by using the architecture that was recommended and the extension that was developed .

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