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HIGH PERFORMANCE CIRCUITS

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***Abstract*: The constant reduction in size of CMOS technology to nanometers is causing problems in circuit performance and energy scaling. At the same time, the scaling of future workloads is increasing rapidly, creating a mismatch between the capabilities of CMOS technology and the demands of future applications. In such a scenario, one can either accept computing systems that are sufficient or look for alternative modifications to advance without relying on technology progress. Two possible approaches to bridge this gap are area reduction and approximate computing. The latter is an interesting area for achieving energy efficiency in computing intensive applications like visual processing and multimedia signals that do not require high accuracy. One way to achieve this is by using approximate multipliers, which can reduce energy consumption by up to 70% and have lower EDP compared to existing designs. This project proposes two novel designs for approximate multipliers, which were simulated using Cadence digital labs and mapped onto TSMC 180nm technology with a slow library using Cadence RTL complier V 7.1**

Keywords:Approximateadders,Approximate multipliers, error %, low power

1. INTRODUCTION

With the rise of an ever increasing number of complex applications in areas like AI and media preparing , the general computational outstanding tasks at hand of the applications and their separate vitality utilization are on the ascent. Applications from the spaces of Wub od thins(IoT) and digital physical frameworks(CPS) that include gigantic measure of information examination require a huge measure of computational and in this way vitality and force assets. Now a day as technology is advancing, the high speed and less area and less power consuming systems are preferred for better efficiency. But the problem is the speed and area of the area of the systems is inversely proportional as for high speed systems the hardware of the system increases. To overcome this approximate computing is introduces. As human eye does not have the tendency to detect variation in the results within images and videos. By considering this fact approximate circuits were proposed in applications like digital signal processing(DSP),Artificial intelligence(AI), and image processing and so on. Arithmetic circuits are the main building blocks of these applications, so that so many researches use these blocks to enhance efficiency.

2. APPROXIMATE ADDERS

Digital computing systems heavily rely on binary arithmetic operations like addition, subtraction, multiplication, and division. These operations are built upon adders, which serve as the fundamental building blocks. Adders are crucial in multimedia applications, but they are subject to constraints like area, power, and delay, which depend on their architecture. Among the traditional adders, Ripple Carry Adder (RCA) is the simplest to construct and takes up less area, but it suffers from higher delay. Since area and power consumption are directly related, parallel

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prefix adder consumes more power than RCA. Unfortunately, none of the traditional adders meet the design metrics of low delay and low power consumption. To improve delay and power design metrics, accuracy can be sacrificed. Many error-resilient techniques have been proposed previously to improve delay and power. Approximate computing aims to implement hardware and software systems by compromising accuracy. Approximate adders fall into four categories, which are Speculative adders, Segmented adders, Carry select adders, and approximate full adders.

Approximate Full Adders

Approximate Adders contain two sub adders blocks. Higher order bits contain approximate adder block. FIG 2.1.1 shows the approximate adder block design. In approximate sub adder block the approximate full adders are used as shown in fig 2.1.1 Lower-part-OR Adders(LOA) and approximate full adder designs were introduced by modifying the conventional full adder circuit.

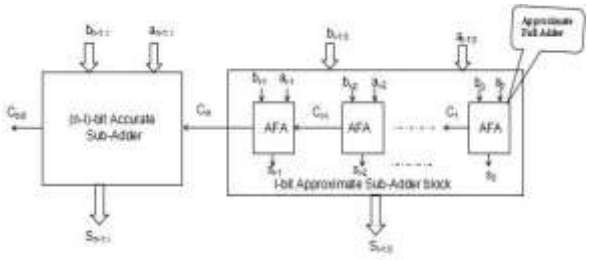


Fig2.1Block diagram for Approximate full adder

2.1.1 Approximate Full adder Design 1

A modified version of the full adder architecture, called the approximate full adder (AFA), has been proposed. In this version, the carry circuit has been modified. The equations for the full adder can be written as

$$Sum = A \oplus B \oplus Cin \text{ .....} \quad (2.1.1)$$

$$Cout = A.B + B.Cin + Cin.A \text{.....} (2.1.2)$$

The adder takes A, B, and Cin as inputs, and outputs Sum and Cout as the sum and carry out, respectively. The typical gate-level implementation of the full adder is illustrated in the fig (2.1.1)

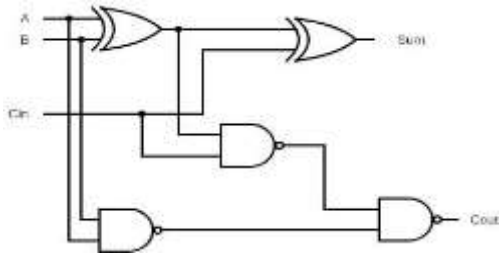


Fig 2.1.1 Full Adder- Gate Level Implementation

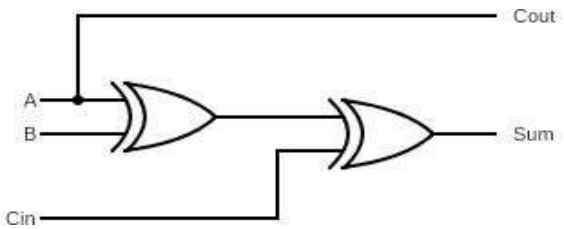
To construct an N-bit ripple carry adder, N full adders are arranged in a series. The carry is transmitted from the least significant bit to the most significant bit, resulting in more delay despite RCA having less area and power consumption. Since the carry circuit has been modified, the delay has increased. As a result, four different approximate full adder designs have been proposed by modifying the carry circuit.

In the Approximate full adder Design #1 the sum has been taken as accurate one and the carry is taken as the 'A' i.e, the equation for sum and carry are

$$Sum = A \oplus B \oplus Cin \text{ ..... } (2.1.3)$$

$$Cout = A \text{ ..... } (2.1.4)$$

Design #1 of the approximate full adder is illustrated in the figure. (2.1.2)



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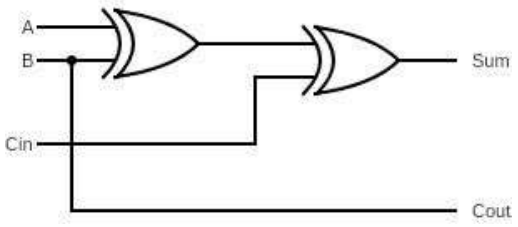
2.1.2 Approximate Full Adder design #1

2.1.3 Approximate Full Adder Design 2

Design #2 of AFA, illustrated in figure 2.1.3, uses B as the carry out and provides an accurate sum.

Cout = B



2.1.3 Approximate Full adder Design #2

Although AFA designs #1 and #2 result in reduced delay, they have a higher circuit error. AFA designs #3 and #4 were created to minimize the error and improve circuit performance.

2.1.4 Approximate full Adder Design #3

In AFA Design #3 shown in fig 2.1.4 the carry out is taken as Cout = A.B

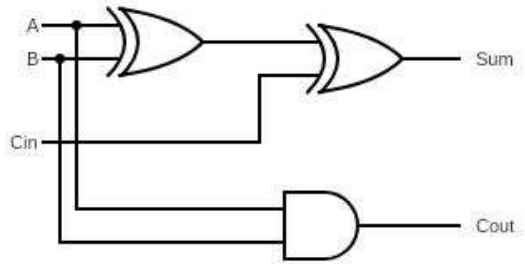


FIG 2.1.4 Approximate full adder design #3

2.1.5 Approximate full adder design #4

In AFA Design #4 shown in fig 2.1.5 the carry out is taken as Cout = A+B

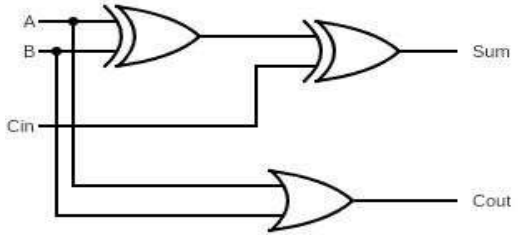


Fig 2.1.5 Approximate full adder design #4

The AFA consists of four designs that are more efficient than conventional adders in terms of reducing delay, area, and power consumption. The main focus of these designs is on the carry part, while the sum remains unchanged. The table below compares the correct and incorrect values of the carry between the Full Adder and the four Approximate Full Adder designs. Since the sum values of the AFA designs are accurate, only the carry values are being compared. The truth table includes data for both the FA and AFA designs.

Inputs			Accurate o/p		AFA#1		AFA#2		AFA#3		AFA#4	
A	B	Cin	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	1×	1	0	1	1×
0	1	1	0	1	0	0×	0	1	0	0×	0	1
1	0	0	1	0	1	1×	1	0	1	0	1	1×
1	0	1	0	1	0	1	0	0×	0	0×	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1
Cout to be correct						0.75		0.75		0.75		0.75

The above table shows the probability of carryout to be correct is always 0.75%
Consider the below example
A – 1011010110101101
B – 1010110101010011
Example of approximate adders

Accurate Sum	10110001100000000(90880)
AFADesign-1 sum	10110001010100100(90788) Error is 0.1%

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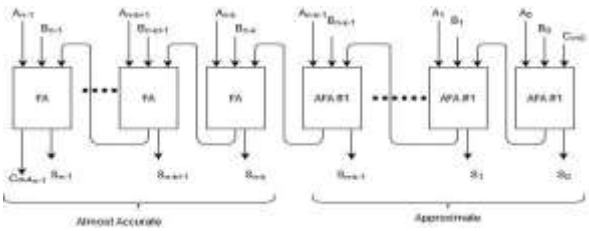
AFADesign-2 sum	10110001001011000(90712) Error is 0.18%
AFADesign-3 sum	10110001011111100(90876) Error is 0.004%
AFA Design4 sum	10110001000000000(90624) Error is 0.28%

Inputs			Accurate O/P		Approximate proposed outputs	
A	B	Cin	Cout	S	Cout	Sum
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	1×	1
0	1	1	1	0	1	0
1	0	0	0	1	1×	1
1	0	1	1	0	1	0
1	1	0	1	0	1	1×
1	1	1	1	1	1	0×
Probability of the sum and Carry to be Correct					0.75	0.75

The example given above indicates that the error does not depend on individual bits, but rather on the entire number. Therefore, even though the output is 1011111100 instead of 1100000000, the error is only 0.004%. This is because the accurate parts/bits mostly cancel out the error. The development of N bit RCA was made possible by using these approximate adders. The figure below illustrates an approximate adder that uses both half accurate and half approximate designs.

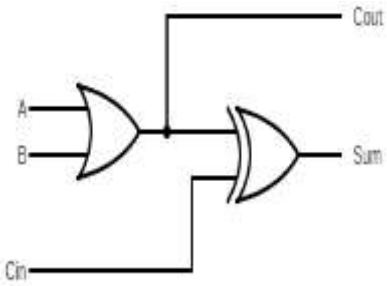


Proposed Work :

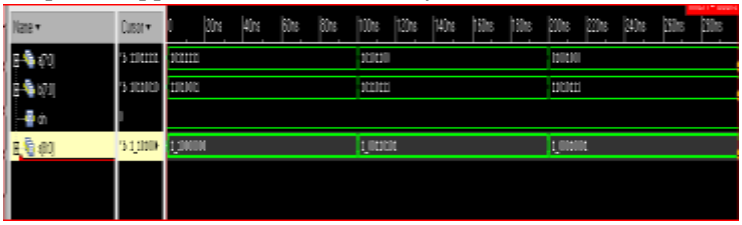
In the proposed work the sum is EX-OR with Cin and Carry is sum of two inputs A & B

Sum = (A+B) ⊕ Cin

Carry = A+B



Proposed Approximate Adder Waveform :



Examples of proposed work

Inputs	Accurate Sum	Proposed Approximate Sum	Error %
A-11011111 B-01110000	101001111(335)	101010001(337	0.59
A-10111111 B-11010001	110010000(400)	110010001(401	0.25
A-10101100 B-11010001	101111101(381)	110000111(391	2.62
A-10101100	101100011(355)	101100001(353	0.56

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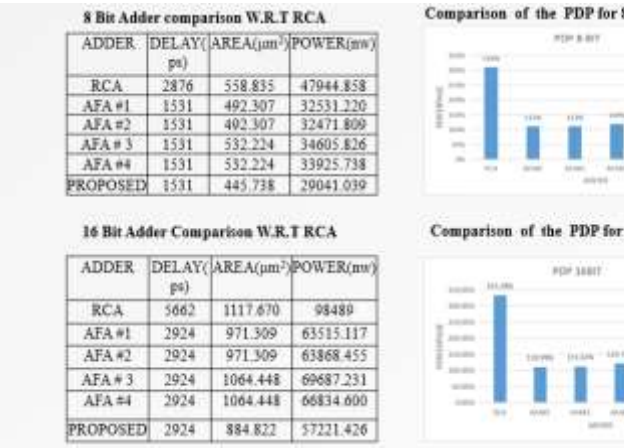
B-10110111			
A-11011111 B-10110010	110010001(401)	110010001(401	0

Comparison :



3. APPROXIMATE MULTIPLIERS

The fundamental building block for processing signals, images, and videos is multiplication, but it is associated with complex circuitry and high power consumption. The process of basic multiplication involves three stages: partial product generation, reduction of partial product, and the addition of partial products with carry propagation. At any of these three stages, approximation may be utilized. There are four types of approximate multiplication processes that can be identified.

i).**Approximation in generating the partial products**

Among the three stages of multiplication process, the first stage is generation of partial products. By modifying the K-map the logic error is introduced in generation of the partial products.

ii). **Approximation in the partial product tree**

The approximation can be introduced in the partial product matrix. By eliminating the some of the partial products so that complexity of the circuit is reduced

3.1 Introducing Approximate compressors in the partial product tree.

Reduction of partial product stage is a main critical block in multiplier, compressors are used for this process. But compressors are XOR rich circuits, which uses more area and power. By considering this fact approximation were introduced in the compressors circuit. By considering this fact approximation were introduced in the compressors circuit .

3.1.1Exact 4-2 Compressor

Compressors have the function of tallying the amount of "1's" in inputs. An exact 4:2 Compressor is created through the utilization of two full adders, and it possesses three outputs and five inputs. The equation outlines the precise function of the 4:2 compressor.

A+B+C+D+Cin=2(Cout+Carry)+Sum……(3.1)

Where A,B,C,D and Cin are the inputs and Carry,Cout and Sum are the outputs of the compressor.

The expression for the three outputs for the exact 4:2 compressor is

$$Sum = A \oplus B \oplus C \oplus D \oplus Cin$$

$$Cout = (A \oplus B) \cdot C + \overline{(A \oplus B)} \cdot A$$

$$Carry = (A \oplus B \oplus C \oplus D) \cdot Cin + \overline{(A \oplus B \oplus C \oplus D)} \cdot D$$

From the fig 3.1 it is illustrated that the accurate 4:2 compressor uses two full adders, which utilize more power and area. So many approximate 4:2 compressor designs are proposed previously to improve the delay, area and power by compromising the accuracy

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Cin	D	C	B	A	Cout	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

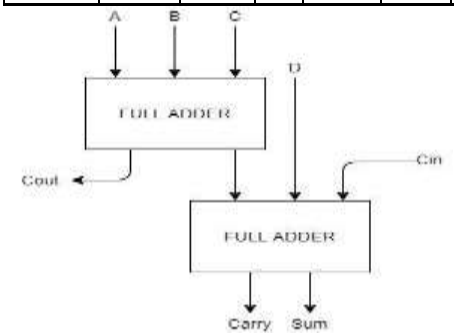

Fig 3.1 Block diagram of Exact 4:2 Compressor

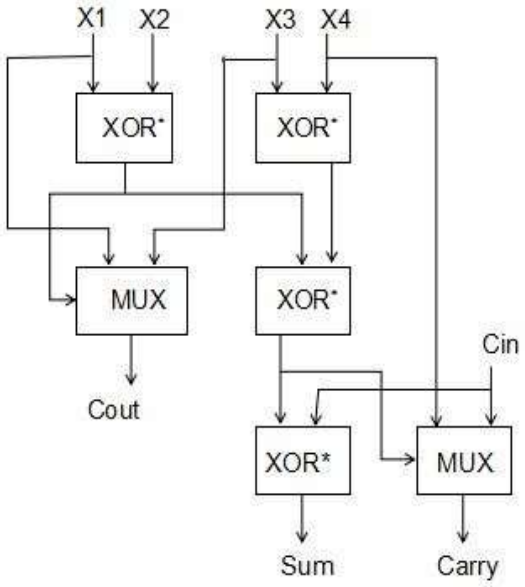

Fig 3.2 Modified Accurate 4:2 Compressor

The modified accurate 4:2 compressor has the lesser delay compared to exact 4:2 compressor.

Truth Table for Exact 4-2 Compressor

3.2.1 Approximate 4:2 compressor Ref[11]

The Approximate 4:2 compressor implemented by redesigning the gates in the hardware circuit of the exact 4:2 compressor. Here Cin and Cout is ignored in the hardware design to decrease the complexity and power utilization. The below figure shows the gate level implementation of the 4:2 approximate compressor Ref[11] and below expressions illustrates the output.

$$Sum = \overline{(A \oplus B + C \oplus D)}$$

$$Carry = \overline{(A + B + C + D)}$$

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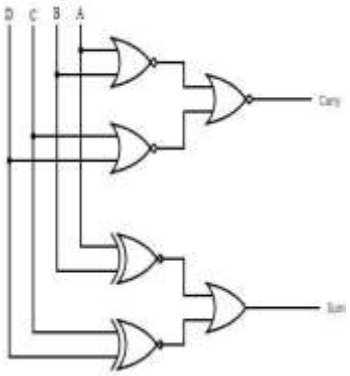
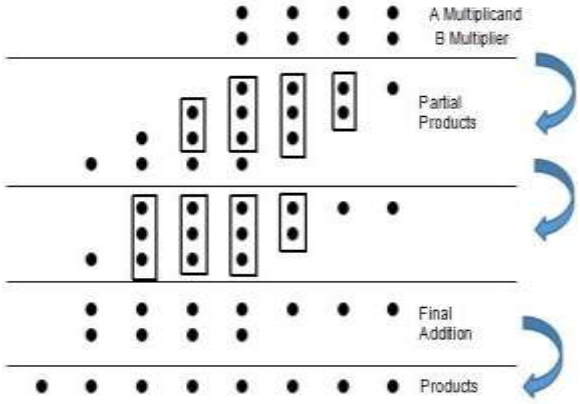


Gate level implementation of 4:2 compressor

4. Proposed Designs :

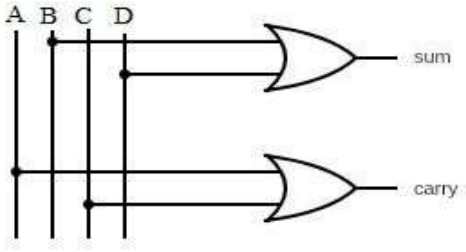
Basic multipliers undergo three stages : Generation of partial product,reduction of partial product and addition of the partial products. In any of these three stages the approximation is introduced



In partail product generation by eleimanting lower order terms the approximation is introduced.For reducing the partail products compressors are used.As the traditional compressors are XOR rich circuits, consumes more area and power, many approximate compressors were introduces previously.As reducing the partail products is more complex and consumes more power,the 4:2 compressors can be taken into count todo the approximation.

4.1 Proposed Aprroximate 4:2 Compressor

The suggested approximate 4:2 compressor can be built with a reduced amount of hardware circuitry, requiring solely two 2-input OR gates. The diagram displays the suggested 4:2 compressor.



The compressor provides the solution by tallying the quantity of ones. The operation of the compressor that has been suggested is as follows.

Sprop = Sum + Carry …… (4.1)

The proposed compressor equation is shown below

Carry = A+ C …….. (4.2)

Sum = B + D ……..(4.3)

Upon comparison with the existing designs, it can be observed that the suggested compressor has a smaller area and delay. Additionally, the error rate is moderate.

Based on Table 4.1, the proposed compressor has a total probability of error of 31/256.

4.2 Approximate Multiplier Design-1

In order to minimize the partial products in a multiplier, compressors are employed. When utilizing approximate compressors to decrease partial products, the analysis focuses on the most significant bits for precise calculations, and exact 4:2 compressors are utilized. As the MSB bits have greater significance, if approximate compressors were employed on the MSB side, the error rate would be higher. For the rest of the partial products, the proposed approximate compressor is used, specifically on the LSB side.

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The Fig 4.2 shows the approximate multiplier design

Inputs				Exact	Proposed 4:2 compressor				
A	B	C	D	S	Carry	Sum	S_{prop}	E	P(E)
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1	0	0
0	0	1	0	1	1	0	1	0	0
0	0	1	1	2	1	1	2	0	0
0	1	0	0	1	0	1	1	0	0
0	1	0	1	2	0	1	1	1	9/256
0	1	1	0	2	1	1	2	0	0
0	1	1	1	3	1	1	2	1	3/256
1	0	0	0	1	1	0	1	0	0
1	0	0	1	2	1	1	2	0	0
1	0	1	0	2	1	0	1	1	9/256
1	0	1	1	3	1	1	2	1	3/256
1	1	0	0	2	1	1	2	0	0
1	1	0	1	3	1	1	2	1	3/256
1	1	1	0	3	1	1	2	1	3/256
1	1	1	1	4	1	1	2	2	1/256
The total probability of error P(E)									31/256

Table 4.1 shows the probability error

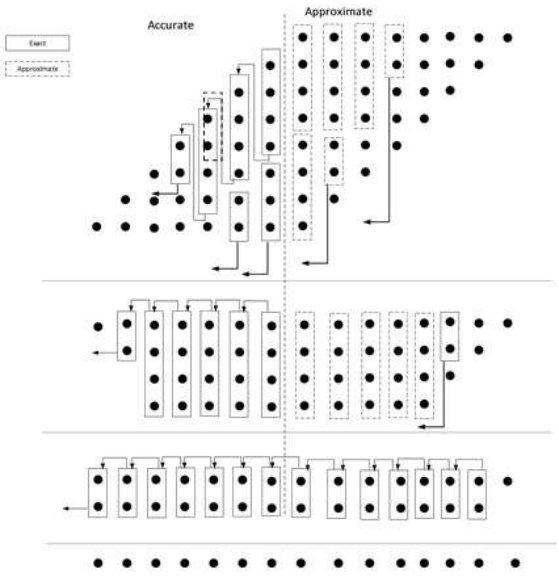

Fig 4.2 Approximate mutliplier

The proposed 4:2 compressor is used in the approximate multplier design the error comparsion is as shown in the the table

Multiplier	Input 1 a-00001011(11) b-00101010(42) Exact-462		Input 2 a-10110001(177) b-00111001(57) Exact-10089		Input 3 a-11101000(232) b-00111011(59) Exact-13688	
	Product	%E	Product	%E	Product	%E
Ref[11]	558	20	10281	2	13560	1
Proposed design-1	450	2.73	10457	3.64	14000	2.27

Results and discussions :

The design architectures were constructed using Verilog HDL and evaluated through simulation utilizing Cadence Digital Labs. The designs were then mapped onto TSMC 180nm technology using a slow library and operated under conditions of 1.8v and 25°C, all accomplished through the use of Cadence RTL Compiler.

Comparison of different 4:2 compressor with exact compressor

4:2 Compressor	Delay (ps)	Power (nW)	Area (μm^2)	Energy (zJ)	EDP (zJ.ps)	Err rate
Exact	6000	15166.887	70	91001322	54.6×10^{10}	0
Ref[11]	1306	1949.708	53	2546318.648	0.33×10^{10}	100/256
Proposed	**1200**	**694.821**	**27**	**833785.2**	**0.1×10^{10}**	**31/256**

From the table it observed that the proposed 4:2 compressor has less delay , power and are when compared to with the exact, existed aprroximate 4:2 compressord. The delay of the proposed compressor is only 20% when compared with the exact compressor. The proposed 4:2compressor consumes 4.58% power and 30% area when compared with the exact compressor

Conclusion :

A novel approximate 4:2 compressor has been suggested, which has a smaller area and delay. The proposed compressor is constructed using

straightforward hardware circuitry and exhibits lower error rates compared to existing approximate compressors. The results demonstrate that the approximate multiplier utilizing the proposed 4:2 compressor has a smaller area, lower power consumption, and reduced delay. Furthermore, the complexity of the multiplier circuit has been decreased. An Approximate Full Adder (AFA) has been suggested by making modifications to the traditional design, which yields the same or lesser error rate compared to existing AFA designs. Based on the examples, it can be inferred that even when both the sum and carry circuits are approximated, the overall error of the circuit is not significantly impacted. This is because the error does not solely depend on the individual bits of the number, but rather on the number as a whole.

References:

1. Sreehari Veeramachaneni, Kirthi M,Krishna Linagamaneni Avinash sreekanth Reddy Puppala M.B. srinivas,"Novel Architectures for High-Speed and -Power 3-2,4-2 and 5-2 Compressors," 20th International Conference on VLSI Design , Jan 2007, Pp.324-329
2. Sunil Dutt, Sukumar Nandi and Gaurav Trivedi, "Analysis and Design of Adders for Approximate Computing", in ACM Transactions on Embedded Computing Systems, vol. 17, no. 2, pp. 40:1 – 40:28, 2017.
3. A. K. Verma, P. Brisk, and P. Ienne, "Variable latency speculative addition: A new paradigm for arithmetic circuit design," In DATE, pages 1250 -1255, 2008
4. Tongxin Yang Tomoaki Ukezono Toshinori Sato, "A Low-Power Configurable Adder for Approximate Applications",IEEE International symposium on circuits and systems(ISCAS), May 2018
5. H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-Inspired Imprecise computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications," IEEE Trans. Circuits Syst., 2010
6. N. Zhu, W. L. Goh, and K. S. Yeo. "An enhanced low-power high-speed adder for error-tolerant application". In ISIC 2009, pages 69-72, 2009