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DESIGN AND SIMULATION OF LDO REGULATOR WITH LOW QUIESCENT CURRENT IN 90nm TECHNOLOGY

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ABSTRACT
Low Dropout (LDO) Voltage Regulators are crucial components in modern electronic systems due to their ability to maintain a stable, low-noise DC output voltage even when the input voltage is marginally higher than the output. This compact linear regulator architecture integrates key modules including an error amplifier, pass element (typically a PMOS transistor), a precise voltage reference source, and a feedback voltage divider network.
In this design, the error amplifier—realized using standard 90nm CMOS technology—operates at a supply voltage of 1.6 V and delivers a high voltage gain of 74 dB. Its role is to sense deviations in the output and correct them by modulating the pass device, ensuring tight regulation across varying input and load conditions. A bandgap reference circuit is deployed to generate a temperature-independent reference voltage of 1.6 V, enhancing reliability across environmental variations.
The LDO consistently provides an output voltage of 1.64 V when supplied with input voltages ranging from 1.8 V to 3.5 V, demonstrating low dropout operation and superior line and load regulation characteristics. The design not only optimizes performance for low-voltage, low-power applications but also emphasizes robustness in maintaining output stability under dynamic conditions. This makes it ideal for sensitive analog and mixed-signal integrated circuits where power integrity is essential.

I. INTRODUCTION

Low Dropout (LDO) Voltage Regulators are essential in modern SoC designs, offering stable, low-noise power supplies critical for precision analog and digital blocks. Their ability to regulate output with minimal voltage headroom makes them suitable for powering sensitive circuits like RF front-ends and low-voltage digital cores [12]. As SoCs integrate diverse functional units—ADCs, RF modules, CPUs, and memory—power delivery demands become more stringent. Even minor supply variations can lead to signal distortion or system faults. LDOs are preferred in such settings due to their low output noise and fast transient performance, unlike switching regulators that can introduce EMI [14]. Yet, conventional LDOs struggle under tight noise rejection and low quiescent current demands.

A. Power Integrity and PSRR Limitations

A key performance metric in LDOs is the Power Supply Rejection Ratio (PSRR), indicating the regulator's ability to attenuate supply noise. While traditional designs perform well at low frequencies, PSRR deteriorates above several hundred kilohertz due to amplifier bandwidth limitations and

layout parasitic [10]. In high-speed digital and RF circuits, power rails are exposed to significant noise from clocking and data activity. Without strong PSRR, this noise couples into analog paths, degrading performance [1]. Thus, high-frequency PSRR becomes critical, particularly for portable and mixed-signal applications where low power and high noise immunity are both required.

B. Quiescent Current and Efficiency Considerations

Quiescent current refers to the internal bias current consumed when the load is light or zero. Minimizing this current is vital for battery-driven and IoT systems to ensure extended standby operation [7]. However, reducing quiescent current often compromises dynamic performance, including transient response and PSRR. To address this, modern LDOs employ:

- Adaptive biasing that scales current with load activity,
- Gain-boosted amplifiers to retain bandwidth at low power,
- Cascode and feedforward paths for noise suppression,
- Flipped voltage follower (FVF) topologies to lower output impedance and isolate noise sources.

These circuit innovations help balance power efficiency with robust regulation [4].

C. 90nm CMOS Technology Benefits

Designing LDOs in 90nm CMOS offers an effective trade-off between integration capability and analog performance. Although finer nodes exist, 90nm provides well-characterized models, lower leakage, and good analog compatibility. Advantages include:

- Lower threshold voltages enabling minimal dropout operation,
- Higher transistor gain-bandwidth, beneficial for error amplifiers,
- Support for both thin and thick oxide devices for varied voltage paths,
- Improved parasitic control for better PSRR and layout fidelity.

Furthermore, 90nm remains widely used in industry for analog-mixed signal integration, making it suitable for LDO development in both research and commercial environments [13].

II. LITERATURE SURVEY

A. REVIEW OF ON-CHIP POWER MANAGEMENT

Modern SoCs, especially in energy-sensitive and mixed-signal applications, rely heavily on on-chip voltage regulation to ensure stable, low-noise power delivery. On-chip regulators enhance system efficiency, reduce IR drop, and support dynamic power strategies like DVFS and power gating [6]. Common types include LDOs, linear regulators, switching regulators,

and switched-capacitor converters, each with trade-offs in efficiency, noise, and integration complexity [5].

A. TYPES OF VOLTAGE REGULATORS

- **Linear Regulators:** These regulators dissipate excess voltage to maintain output and are valued for simplicity and low output noise, though they suffer from low efficiency [15].
- **Low Dropout Regulators (LDOs):** LDOs enable regulation with minimal voltage headroom, making them ideal for battery-powered and analog systems. They combine an error amplifier, pass device, and reference source for precise output [3].
- **Switched-Capacitor (SC) Regulators:** SC regulators use capacitive charge transfer and suit applications needing full integration without inductors. However, they are limited by ripple and efficiency [2].
- **Digital LDOs (DLDOs):** DLDOs use digital control for fast response and ease of scaling in nanoscale nodes, proving ideal for fine-grained power domains [9].
- **Switching Regulators:** Efficient for high-power applications, switching regulators are harder to integrate due to inductors and EMI, though vital in systems like processors [8].

B. DESIGN CHALLENGES IN LOW QUIESCENT CURRENT LDOs

Designing LDOs with high PSRR, fast transient response, and low quiescent current is challenging in deep-submicron technologies like 90nm. Key issues include designing low-power error amplifiers [3], choosing between PMOS (simple, area-hungry) and NMOS (efficient, needs charge pump) pass devices [9], ensuring loop stability [8], minimizing dropout voltage, and reducing standby power through techniques like adaptive biasing and dynamic control.

C. ON-CHIP VOLTAGE REGULATORS IN SOCs

In complex SoCs, placing voltage regulators near the load improves regulation and efficiency. DLDOs enable multiple voltage domains, while LDOs serve sensitive analog/RF blocks like ADCs and PLLs [11]. They also assist in controlled startup and power gating by sequencing power rails and minimizing leakage during idle states [6].

III. METHODOLOGY

A. ARCHITECTURE OF LOW DROPOUT (LDO) REGULATOR

The architecture of a Low Dropout (LDO) regulator comprises four fundamental blocks: a pass transistor, an error amplifier,

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a voltage reference, and a feedback network. These elements operate in a closed-loop system to stabilize the output voltage, compensating for changes in input voltage or load current.

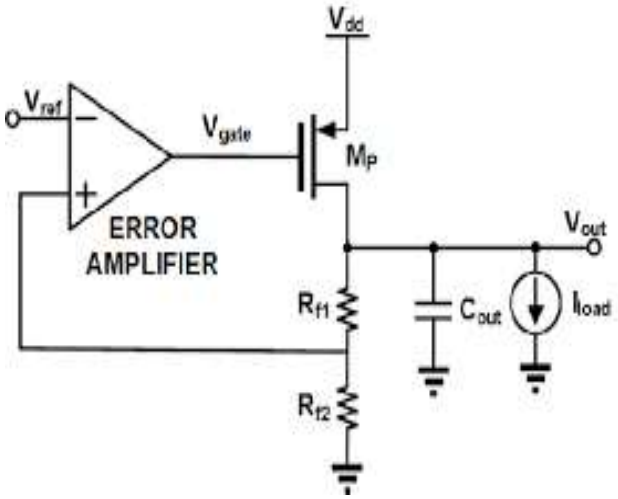

Figure 1 Architecture of LDO

Key Components of LDO

- **Pass Transistor:** This transistor functions as the primary control element, regulating current from the input to the output. PMOS devices are typically favored due to their lower dropout characteristics, as they can operate effectively even at small input-output voltage differences. NMOS transistors are also used but require a charge pump, increasing design complexity. The size and bias of this transistor influence the LDO's efficiency, dropout voltage, and transient response.
- **Error Amplifier:** Serving as a high-gain differential amplifier, it compares the feedback voltage to a reference and adjusts the pass transistor to maintain voltage regulation. The amplifier's characteristics directly affect loop stability, bandwidth, and power consumption.
- **Voltage Reference:** A stable reference, usually based on bandgap principles (~1.2V), provides a consistent voltage independent of temperature, supply, and process variations. It acts as the target output voltage, and its precision significantly impacts overall LDO accuracy.
- **Feedback Network:** Typically, a resistor divider, this network samples the output voltage and scales it down for comparison with the reference. The ratio of these resistors determines the regulated output voltage and influences loop stability and accuracy.
- **Additional Features:** Advanced LDO designs often incorporate protection features such as current limiting, soft-start circuits to manage inrush current, and compensation components to ensure system stability under dynamic load conditions.

IV. CIRCUIT DESIGN OF LDO

A. Construction of ERROR Amplifier

A two-stage operational amplifier (op-amp) is a critical control element in Low Dropout (LDO) regulator architectures, tailored to deliver high gain and adequate output drive for precise voltage regulation. This amplifier

typically comprises two cascaded stages implemented using MOS transistors.

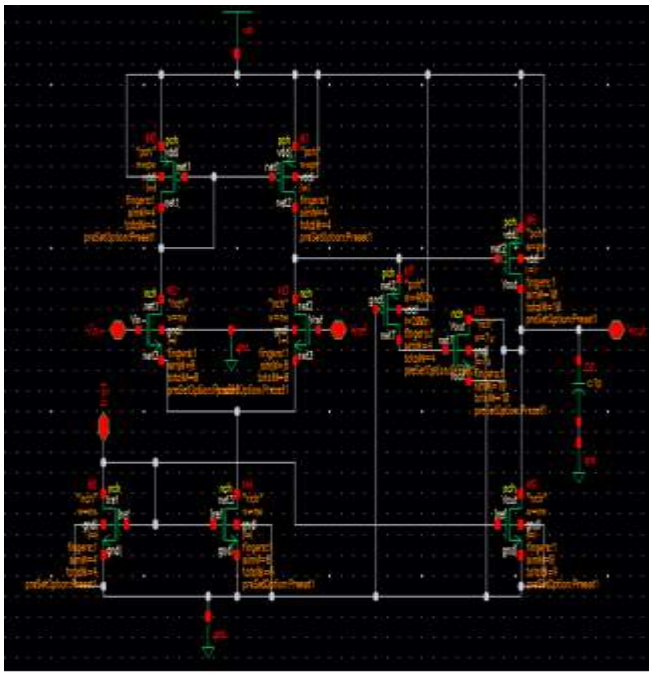

Fig 4.1 Schematic Design of Two-Stage Amplifier

- The first stage is a differential amplifier, typically formed by a matched pair of transistors. One input receives the feedback voltage from the LDO output, while the other connects to a fixed reference voltage. Active loads, like current mirrors, convert the differential current into a single-ended voltage, offering high gain and setting the amplifier's input characteristics.
- The second stage is usually a common-source amplifier, which further amplifies the signal to drive the gate of the pass transistor (typically PMOS). This pass transistor regulates the output voltage by adjusting its resistance based on the amplifier's output.
- A Miller compensation capacitor is added between the stages to introduce a dominant low-frequency pole, enhancing stability and phase margin. In some designs, a series resistor is added for improved transient response.
- Biasing circuits ensure stable operation across process and temperature variations, and output buffers may be included to enhance drive strength.

B. Working of ERROR Amplifier

The amplifier operates by comparing the feedback voltage from the LDO output with a stable reference voltage. Any deviation results in a differential current in the input pair, which gets amplified into a voltage signal in the first stage. The second stage boosts this signal further, modulating the gate voltage of the pass transistor to regulate output. If the output voltage drops, the amplifier increases the gate drive to reduce resistance and raise the output. If the voltage rises, the amplifier decreases gate drive to limit current. This negative feedback loop ensures tight voltage regulation.

The Miller capacitor ensures frequency stability by placing a dominant pole at low frequency, reducing phase shift and avoiding oscillation. Overall, the two-stage op-amp is the core control element, balancing gain, bandwidth, noise, and stability to maintain reliable low-noise voltage regulation in modern LDO applications.

C. Pass Transistor

The pass transistor regulates output voltage by adjusting current flow based on the error amplifier's control signal. PMOS transistors are commonly used for their low dropout and simpler drive requirements, while NMOS offers better performance but needs a charge pump. The transistor's size and type influence dropout voltage, efficiency, and response time. It serves as the core regulating element of the LDO**.**

D. Resistor Divider

The resistor divider provides feedback by scaling the output voltage for comparison with the reference. Its ratio sets the output voltage. Proper resistor selection ensures low power loss and good stability. A bypass capacitor is often added to improve response and phase margin.

E. Voltage Reference

The voltage reference—typically a bandgap circuit—supplies a stable voltage regardless of temperature or supply changes. It ensures precise regulation by serving as the comparator's target. Sub-bandgap references are used for low-voltage applications but may reduce accuracy.

F. Working of LDO Regulator

A Low Dropout Regulator (LDO) ensures a stable output voltage even when the input is only marginally higher than the output. The core architecture consists of four main blocks: a pass transistor, an error amplifier, a voltage reference, and a resistive feedback network.

When the LDO powers up, a temperature-independent reference voltage is generated. This is compared with a scaled version of the output voltage from the resistive divider. The error amplifier detects the voltage difference and drives the pass transistor to regulate current flow to the load. In PMOS-based LDOs, if the output drops due to load increase, the feedback voltage decreases. The amplifier increases its output, enhancing PMOS conductivity, allowing more current, and restoring output voltage. Conversely, a voltage rise reduces PMOS conductivity to lower the output. This closed-loop feedback enables tight regulation. The dropout voltage—the minimum input-output difference for regulation—depends on the pass transistor's on-resistance. Using CMOS (PMOS or NMOS) instead of BJT helps achieve low dropout, crucial in low-voltage systems. The error amplifier's gain and bandwidth determine how quickly and accurately the LDO responds to load or line transients. Proper compensation ensures both fast response and loop stability.

Designing LDO regulators requires careful trade-offs among key parameters. Achieving low dropout voltage demands large pass transistors, increasing area and parasitics. Minimizing quiescent current is vital for battery use but may reduce amplifier speed.

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Stability hinges on compensation and capacitor ESR, often requiring specific components. Fast transient response needs wide bandwidth and strong drive capability. High loop gain and precise feedback ensure good load and line regulation. Noise-sensitive applications need high PSRR and low output noise, demanding careful layout. However, enhanced performance often raises area and cost, especially in SoCs, requiring balanced design optimization.

G. MATHEMATICAL DESIGN OF LDO

The output voltage V_out is determined by

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

the resistive divider in the feedback loop. The relationship is given by:

Assume the desired V_{OUT} = 1.6 V and V_{ref} =

$$\frac{R_2}{R_1} = \frac{V_{out}}{V_{ref}} - 1$$

1.21 V. Rearrange to calculate the resistor ratio:

Step 1: Error Amplifier Gain

The PSRR depends on the error amplifier

$$PSRR_{dB} = 20\log_{10}\left(\frac{1}{A_{EA}}\right)$$

gain:

From the PSRR target of -35 dB:

Step 2: Output Capacitance

$$C_{out} = \frac{10 \times 10^{-3}}{1 \times 10^{-3} \cdot 2\pi \cdot 10^{6}} \approx 1.59\,\mu F$$

The output capacitor determines the transient response:

V. RESULTS:

Figure 1-2 represents the simulation results of key circuit blocks using Cadence Virtuoso. Designs were rigorously tested to meet performance specifications, with layouts and results verified through Calibre for design rule compliance and real-world reliability. This ensures functional accuracy and robust performance.

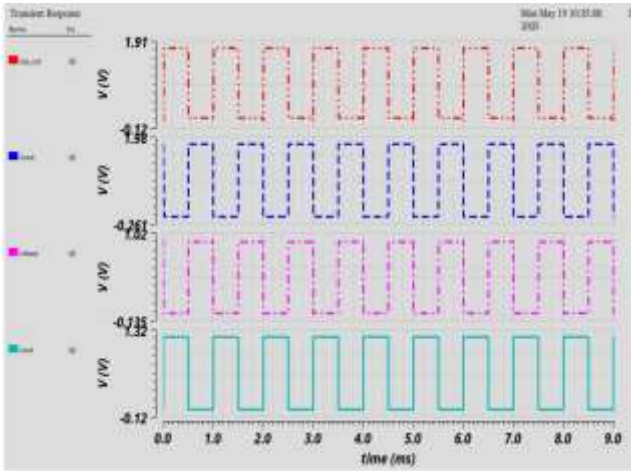

Figure 6.1 Transient Response

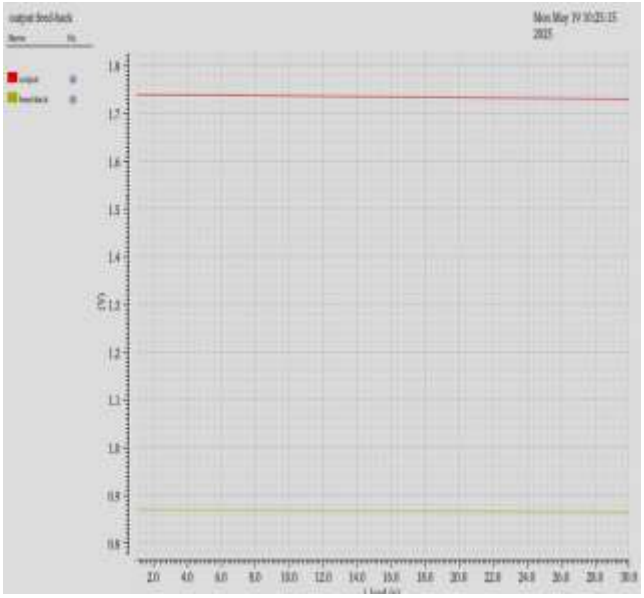

Figure 6.2 Output feedback

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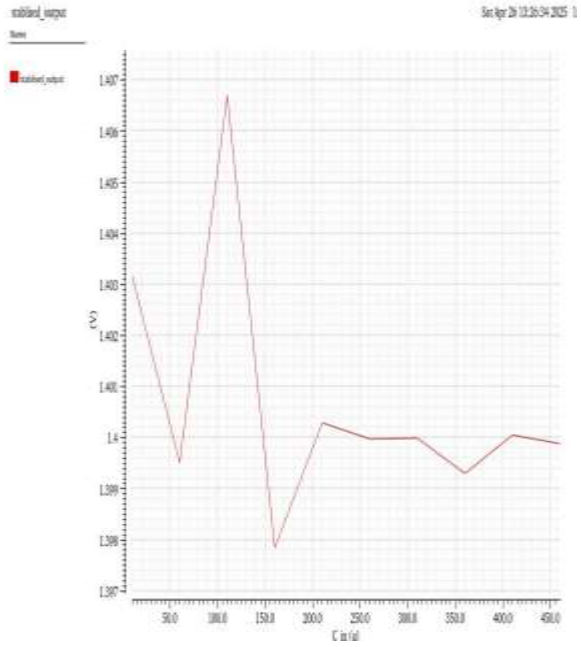

Figure 6.3 Stabilized output

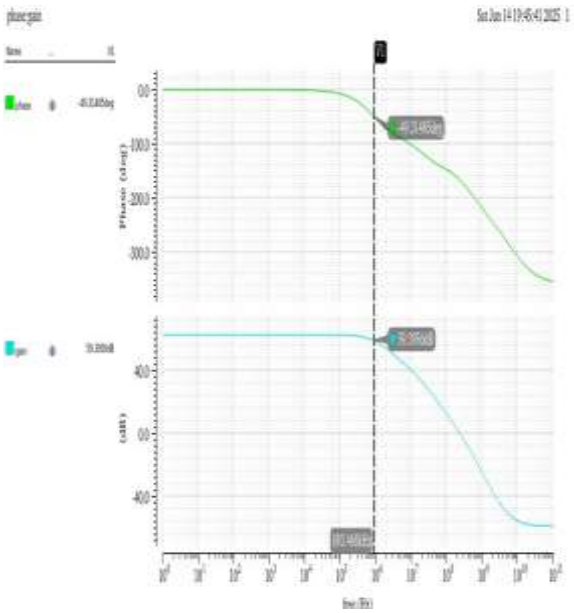

Figure 6.17 Phase gain of LDO

VI. CONCLUSION

The proposed LDO regulator, implemented in 90 nm CMOS, achieves a strong balance of noise performance, efficiency, stability, and low power consumption. It delivers a regulated 1.64 V output from 1.8 V–3.5 V input, with excellent line/load regulation, high-frequency PSRR, and low quiescent current—ideal for analog/RF blocks in SoCs and low-power IoT applications. Post-layout simulations confirm robust performance under PVT variations, validating its real-world reliability.

VII. FUTURE SCOPE

Future LDOs will focus on deeper SoC integration, ultra-low quiescent current, enhanced PSRR beyond 10 MHz, and adaptive digital control for reliability. Applications in IoT and biomedical devices will drive demand for energy harvesting compatibility, while sustainability and smart diagnostics will shape next-generation LDO designs.

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