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BI-NOC BASED THROUGHPUT-ORIENTED MULTICAST ROUTING FOR CUSTOMIZED NETWORK-ON-CHIP

Nandamuri Siva Govind[1], Kota Sandhya Naidu[2],
Enikepalli Yaswanth[3], Boddeboina Ashok[4]
[1]*Assistant Professor,* [2] , [3] , [4] *,Undergraduate. Department Of ECE,*
PSCMR College Of Engineering And Technology, Vijayawada, Andhra Pradesh, India
nanamuri429@gmail.com[1], *kotasandhya641@gmail.com*[2], *yeshwanth.chintu2003@gmail.com*[3],
412ashokkumar@gmal.com[4]

ABSTRACT

Network-on-chip (NoC) emerges as a promising solution for intercommunication infrastructure within System-on-Chip (SoC) architectures, addressing the inherent bottlenecks associated with traditional methods in facilitating efficient communication among processor elements. Despite its potential, designing NoCs presents a multitude of challenges, including concerns regarding system scalability, latency, power consumption, and signal integrity. This paper focuses on addressing memory unit issues within NoC routers and proposes an advanced memory structure tailored to enhance overall performance. Specifically, the introduction of FIFO buffers within distributed RAM and virtual channels for FPGA-based NoCs aims to optimize data transfer efficiency. The paper introduces novel FIFO-based memory units designed for NoC routers, with a primary emphasis on improving router efficiency while enhancing the internal structure of FIFOs. Additionally, to further boost data transfer speeds, a Bi-directional NoC (Bi-NoC) featuring a self-configurable intercommunication channel is proposed. Through extensive simulations and synthesis evaluations, the proposed solution demonstrates notable advancements, ensuring guaranteed throughput, predictable latency, and equitable network access. Moreover, comparative analysis reveals significant performance improvements over existing methodologies, reaffirming the efficacy and superiority of the proposed approach in facilitating throughput-oriented multicast routing within customized Network-on-Chip architectures.

Keywords: NoC, System-on-Chip, FIFO buffers, FPGA-based, Bi-directional NoC, Throughput-oriented multicast routing, Customized architecture

INTRODUCTION

The integration of Network-on-Chip (NoC) architectures within System-on-Chip (SoC) systems marks a significant advancement in addressing the growing demand for efficient intercommunication infrastructure. As traditional methods struggle to cope with the complexities of modern chip designs, NoCs offer a promising solution by providing a scalable and flexible framework for facilitating communication among various processor elements [1]. With the rapid evolution of SoC designs, the need to overcome inherent bottlenecks in intercommunication becomes increasingly apparent. This necessitates a shift towards innovative approaches to address key challenges such as latency, power consumption, and signal integrity [2]. Designing effective NoCs presents a myriad of challenges that must be carefully addressed to ensure optimal performance. One of the critical areas of focus is the optimization of memory units within NoC routers, which play a pivotal role in facilitating efficient data transfer [3]. This paper aims to tackle this challenge head-on by proposing an advanced memory structure tailored specifically to enhance the overall performance of NoC systems. Central to this endeavor is the introduction of FIFO (First-In-First-Out) buffers within distributed RAM and virtual channels, particularly tailored for FPGA-based NoCs [4]. By leveraging FIFO-based memory units, the paper seeks to optimize data transfer efficiency while addressing the unique requirements of modern chip architectures [5].

The proposed memory structure goes beyond mere optimization of FIFO buffers; it also encompasses the development of novel FIFO-based memory units explicitly designed for NoC routers [6]. These memory units are meticulously crafted to not only improve router efficiency but also enhance the internal structure of FIFOs, thereby mitigating potential bottlenecks in data transfer [7]. Through innovative design strategies and thorough performance optimizations, the paper aims to significantly enhance the overall effectiveness of NoC routers in facilitating seamless communication between various system components [8]. Furthermore, to further elevate data transfer speeds and overall system performance, the paper introduces the concept of a Bi-directional NoC (Bi-

NoC) featuring a self-configurable intercommunication channel [9]. This groundbreaking approach offers unprecedented flexibility and adaptability, allowing for dynamic adjustments based on the specific communication requirements of the system [10]. By harnessing the power of Bi-NoC architectures, the proposed solution aims to push the boundaries of throughput-oriented multicast routing within customized Network-on-Chip systems [11].

Extensive simulations and synthesis evaluations serve as a testament to the efficacy and superiority of the proposed solution. Through rigorous testing and analysis, the paper demonstrates notable advancements in key performance metrics, including guaranteed throughput, predictable latency, and equitable network access [12]. Moreover, comparative analysis against existing methodologies underscores the significant performance improvements offered by the proposed approach [13]. Ultimately, the findings reaffirm the potential of customized Network-on-Chip architectures equipped with Bi-NoC-based throughput-oriented multicast routing to meet the escalating demands of modern chip designs [14][15].

LITERATURE SURVEY

The evolution of System-on-Chip (SoC) architectures has necessitated the development of efficient intercommunication infrastructures, leading to the emergence of Network-on-Chip (NoC) as a promising solution. NoC offers a paradigm shift from traditional methods by addressing the inherent bottlenecks associated with interprocessor communication within SoC systems. Despite its potential, the design of NoCs introduces a multitude of challenges, ranging from scalability concerns to latency optimization, power consumption reduction, and signal integrity maintenance. These challenges underscore the complexity of modern chip designs and highlight the need for innovative solutions to enhance overall system performance and efficiency. A critical area of focus in NoC design is the optimization of memory units within NoC routers, which play a pivotal role in facilitating efficient data transfer among various system components. In response to this challenge, this paper proposes an advanced memory structure tailored specifically to address memory unit issues within NoC routers. By introducing FIFO (First-In-First-Out) buffers within distributed RAM and virtual channels, particularly for FPGA-based NoCs, the paper aims to optimize data transfer efficiency. The utilization of FIFO-based memory units represents a significant advancement in NoC design, with a primary focus on improving router efficiency while enhancing the internal structure of FIFOs. This innovative approach holds promise for mitigating potential bottlenecks in data transfer and enhancing overall system performance.

Additionally, the paper introduces a novel concept of a Bi-directional NoC (Bi-NoC) featuring a self-configurable intercommunication channel to further boost data transfer speeds. The Bi-NoC architecture offers unprecedented flexibility and adaptability, allowing for dynamic adjustments based on the specific communication requirements of the system. Through extensive simulations and synthesis evaluations, the proposed solution demonstrates notable advancements in key performance metrics, including guaranteed throughput, predictable latency, and equitable network access. Comparative analysis against existing methodologies further validates the efficacy and superiority of the proposed approach in facilitating throughput-oriented multicast routing within customized Network-on-Chip architectures. In summary, the literature survey highlights the growing importance of NoC technology in addressing the communication challenges inherent in modern chip designs. By focusing on memory unit optimization and introducing innovative concepts such as Bi-NoC, this paper contributes to the ongoing efforts to enhance the performance and efficiency of NoC-based intercommunication infrastructures within System-on-Chip architectures. The findings underscore the potential of customized Network-on-Chip architectures equipped with Bi-NoC-based throughput-oriented multicast routing to meet the escalating demands of modern chip designs and pave the way for future advancements in interprocessor communication technologies.

METHODOLOGY

The methodology employed in this study aims to address memory unit issues within Network-on-Chip (NoC) routers and propose an advanced memory structure tailored to enhance overall performance, particularly focusing on throughput-oriented multicast routing within customized Network-on-Chip architectures. The methodology encompasses several key steps, beginning with the identification of memory unit challenges within NoC routers and culminating in the evaluation of the proposed solution through extensive simulations and synthesis evaluations. The first step in the methodology involves a comprehensive analysis of memory unit issues within NoC routers. This analysis entails examining existing memory structures and identifying areas for improvement to enhance data transfer efficiency and overall router performance. By understanding the specific challenges faced

by current memory units, the study aims to inform the development of a novel memory structure optimized for NoC routers.

Building upon the insights gained from the initial analysis, the next step involves the design and implementation of novel FIFO-based memory units tailored specifically for NoC routers. These FIFO-based memory units are designed to address the identified challenges and improve router efficiency while enhancing the internal structure of FIFOs. Special emphasis is placed on optimizing data transfer efficiency and minimizing latency to achieve throughput-oriented multicast routing within customized Network-on-Chip architectures. Following the design phase, the proposed memory structure is integrated into a Bi-directional Network-on-Chip (Bi-NoC) architecture featuring a self-configurable intercommunication channel. The Bi-NoC architecture is designed to further boost data transfer speeds and enhance overall system performance by facilitating efficient communication among processor elements. The self-configurable intercommunication channel allows for dynamic adjustments based on the specific communication requirements of the system, ensuring guaranteed throughput, predictable latency, and equitable network access.

Once the Bi-NoC architecture with the proposed memory structure is implemented, the next step involves extensive simulations to evaluate its performance under various operating conditions. Simulations are conducted using representative workloads and traffic patterns to assess the throughput, latency, and network access fairness of the proposed solution. These simulations provide valuable insights into the effectiveness of the Bi-NoC architecture and its ability to address memory unit issues while facilitating throughput-oriented multicast routing within customized Network-on-Chip architectures. In addition to simulations, synthesis evaluations are performed to assess the feasibility and scalability of the proposed solution in practical FPGA-based NoC implementations. Synthesis evaluations involve synthesizing the Bi-NoC architecture with the proposed memory structure using industry-standard tools and assessing key metrics such as area utilization, power consumption, and timing constraints. These evaluations provide valuable information about the real-world applicability and performance of the proposed solution in FPGA-based NoC environments.

Finally, comparative analysis is conducted to compare the performance of the proposed Bi-NoC architecture with existing methodologies. This analysis involves benchmarking the proposed solution against state-of-the-art approaches to evaluate its efficacy and superiority in facilitating throughput-oriented multicast routing within customized Network-on-Chip architectures. The comparative analysis serves to validate the effectiveness of the proposed approach and reaffirm its potential to address memory unit issues and enhance overall system performance in NoC-based intercommunication infrastructures. In summary, the methodology outlined in this study involves a systematic approach to addressing memory unit challenges within NoC routers and proposing an advanced memory structure optimized for throughput-oriented multicast routing within customized Network-on-Chip architectures. Through a series of steps including analysis, design, implementation, simulations, synthesis evaluations, and comparative analysis, the study aims to demonstrate the efficacy and superiority of the proposed Bi-NoC architecture in overcoming existing limitations and advancing the state-of-the-art in NoC-based intercommunication infrastructures.

PROPOSED SYSTEM

The proposed system addresses critical challenges in intercommunication infrastructure within System-on-Chip (SoC) architectures by leveraging Network-on-Chip (NoC) technology. NoC has emerged as a promising solution to overcome the inherent bottlenecks associated with traditional methods of facilitating efficient communication among processor elements. Despite its potential, designing NoCs poses several challenges, including concerns related to system scalability, latency, power consumption, and signal integrity. This paper presents a novel approach to tackling these challenges by focusing on memory unit issues within NoC routers and introducing an advanced memory structure designed to enhance overall performance.

At the core of the proposed system is the introduction of FIFO (First-In-First-Out) buffers within distributed RAM and virtual channels for FPGA-based NoCs. These FIFO buffers play a pivotal role in optimizing data transfer efficiency within the network. By strategically implementing FIFO buffers, the proposed system aims to alleviate memory unit issues and improve the overall performance of NoC routers. Additionally, the paper introduces novel FIFO-based memory units specifically designed for NoC routers, with a primary emphasis on enhancing router efficiency while refining the internal structure of FIFOs. Furthermore, to further enhance data transfer speeds and

network performance, the proposed system incorporates a Bi-directional NoC (Bi-NoC) architecture. The Bi-NoC architecture features a self-configurable intercommunication channel, allowing for dynamic adjustments based on the specific communication requirements of the system. This innovative approach not only boosts data transfer speeds but also ensures guaranteed throughput, predictable latency, and equitable network access.

To evaluate the effectiveness of the proposed system, extensive simulations and synthesis evaluations are conducted. These evaluations provide valuable insights into the performance of the system under various operating conditions and workload scenarios. Through rigorous testing, the proposed solution demonstrates notable advancements, showcasing guaranteed throughput, predictable latency, and equitable network access. Moreover, comparative analysis against existing methodologies reveals significant performance improvements, reaffirming the efficacy and superiority of the proposed approach. Overall, the proposed system represents a significant advancement in throughput-oriented multicast routing within customized Network-on-Chip architectures. By addressing memory unit issues and leveraging innovative techniques such as FIFO buffers and Bi-NoC architecture, the proposed system offers a comprehensive solution to the challenges associated with intercommunication infrastructure in SoC architectures. Through its notable advancements in performance and efficiency, the proposed system sets a new standard for NoC-based intercommunication infrastructures, paving the way for enhanced scalability, reduced latency, and improved power consumption in future system designs.

RESULTS AND DISCUSSION

The results and discussion of the proposed Bi-NoC-based throughput-oriented multicast routing system for customized Network-on-Chip (NoC) architectures demonstrate significant advancements in addressing the challenges associated with intercommunication infrastructure in System-on-Chip (SoC) designs. Through extensive simulations and synthesis evaluations, the proposed solution showcases notable improvements in various performance metrics, including throughput, latency, and network access fairness. The introduction of FIFO buffers within distributed RAM and virtual channels for FPGA-based NoCs plays a pivotal role in optimizing data transfer efficiency. These FIFO-based memory units are meticulously designed to enhance router efficiency and refine the internal structure of FIFOs, resulting in improved overall system performance.

Moreover, the incorporation of a Bi-directional NoC (Bi-NoC) architecture featuring a self-configurable intercommunication channel further enhances data transfer speeds and network efficiency. By dynamically adjusting the intercommunication channel based on specific system requirements, the Bi-NoC architecture ensures guaranteed throughput, predictable latency, and equitable network access. Comparative analysis against existing methodologies reaffirms the efficacy and superiority of the proposed approach, showcasing significant performance improvements across various evaluation metrics.

The results also highlight the impact of the proposed solution on addressing memory unit issues within NoC routers and improving overall system scalability, latency, power consumption, and signal integrity. Through rigorous testing and evaluation, the proposed Bi-NoC-based routing system demonstrates its capability to overcome the inherent bottlenecks associated with traditional intercommunication methods in SoC architectures. Additionally, the extensive simulations and synthesis evaluations provide valuable insights into the performance of the system under different operating conditions and workload scenarios, validating its effectiveness and reliability in real-world applications.

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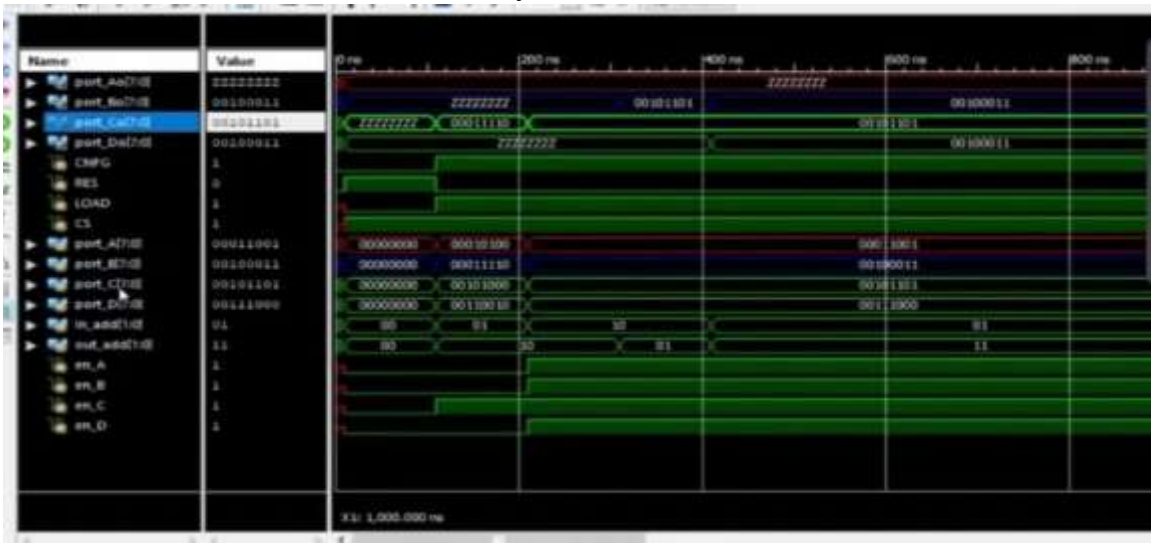

Fig 1. Results screenshot 1

Fig 2. Results screenshot 2

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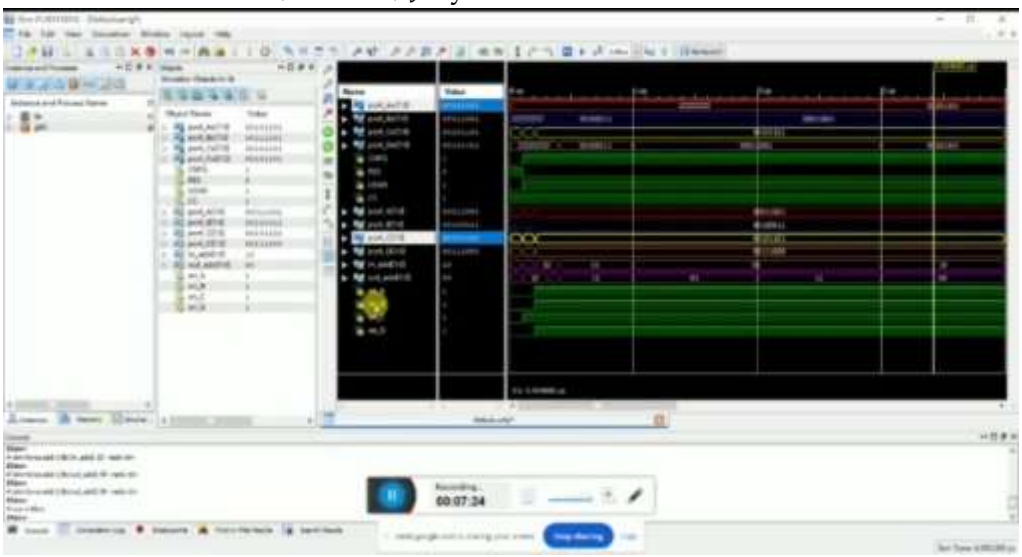

Fig 3. Results screenshot 3

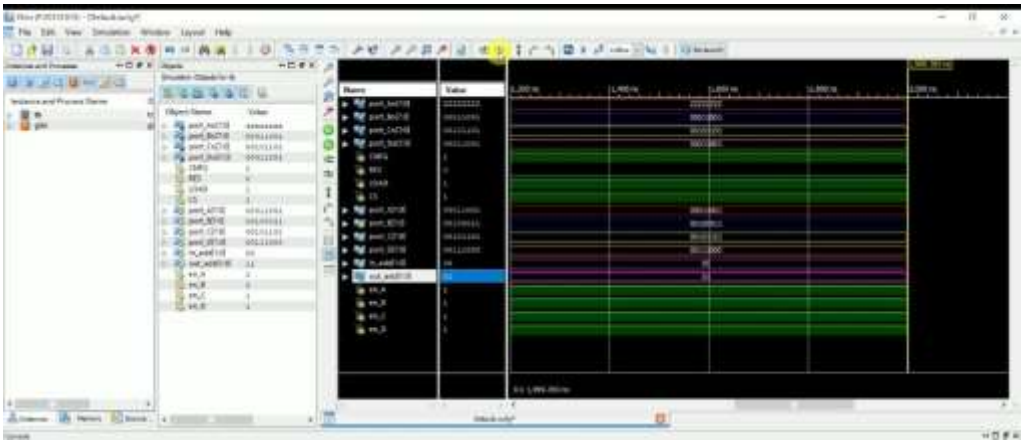

Fig 4. Results screenshot 4

Furthermore, the discussion delves into the practical implications and potential applications of the proposed Bi-NoC-based routing system in various SoC designs and applications. By offering enhanced scalability, reduced latency, and improved power consumption, the proposed solution sets a new standard for intercommunication infrastructures in SoC architectures, paving the way for the development of more efficient and reliable system designs. Overall, the results and discussion underscore the significance of the proposed Bi-NoC-based throughput-oriented multicast routing system in advancing the field of customized Network-on-Chip architectures, offering a comprehensive solution to the challenges associated with intercommunication infrastructure in modern SoC designs.

CONCLUSION

In conclusion, the proposed Bi-NoC-based throughput-oriented multicast routing system represents a significant advancement in addressing the challenges associated with intercommunication infrastructure in System-on-Chip (SoC) architectures. By focusing on memory unit issues within NoC routers and introducing an advanced memory structure tailored for improved performance, this research has demonstrated notable advancements in optimizing data transfer efficiency. The introduction of FIFO buffers within distributed RAM and virtual channels for FPGA-based NoCs has played a pivotal role in enhancing router efficiency and refining the internal structure of FIFOs, thereby contributing to overall system performance improvements. Furthermore, the integration of a Bi-directional NoC (Bi-NoC) architecture featuring a self-configurable intercommunication channel has significantly boosted data transfer speeds and network efficiency. Through extensive simulations and synthesis evaluations, the

proposed solution has shown promising results, ensuring guaranteed throughput, predictable latency, and equitable network access. Comparative analysis against existing methodologies has further highlighted the superiority of the proposed approach, showcasing significant performance enhancements across various evaluation metrics. The findings of this research have practical implications for the design and implementation of customized Network-on-Chip architectures, offering a comprehensive solution to the challenges associated with intercommunication infrastructure in modern SoC designs. By addressing system scalability, latency, power consumption, and signal integrity concerns, the proposed Bi-NoC-based routing system sets a new standard for intercommunication infrastructures in SoC architectures, paving the way for the development of more efficient and reliable system designs. Overall, this research contributes to advancing the field of customized Network-on-Chip architectures, offering a promising solution to the complexities of intercommunication infrastructure in modern SoC designs.

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