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The Design of Low-Power And High-Speed Full Adder Through The Exploration of Novel XOR And XNOR Gates

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Abstract

In this project, we propose six different hybrid full adder circuits that make use of the XNOR, XOR gates that have lately come into existence. These circuits are tuned with respect to power use and processing speed in contrast to more standard designs. This is a viable choice due to its low output capacitance. There was no clear winner among the three proposed full adder circuits, which all fared well in terms of speed, power consumption, and motor control. In this work, we propose a novel family of circuits that can execute XOR, XNOR, and XOR/XNOR in parallel. The suggested circuits are well optimised in terms of power consumption and delay thanks to their low output capacitance and low short circuit power dissipation. We introduce six novel hybrid 1-bit full-adder (FA) circuits and a Ripple Carry Adder based on the special full-swing XOR-XNOR or XOR/XNOR gates. Each of the proposed circuits has benefits and drawbacks that must be considered. A new strategy for transistor sizing is presented to optimise the PDP of the circuits. The proposed method uses a particle swarm optimisation methodology for numerical computing to determine the best PDP. The effects of changing the transistor size, supply voltage, output capacitance, input noise immunity, and threshold voltage on the proposed circuits are investigated.

Key words: ***XOR-XNOR, full-adder, Ripple Carry Adder***

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1. Introduction

The present work presents six unique hybrid full adder circuits, each of which makes use of the newly invented XNOR, XOR gates. All of the hybrid full adder circuits are presented here. When compared to designs that are more traditional, these circuits are optimised in terms of both the amount of power they use and the speed at which they process information. This choice is a good one to choose with since it has a relatively low output capacitance. Due to the fact that each of the three recommended full adder circuits performed comparably well in terms of speed, power consumption, and motor control, it was not possible to identify a single obvious winner. Tanner is the name of the simulation tool that is utilised for the simulations of the 45-nm technology. The performance of the proposed circuits is superior than that of the reference circuit. It is possible to test the performance of the suggested full adder circuits by making adjustments to the voltage at the input and the load at the output.

All three of these novel families of circuits, XOR, XNOR, and XOR/XNOR, are offered here as potential candidates for parallel implementation. The suggested circuits have a low short circuit power dissipation and a low output capacitance, which makes them highly optimised in terms of power consumption and delay thanks to these characteristics. It is shown that there exist six novel hybrid 1-bit full-adder (FA) circuits that are based on the peculiar full-swing XOR-XNOR or XOR/XNOR gates, in addition to a Ripple Carry Adder.

2. Existing Method

In mathematics, an adder may be either a "half adder" or a "full adder." The term "adder" may be used to refer to either species. A "half adder" with just two inputs and two outputs is completely useless in practise. In order to carry out operations like fast Fourier transforms (FFTs) and infrared integral and differential filters (IIRs), the ALU makes use of a complete adder, which is an adder with three inputs and two outputs. Three inputs and two outputs define a complete adder. The power consumption, output latency, and board area of the conventional full adders employed in ALU are all much higher. However, modern consumers are increasingly expressing

an interest in devices that are user-friendly, compact, lightweight, durable, and versatile. Hybrid technologies have developed in response to the aforementioned causes. As the use of mobile communications and personal computers continues to surge, the creation of low power hybrid VLSI systems has emerged as a crucial performance goal. That's because developments in each of those areas are accelerating at a rapid pace. Hybrid systems combine several kinds of reasoning into one cohesive whole. For the most part, a hybrid one-bit full adder is made up of a combination of complementary metal oxide semiconductor (CMOS) logic, transmission gate logic, and pass transistor logic.

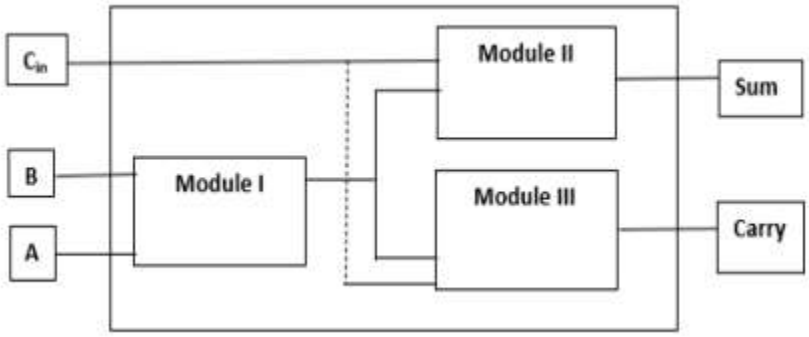

Figure 1: Block diagram of hybrid logic FA circuit

For the purpose of carrying out logical processes, XOR/XNOR circuits as well as simultaneous XOR-XNOR circuits.The suggested XOR-XNOR circuit exhibits high performance in terms of power consumption, latency, low output capacitance, driving capacity, and resilience. This is the case even if the crucial route does not have a NOT gate. The circuit is comprised of twelve transistors. The XOR-XNOR circuit that has been suggested is between 16.2% and 85.8% more efficient in PDP while also being quicker by 9% to 83.2%. Full adders are available in a variety of formats, including conventional CMOS full adders, New14T full adders, CFA full adders, TFA full adders, TGA full adders, and New-HPSC full adders. The passage of time is determined by the dynamic interaction of the vehicle's speed, its driving abilities, and its input capacitance while using this cutting-edge approach. [6] is an example of an all-encompassing adder that use CMOS logic in conjunction with transmission gates and Pass transistors. The adder in its entirety is simulated using Cadence's tool, which is tailored for technology

operating at 45 nm. The performance of the recommended full adder is evaluated in comparison to that of 20 other full adders currently on the market, the supply voltages of which vary from 0.4V to 1.2V. Ongoing research is being done in order to build a high-performance adder that is completely functioning. In this investigation, our primary emphasis is on developing a complete adder that has lower latency and uses less transistors. Additionally, we examine and evaluate two additional designs that also make use of fewer transistors. The anticipated characteristics and benefits of using this low-power logic architecture are outlined in the following paragraphs. It is feasible to activate some line multiplexers using an external signal in specific cases. The select line of the multiplexers is instead controlled by the Carry input signal, which has a complete voltage swing but no propagation delay. This was done so that the total propagation latency of the adder could be reduced.

XNOR and XOR gates are often used in the construction of full adders. When it comes to the amount of power that it requires, an XOR or XNOR circuit in a complete adder wins the prize. Therefore, a reduction in the amount of power consumed by the XOR or XNOR circuit will result in a reduction in the amount of power needed by the adder as a whole. The XOR and XNOR gates are both used in a variety of different circuits, such as comparators and parity checks, amongst other applications. In recent years, there has been a meteoric rise in the demand for portable electronic devices. These gadgets need to have a high speed and a low energy consumption. Improving the performance of the system calls for paying attention to design aspects such as the amount of power it consumes. [2] A great number of arithmetic-operating circuits need the whole adder as a fundamental component. Because of this, the effectiveness of the complete adder (also known as "3") is essential to the operation of the whole system. As a result, it is conceivable that an increase in the full adder's efficiency might be beneficial to the overall performance of the system. Using a variety of logic approaches, several types of complete adder circuits have been built, each of which comes with its own individual set of advantages and disadvantages [4-6]. There are now two primary categories that may be used to classify each and every design. These might be considered static or dynamic, depending on the context. There are a number of advantages to using static full adders,

including how simple they are to use, how little power they need, and how reliable they are. When compared to its static counterparts, dynamic full adders take up a much less amount of space on the chip. It has been shown that some types of performance are better suited to particular ways of thinking, while other types of performance are more suited to other ways of thinking. CMOS [5, 6], DPL [7], TGA [8, 9], and TFA [10, 11] are some of the standard techniques to the design of logic circuits. Adders of the hybrid-logic type are considered to be complete adders since they incorporate a range of logic approaches. In an attempt to improve the performance of complete adders, these designs use aspects drawn from a wide range of logic systems.

The output carry signal is produced by the recommended circuit (see Fig.), which does so with the assistance of the transistors NMOS 5, PMOS 5, and NMOS 6, PMOS 6.

3. Proposed System

For the diverse uses shown in Fig. 2, we suggested six novel FA circuits. Furthermore, the suggested FA cell's circuit structure is shown in Fig. 2. (a). All of these novel FAs make use of a hybrid logic approach, with the suggested XOR/XNOR or XOR-XNOR circuit used in their construction. The suggested hybrid FA cells are realised using the standard four-transistor 2-1-MUX architecture [Fig. 2(a)]. This 2-1-MUX is built using a TG logic approach, which eliminates power loss due to static and short circuit conditions. Two 2-to-1 MUX gates and the XOR- XNOR gate are shown in Fig. 2(a) to form the circuit of the first suggested hybrid FA (HFA20T) (e). HFA-20T is a 20-transistor circuit with low power consumption NOT gates on the critical route. Full-swing output, low power dissipation, extremely high speed, resistance to supply voltage scaling, and the ability to use smaller transistors are only a few of the benefits of this design.

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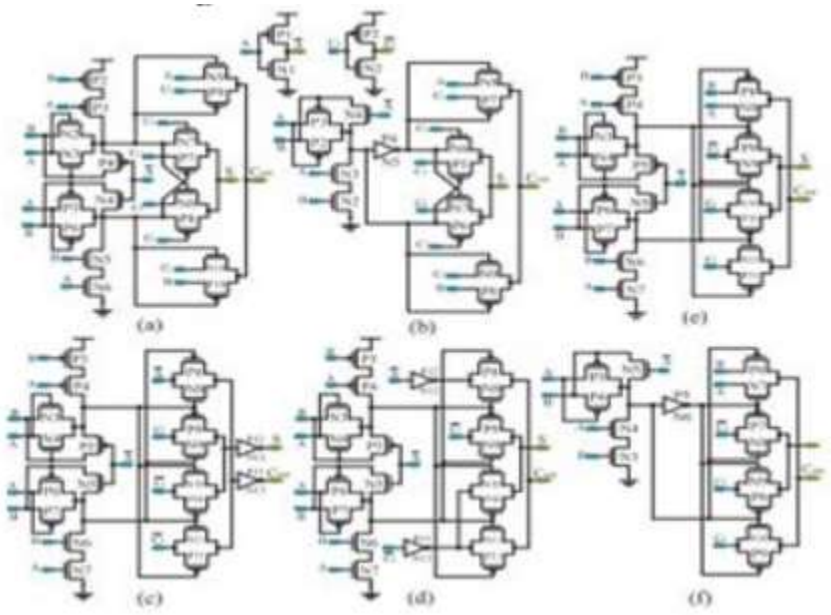

Figure 2: Proposed six new hybrid FA circuits. (a) HFA -20T. (b) HFA -17T. (c) HFA -26T. (d) HFA -26T. (e) HFA -22T. (e) HFA -19T.

When both inputs A and B are set to 1, the output Cout signal is identical to the input signal. However, the capacitance of the inputs may be modified to be almost equal by connecting signals A and B to transistors N9 and P10 [respectively] [in Fig. 2(a)]. The only real issue with using the HFA-20T in chain structure applications, such as a ripple carry adder, is that its output driving capabilities are reduced. This issue will arise in any circuit that employs transmission functions but does not use output buffering. The proposed HFA-20T, whose circuit layout is shown in Figure 2, was developed with low power consumption in mind.

A lot of the modern computing and encryption infrastructure relies on the XOR-XNOR logic combo. Figure 2 shows that a total of six transistors are used in the proposed XOR-XNOR circuit. The circuit consists of six transistors, three PMOS and three NMOS. To get the desired XNOR result, not one but two inverter circuits are used here: the first inverts A's input, while the second inverts the result of the XOR operation. All of this circuit's outputs are now being used to their full potential all at once.

As can be seen in Figure 2, there are a total of six alternative FA circuits that we suggest employing. These novel FAs, all of which were generated by the suggested XOR/XNOR circuit,

may be thought of as having a hybrid character. As shown in Figure 2(a), the HFA20T is the first approved hybrid FA. As can be seen in Figure 2(e), this circuit consists of two 2-to-1 MUX gates and one XOR- XNOR gate. Using low-power NOT gates on the route that is deemed to be the most critical, the HFA-20T circuit is made up of twenty transistors. Full-swing output, low power consumption and extremely high speed, robustness against scaling of the supply voltage, and scalability of the transistors are only a few of the benefits of this design. In chain structure applications like ripple carry adders, the HFA-20sole T's output driving capability is limited. This issue will arise in any circuit that employs transmission functions but does not use output buffering. To lessen the power consumption of the FA structures, it is possible to create the other XOR/XNOR signal by combining the functionalities of an XOR/XNOR gate and a NOT gate. Figure 5's subfigure reveals that the XOR gate is included into the architecture of the proposed hybrid FA cell (HFA-17T) (b). This design uses just 17 transistors instead of the HFA-20T's 20, which is a reduction of 3 transistors. HFA-17T has a greater delay time than HFA-20T because NOT gates were added to the critical route (to create the XNOR signal from the XOR signal). Since an HFA-17T chip has fewer transistors, its power consumption should be less than that of an HFA-20T chip. In a short circuit, however, the NOT gate may enhance the power transferred to the load because of its location on the critical path. As a result, the 17T is still losing a significant amount of power through its dissipation. Because of the NOT gate, the circuit's driving power at the output will also rise somewhat.

When the output capacitance of each stage is large, as is the case in many real-world situations, it is imperative that the circuit's output be buffered. Parasitic capacitors and resistors created during fabrication, as well as gradual increases in the threshold voltage of transistors, really limit the driving capabilities of VLSI circuits. However, it's possible that an output buffer may help in this case. The Sum and Cout outputs of the third suggested hybrid FA, HFA-B-26T, are buffered (see to Fig. 2(c) for more explanation). The HFA-B26T's critical path has one XOR-XNOR gate, one 2- 1-MUX gate, and one NOT gate. To prevent inputs from driving the nodes at the end of a circuit and to lower the resistance at the node's connection to power (VDD and GND), NOT gates are often positioned at the circuit's output. When compared to the HFA-20T and HFA-17T FAs, the HFAB-26T is less effective and has more latency. When the output capacitance of each stage is large, as is the case in many real-world situations, it is imperative that the circuit's output

be buffered. In reality, parasitic capacitors and resistors, as well as an increase in the threshold voltage of transistors over time, reduce the driving capability of VLSI circuits during fabrication; nevertheless, the output buffer helps to rectify this issue. The buffers are employed at the Sum and Cout outputs of the HFA-B-26T, the third proposed hybrid FA, as shown in Figure 2(c). The mandatory path of the HFA-B26T has one XOR-XNOR gate, one 2- 1-MUX gate, and NOT gates. In addition to lowering the resistance between the node at the end of the circuit and the power sources (VDD and GND), placing a NOT gate there prevents the inputs from driving the node. In other words, NOT gates do double duty. When compared to its forerunners, the HFA-20T and HFA-17T FAs, the HFAB-26T FA has a longer delay and higher power consumption. Another suggested hybrid FA with updated buffers is shown in Fig. 2(d), designated as HFA-NB-26T. The data inputs of the 2- 1-MUX gates are shown connected to the buffers. If the A and C signals are generated by the buffer, then the Sum and Cout outputs will be independent of the inputs to the are circuit. Since the A signal is already there, this procedure requires just three extra NOT gates to convert it into the buffered A signal. Because a single NOT gate may transform an A signal into a buffered A signal, this is possible. This necessitates the use of 26 transistors in the construction of the HFA-NB-26T FA circuit. Before XOR and XNOR signals may be generated, the data input nodes of 2-1-MUXs must settle on their ultimate value (GND or VDD). Since just an XOR-XNOR gate and a 2-1-MUX gate are used in the HFA-NB-26T's critical path, its latency is smaller than that of the HFA-B-26T. Due to the presence of a 2-1-MUX gate between the buffer and the output node, however, its driving capacity is reduced. This gate raises the output node's resistance to the supply voltage (VDD) and ground (GND). The circuitry of both the HFA-20T and HFA-17T has been simplified to use just the essential number of transistors. The Sum output is created using just the XOR, XNOR, and C signals, with no extra NOT gates required. If the Sum output is likewise generated using the C signal, then only the XOR and XNOR signals, and not the Sum output, will be linked to the data select lines of the 2-1-MUX. This is because the Sum output may be generated with only the XOR, XNOR, and C signals, without the need for any extra NOT gates. As a result, the circuit's delay is enhanced by a reduction in the capacitance at the XOR and XNOR nodes. HFA-22T and HFA-19T circuits were generated by using the concept mentioned previously in HFA-20T and HFA-17T, as shown in Fig. 1(e) and (f), respectively. Each of these circuits has been given a name. Compared to their

forerunners, the HFA-20T and HFA-17T, the HFA-22T and HFA-19T FA circuits are expected to have lower power consumption and shorter delay periods. This is due to the lower capacitance shared by the XOR and XNOR nodes. When compared to the HFA-20T and HFA-17T, the HFA-22T and HFA-19T will have enhanced driving capabilities thanks to the addition of the C signal.

The logic architecture of every given digital system must have at least one binary adder. In addition to their principal role as ALUs, binary adders have also been put to use as multipliers, dividers, and memory addressers. As a consequence, binary addition is crucial, and any advancement in this area has the potential to boost the processing speed of any computer system, leading to better overall performance. One of the most crucial and fundamental parts of every digital system is the binary adder. In addition to their employment in ALUs, binary adders find use in other units such as multipliers, divisions, and memory addressing. This is due to the adaptability of binary adders. As a consequence, binary addition is crucial, and any advancement in this area has the potential to boost the processing speed of any computer system, leading to better overall performance. When doing binary addition, the carry chain is the most significant challenge. In general, the wider the input operand, the longer the carry chain will be.

Figure 3. illustrates the carry chain's usefulness in the context of an 8-bit binary add operation. The worst-case scenario is shown below, when the carry travels from the least significant bit (LSB) to the most significant bit (MSB) through the route that can physically go the largest distance. The performance of carry-propagate adders may be improved by increasing the speed of the carry chain in these adders, but eliminating carry chains completely is not a practical option. To boost the effectiveness of computer architecture, many digital designers work to create faster adders. This is because adders are often the starting point of many calculations' crucial paths. Most data routing units in microprocessors and digital signal processors (DSPs) are built around a binary adder as their central processing unit (CPU). This is motivating intensive research into ways to reduce the adder's power delay.

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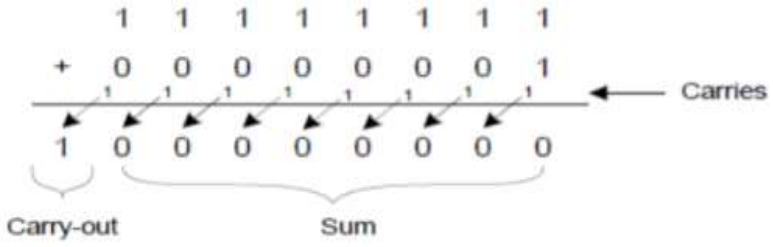

Figure3: Binary Adder Example.

It is well known that parallel-prefix adders may provide the maximum potential performance if constructed utilising VLSI technology. More and more companies are opting for reconfigurable logic solutions like Field Programmable Gate Arrays (FPGAs) over customary ASIC and DSP architectures. Faster processing speeds and reduced battery consumption are only two of the numerous reasons for this trend in mobile DSP and telecommunications applications. That's one of the numerous explanations for this pattern. With the increasing prevalence of mobile and portable devices, a competitive advantage in terms of power usage is becoming more important. However, unlike their VLSI counterparts, the performance of parallel-prefix adders on FPGAs will vary from that of their VLSI counterparts due to the FPGA's changeable logic and routing resources. This is due to the greater availability of resources on FPGAs. For instance, the carry route of the fundamental Ripple Carry Adder (RCA) might be enhanced by making advantage of the fast-carry chain used by the great majority of modern FPGAs. Several of the most obvious difficulties encountered while attempting to develop and implement tree-based adders on FPGAs are covered in this article. This research compares and contrasts many tree-based adder designs that have been implemented on a field-programmable gate array (FPGA) with the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA). The research finishes with some suggestions for improving FPGA design in order to achieve higher performance, after first examining the current state of tree-based adders.

This dissertation helped move the state of the art in parallel-prefix adders forward by introducing new approaches to algorithm and hardware design. It's possible that this will have an effect on both specialist and general computer architectures. Therefore, the results of this research may influence how engineers and scientists from a number of disciplines design and develop future

computer systems. While designing and implementing tree-based adders on FPGAs, this research looks at some of the more concrete issues that may arise. There are several ways to classify these problems. Various tree-based adder designs have been created and published for use with an FPGA; we evaluate the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA) alongside these other designs. There are several adder designs among them. In its last section, the study draws some broad conclusions and makes some suggestions for enhancing FPGA design for optimal performance in tree-based adders.

Accumulators of Multiplicative Carry In order to add two binary integers, all that has to be done is for the carry-out of the first bit to be connected to the carry-in of the second bit. A "ripple-carry adder" is an arithmetic circuit in which the carry-in bit is input and the carry-out bit is output after the sum has been calculated. Each adder in this kind of adder contributes one bit to the final tally, and the adders are chained together to form the final product. In Figure 2.3, we see a 4-bit ripple-carry adder in action. A single-bit adder, represented by a trapezium, is capable of operating independently. At the very top of the illustration, an adder connects the cin and the cout, showing the carry making its way from the cin to the cout. The solid line in Figure 3.1 connects the least significant bit (LSB) of the input (a0 or b0) to the most significant bit (MSB) of sum. The diagram clearly illustrates this relationship. (sn-1). The ripple carry adder is constructed by wiring together several groups of full adders (FA). The ripple carry procedure involves a single full adder adding the two carried binary digits together. The start of the carry-in for the next stage is intrinsically linked to the conclusion of the previous stage.

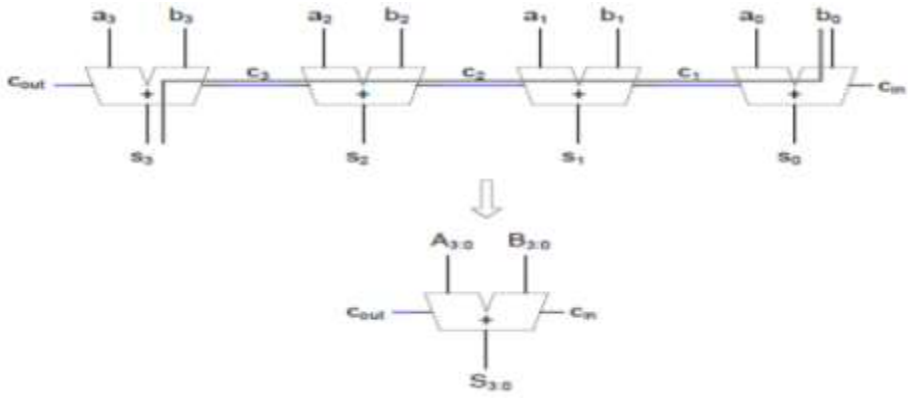

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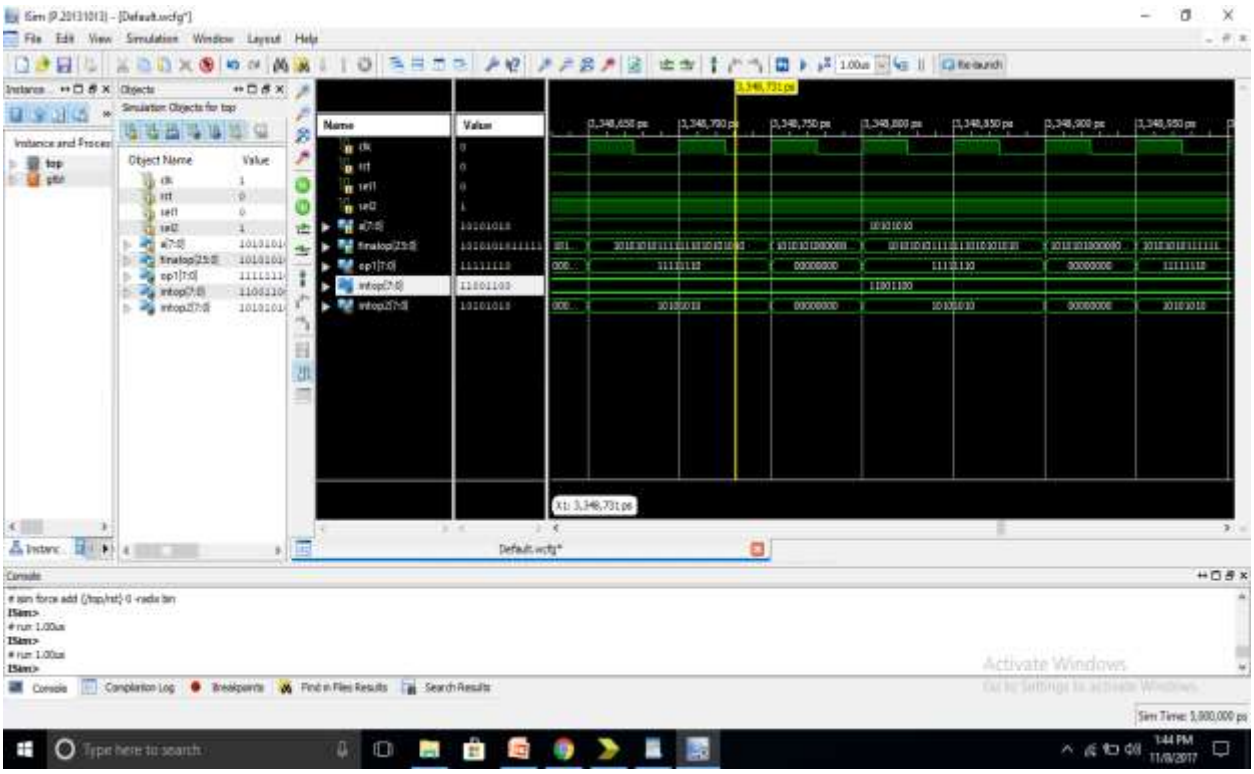
Figure 4:.Ripple-Carry Adder.

The AND, OR, and XOR gates are all assumed to have a delay of 2/, whereas the NOT gate is assumed to have a delay of 1/. Each gate totals one unit in area. Using this technique and assuming that each add block is created using a 9-gate full adder, the critical path is estimated as follows. The formula for this is: ai + bi + si = 10/ 9/ = ai + bi * ci + 1 ci □ si = 5/\ ci □ ci+1 = 4/\ The worst possible delay, or critical route, is given by trca = 9 + (n - 2) x 4 + 5 = f4n + 6. The area required for an n-bit RCA is simply 9n, since each bit requires 9 gates.

4. Results & Simulation Outputs



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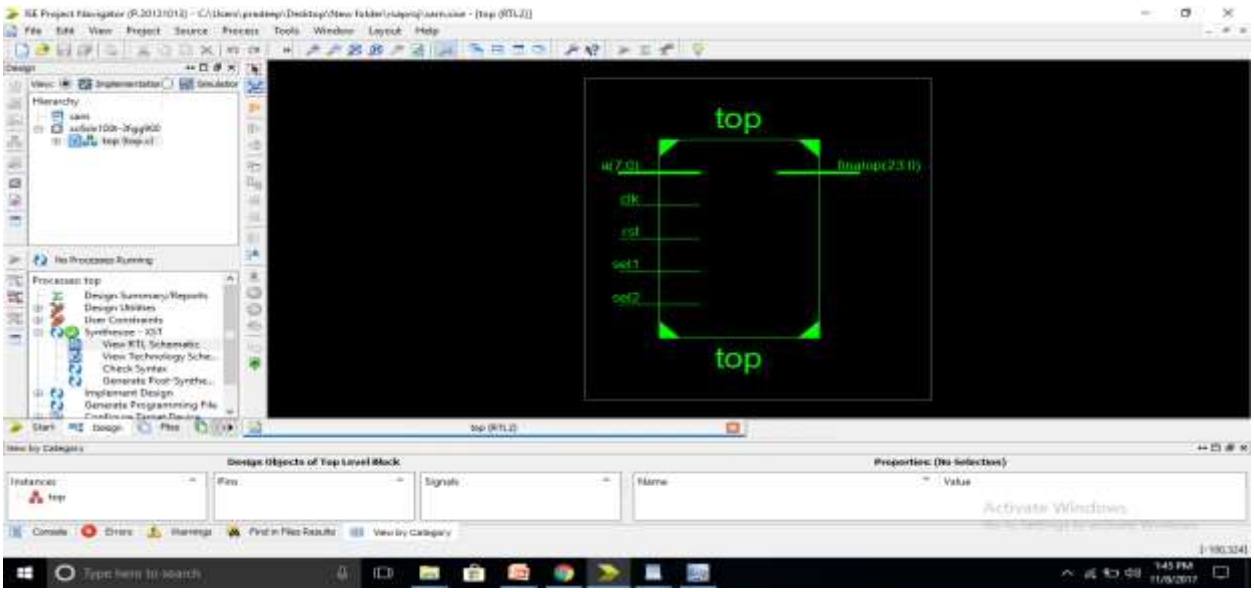

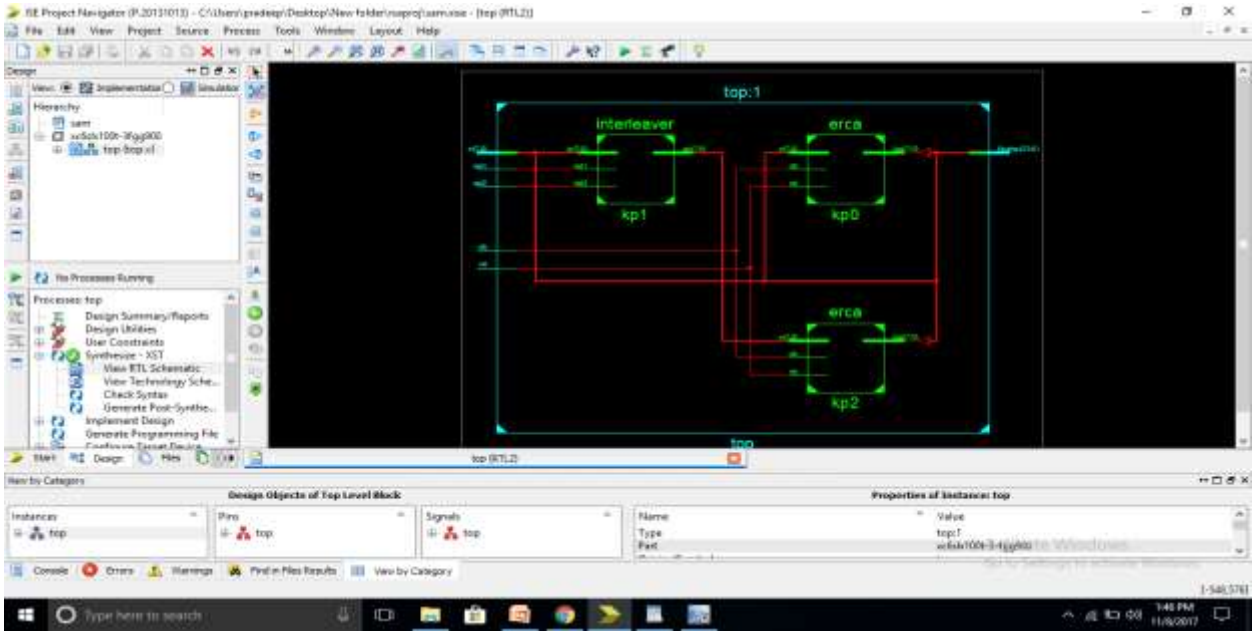

Conclusion

In order to achieve both of these objectives, a unique XOR-XNOR circuit consisting of six transistors is proposed. This circuit is a component of a full adder for 16 digits, which also

consists of a sum and carry circuit, as well as this one. We do this by simulating the recommended XOR-XNOR circuit and entire adder in Microwind, employing both 180 nm and 90 nm CMOS technology, so that we can evaluate how well they function. The power and PDP performance of the recommended circuits is reasonable when the voltage levels are between 0.7 V and 1 V. The entire adder circuit that is recommended makes excellent use of 90 nm technology and is a suitable fit for higher order spiralled adder circuits as well as onto this at lower supply voltages. If it is tested in other software, this circuit may have applications in digital signal processing, microprocessors, and maybe even other fields.

We started out by putting the XOR-XNOR and XOR-XNOR circuits through their paces. The findings of the study indicated that it was not a wise decision to put NOT gates anywhere along the crucial route of the circuit. The optimal voltage source compensation of an XOR-XNOR gate needs adequate comments on the gate's outputs, which is another disadvantage of this kind of logic gate. Because the delay in the circuit and the output capacitance are both expanding as a result of the feedback, the power consumption of the circuit is also growing. After that, we discussed further XOR/XNOR and XOR-XNOR gates that resolve these problems.

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