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OPTIMAL DESIGN AND PERFORMANCE ANALYSIS OF SYMMETRIC HYBRIDISED CASCADED MLI AND ASYMMETRIC SWITCHED CAPACITOR UNIT MLI FOR DYNAMIC LOADS

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Abstract
In this work, two different symmetric and asymmetric multilevel inverter topologies are proposed. In Symmetric configuration, a new cascaded multilevel inverter is proposed. The modified H-Bridge inverter in symmetric configuration produces an increase in output voltage to five levels from three levels by using a bidirectional switch at the midpoint of dual input dc source. The asymmetric configuration is developed with switched capacitor unit, which boosts the output voltage and produces twice the voltage levels at loads.
The proposed topologies are simulated using MATLAB-SIMULINK. The proposed topologies are tested for different resistive and inductive load disturbance conditions with different input voltages and modulation techniques. Also, analysis and comparison of the total harmonic distortion (THD), output voltage is done for both symmetric and asymmetric configurations from the results obtained for various test conditions. The proposed multilevel inverter topologies are also suitable for renewable energy fed applications.

I. Introduction

In recent years, there is an increase in demand for high power equipment at megawatt level. A 2 level inverter produces an output voltage or current in two different levels. This conventional inverter has high switching frequency, high switching losses. There is also harmonic distortion and stress on the switches. Major problem is Total Harmonic Distortion. With these problems, it is difficult to connect the power semiconductor switches directly to medium and high voltage grids. This increased the need for multi level inverter topologies.
Researchers considered multilevel inverters as a new power conversion approach. The Multilevel inverters have been developed and utilized for higher level voltages. In achieving higher voltage levels and power levels, Cascaded multilevel inverters are more flexible than conventional topologies. Cascaded multilevel inverters are constructed by linking in series output terminals of several H-Bridge Inverters. With advancements in multilevel inverters, the need for the new modulation methods for the same is also increasing. PWM switching is suitable for Hybrid cascaded multilevel inverter as it facilitates charging and discharging time for storage elements.
The Cascaded multilevel inverter can be operated in both symmetric and asymmetric configuration. In the Symmetric configuration, the magnitude of DC input sources is equal due to which number of output levels is less. In contrast, for Asymmetric configuration DC input sources are unequal due to which different voltage levels can be generated.
Cascaded multi level inverters are more flexible in achieving higher voltage levels and power levels than conventional inverter topologies [1]. The modularity property of inverter is used to increase the output power of the inverter. The advancements in MLI's is increasing the need for the design of new modulation methods. Each modulation method has its advantages and disadvantages based on the topology of converter and its application domain. The modulation techniques are classified based on the switching frequency. PWM methods based on carrier are classified as level shifted modulation scheme and phase shifted modulation scheme [7]. The carrier waveforms generally used are triangular waveform, saw-tooth waveform and constant waveform. The reference waveforms generally used are sinusoidal waveform, sinusoidal injected with third harmonic waveform and trapezoidal waveform.

The cascaded multi level inverter can be operated in symmetric configuration and asymmetric configuration. The magnitude of input DC voltage sources is equal in symmetric configuration. In asymmetric configuration, the magnitude of input DC voltage sources is unequal because of which more number of different voltage levels can be achieved. This way more number of output voltage levels can be achieved by using lesser number of switches with a reduced THD [16]-[17].

In this research, 17 level symmetric multi level inverter topology and 17 level asymmetric multi level inverter topology are proposed. The proposed symmetric hybridized multilevel inverter topology consists of a modified H-bridge inverter, which results in an increase in the output voltage to five level from the three level by using a bi-directional switch at the midpoint of a dual-input dc source. In the proposed asymmetric multilevel inverter, dc sources are replaced with the switched capacitor unit, which in turn boosts the output voltage and produces twice the voltage levels at the loads. The proposed Symmetric hybridised multilevel inverter is implemented using Level Shifting PWM techniques like Phase Disposition PWM, Phase Opposition Disposition PWM, Alternative Phase Opposition Disposition PWM. The proposed Asymmetric Switched capacitor unit multilevel inverter is implemented using stair case PWM technique.

II. Hybridised H-Bridge Inverter Topology

Of all the available configurations, H-Bridge supports high power levels with the use of low voltage rating components in inverters. In case of fault in any one cell, it can be replaced easily and quickly because of its modularity property. The Cascaded H-Bridge MLI configuration has series connected H-Bridge cells with isolated dc voltage supply connected to each cell. For higher voltage levels cascaded configuration is preferred as it requires less number of switching devices comparatively.

The basic H-Bridge topology produces a three level output voltage waveform with voltage levels as +V, 0V, -V. By adding a bidirectional switch between supply and the H-Bridge, the basic H-Bridge inverter topology is converted to Hybridised H-Bridge inverter topology. The output of hybridised H-Bridge inverter configuration is five level voltage waveform with voltage levels +2V, +1V, 0V, -1V, -2V.

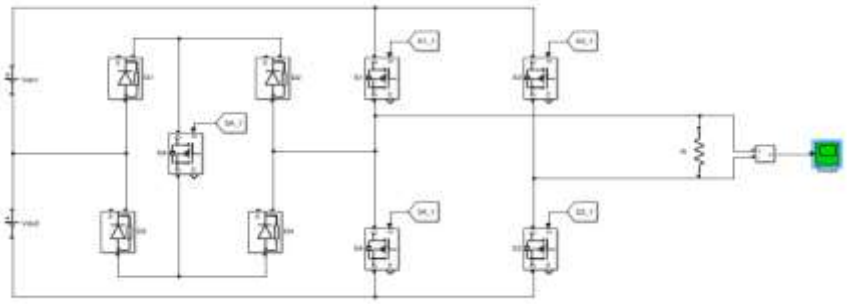

Fig1. Hybridised H-Bridge Inverter

The power semiconductor switches are triggered as per the switching sequence given in the below table to create five level output voltage waveform.

The switching state table for Hybridised H-bridge Inverter is as below :

Switches	S1	S2	S3	S4	SA
Output Voltage Level					
+2	1	1	0	0	0
+1	0	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
-1	0	0	1	0	1
-2	0	0	1	1	0

Table 1 : Switching sequence for Hybridised H-Bridge Inverter

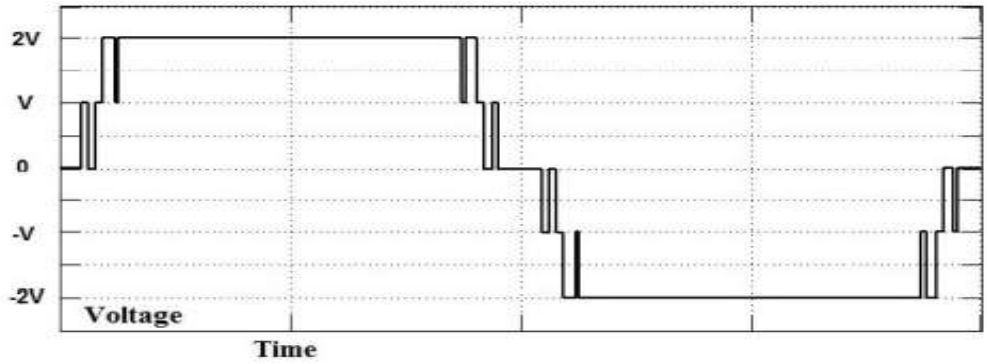

Fig2. Hybridised H-Bridge Inverter Output voltage waveform

The hybridized H-Bridge configuration cells can be cascaded to get the required number of output voltage levels. The Cascaded Multi-level inverter configuration can be operated in two modes: Symmetric Configuration mode and Asymmetric Configuration mode.

In Symmetric configuration, the magnitude of the input DC sources is same. It produces output voltage waveform with less number of voltage levels and a higher THD than asymmetric configuration. In Asymmetric configuration, the magnitude of the input DC sources are different. This asymmetrical configuration produces output voltage waveform with higher number of voltage levels and thus lesser THD.

In this research work, Symmetric configuration is considered. The work proposes a 17 level Symmetric Hybridised Cascaded Multi Level Inverter. Four cells of Hybridised H-Bridge topology are cascaded together to produce a 17 level Symmetric Hybridised Cascaded MLI output voltage waveform.

III. 17 Level Symmetric Hybridised Cascaded Multilvel Inverter

The proposed 17 level Symmetric Hybridised Cascaded MLI configuration is developed with an input voltage source of 24 volts and tested for different R and RL loads.

Each Hybridised H-Bridge topology cell is given an input voltage supply of 24 volts and an RL-Load of 100+j10 Ohms is connected across the whole multi level inverter configuration. The pulse generators of hybridized H-Bridge cells are switched at different times using staircase modulation technique such that a 17 level output voltage waveform is generated.

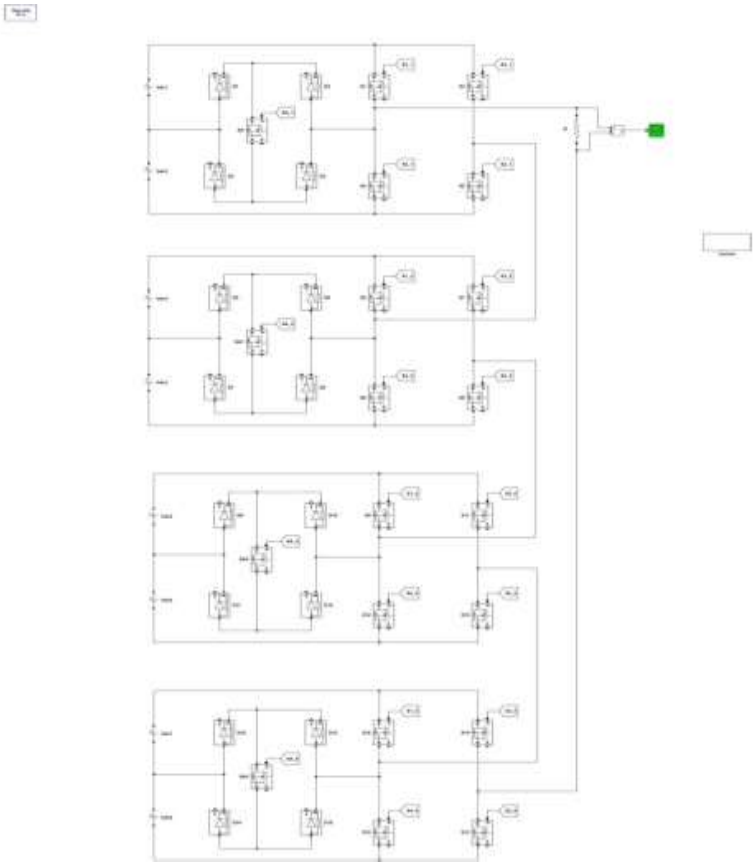

Fig3. 17 Level Symmetric Cascaded Hybridised H-Bridge Multilevel Inverter

The power semiconductor devices of each H-Bridge are triggered at different time instants to generate the 17 level output voltage waveform. The switching state table for the 17 level Symmetric Hybridised Cascaded MLI is as below

Voltage level	1	2	3	4	5	6	7	8	0	0	-1	-2	-3	-4	-5	-6	-7	-8
Switches																		
S_1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S_5	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S_9	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_{13}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S_A	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
S_B	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0

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S_D	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	

Table 2 : Switching sequence for 17 level Symmetric cascaded Hybridised H-Bridge multilevel Inverter

With the above switching states, the 17 level output voltage waveform is generated as below.

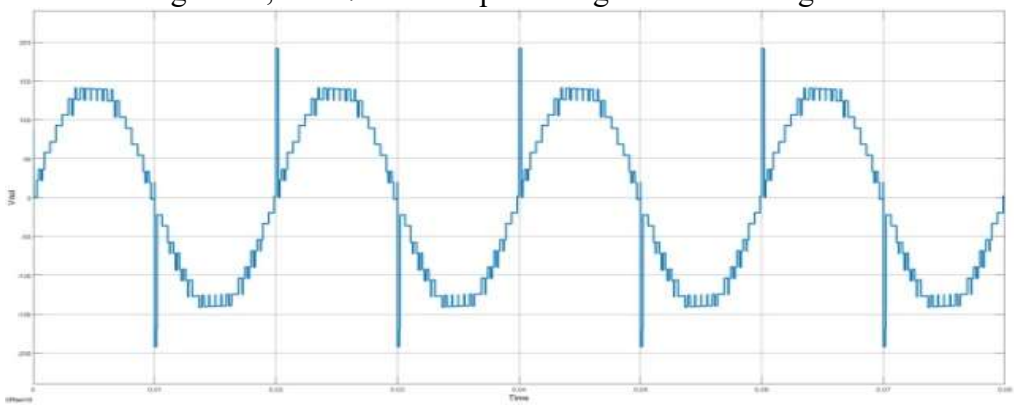

Fig4. 17 level Output voltage waveform of Symmetric cascaded hybridised H-Bridge MLI

The 17 level output voltage waveform is generated with a maximum voltage of 147V. The total harmonic distortion of the output voltage waveform is calculated using FFT analysis and is observed as 12.91%.

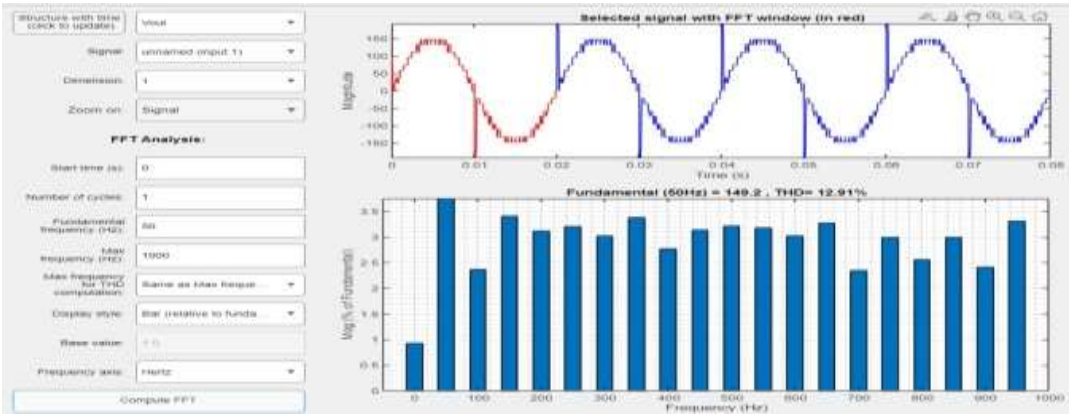

Fig5. %THD calculation of 17 level output voltage waveform

To decrease the THD in the output voltage waveform, different modulation techniques can be implemented in the circuit. With the increase in advancements of Multi Level Inverters, the need for new modulation techniques is also increasing. This led to the development of many new modulation techniques. These modulation methods are classified on the basis of switching frequency i.e., low switching frequency and high switching frequency.

Low switching frequency modulation methods include :

1) Selective Harmonic Elimination modulation method
2) Nearest vector modulation method
3) Nearest level modulation method
4) Hybrid modulation method

High switching frequency modulation methods include :

1) Hybrid modulation method
2) Multicarrier PWM modulation method
   a) Level shifted PWM – PD PWM, POD PWM, APOD PWM
   b) Phase shifted PWM
3) Space Vector modulation method

Depending on the converter topology and its application, each modulation has its own advantages and disadvantages.

As MOSFET has high switching frequency, High switching frequency modulation methods are preferred. In this Research work, Level shifted multicarrier PWM modulation method is considered.

IV. Level Shifted Multi Carrier PWM method

Level Shifted PWM method:

Multi carrier PWM methods are used in inverters which produce output voltage of three levels or more than three levels. In Level shifted PWM technique, n-1 carrier signals are vertically shifted to each other where n is number of inverter output voltage levels.

Level shifted PWM technique is classified into three techniques based on the phase difference between the carrier signals. They are :

1. Phase Disposition PWM technique (PD PWM)
2. Phase Opposition Disposition technique (POD PWM)
3. Alternative Phase Opposition Disposition technique (APOD PWM)

a) Phase Disposition PWM technique :

In this technique, all the carrier signals are in same phase.

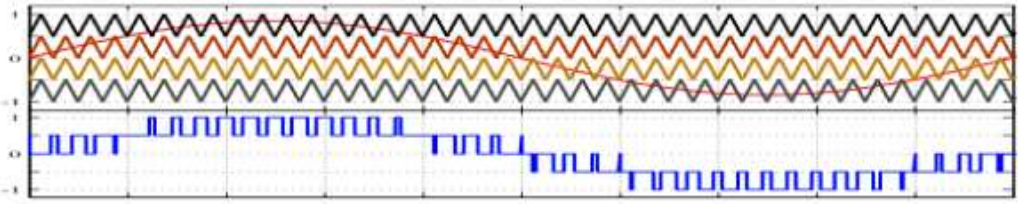

Fig6. Phase Disposition PWM technique

b) Phase Opposition Disposition PWM technique :

In this technique, all the carrier signals above zero are out of phase with those below zero by 180 degrees.

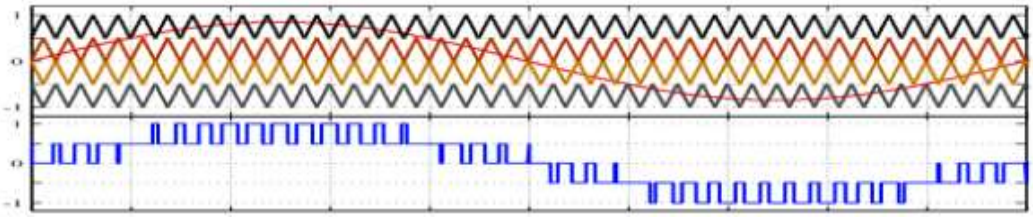

Fig7. Phase Opposition Disposition PWM technique

c) Alternative Phase Opposition Disposition technique :

In this technique, all the adjacent carrier signals are out of phase by 180 degrees.

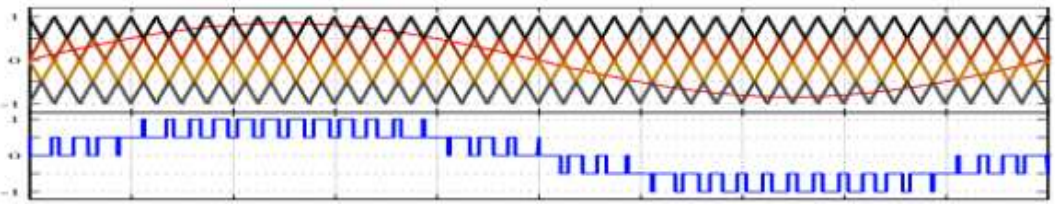

Fig8. Alternative Phase Opposition Disposition PWM technique

Level shifted PWM techniques are mostly used to produce high quality output waveforms. Triangular, Saw tooth and Constant DC magnitude waveforms can be used as Carrier signals. Sinusoidal, Sinusoidal injected with third harmonic and Trapezoidal waveforms can be used as Reference signals. In this work, Triangular carrier signal and Sinusoidal reference signal are considered.

V. Asymmetric Switched Capacitor Unit Multilevel Inverter

Multilevel Inverters with asymmetrical voltage sources (Capacitors) are used to reduce the number of semiconductor devices used and increase the number of output voltage levels. Switched Capacitor

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Multilevel inverters are introduced to reduce the number of DC voltage sources, semiconductor devices and generate multiple voltage levels. The common architecture of this multilevel inverter configuration consists of a switched capacitor based DC-DC converter that can produce multiple output voltage levels at the DC bus. This conversion of voltage is done by charging the switched capacitor to input voltage magnitude by connecting switched capacitor in partial to the input voltage source initially and then by connecting the input voltage source and switched capacitor in series to the load. The number of voltage sources can be increased based on the required number of output voltage levels.

Basic Switched Capacitor Unit :

The basic switched capacitor unit consists of an input voltage source, a diode, two semiconductor switches, a capacitor. The switched capacitor outputs the input voltage by twice at the load end. The capacitor will charge through switch S2 when input voltage is applied and will discharge through switch S1. When the capacitor is charging, it charges to input voltage and the load voltage is equal to input voltage. When the capacitor is discharging, the load voltage is equal to the sum of input voltage and capacitor voltage. Thus the switched capacitor unit configuration produces +V and +2V output voltages at the load ends with lesser number of switches.

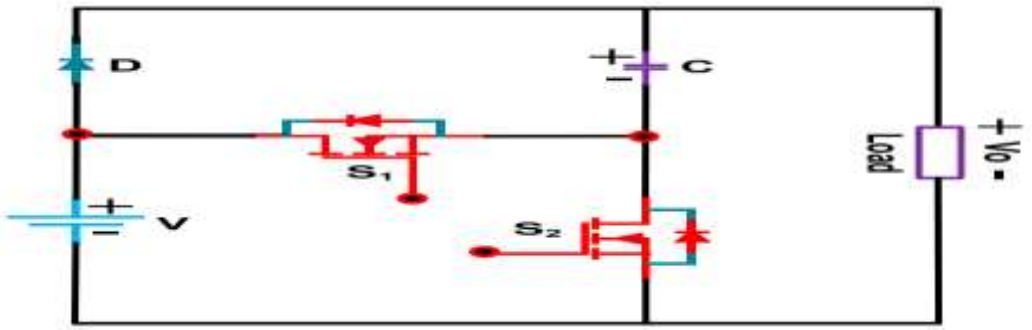

Fig9. Basic Switched Capacitor Unit

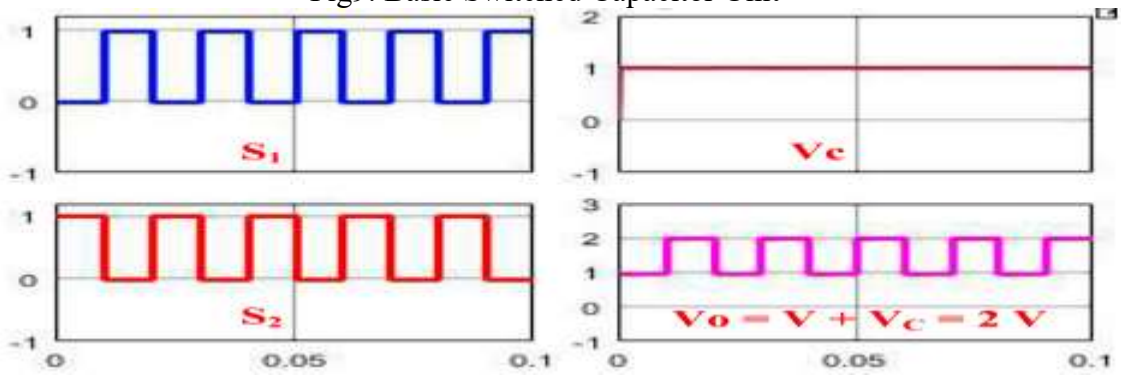

Fig10. Switching sequence of switches S1 and S2, Capacitor Voltage waveform, Output Voltage waveform

VI. Simulation Results

Implementation of Level Shifted PWM technique Control circuit for 17 Level Symmetric Cascaded Hybridised H-Bridge MLI and Simulation results

The Level shifted PWM techniques are implemented in the 17 Level Hybridized Symmetric Multilevel Inverter by using the control circuit as shown below.

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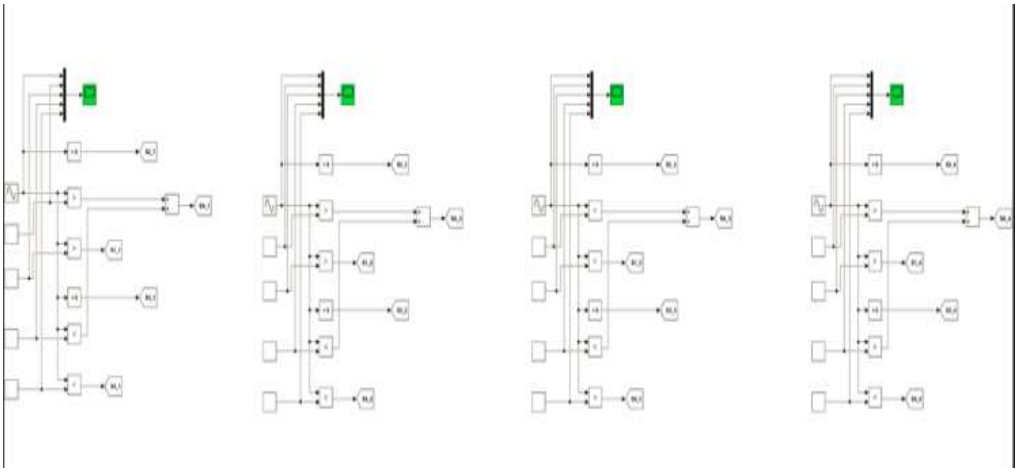

Fig.11 Control circuit for Level shifted PWM technique in Symmetric MLI configuration

a) Phase Disposition PWM technique :

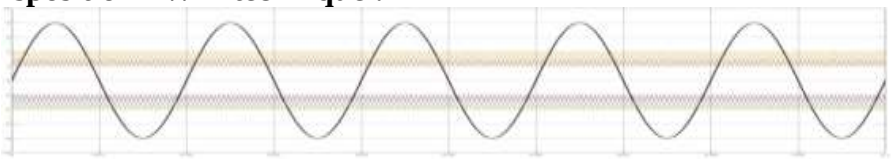

Fig12. Level 1 Phase Disposition PWM

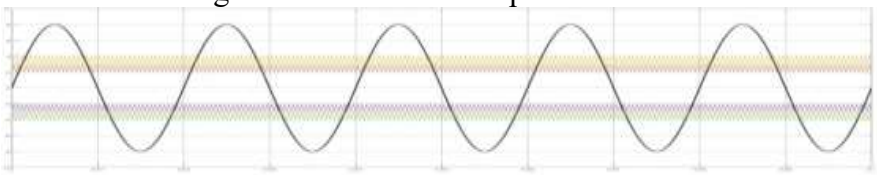

Fig13. Level 2 Phase Disposition PWM

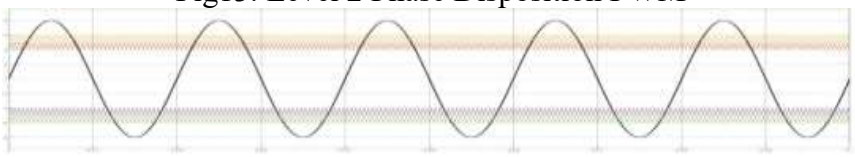

Fig14. Level 3 Phase Disposition PWM

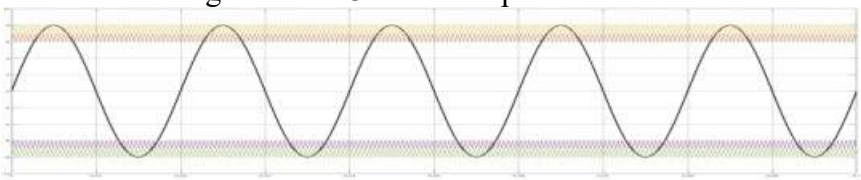

Fig15. Level 4 Phase Disposition PWM

The switching pulses are generated by comparison of sinusoidal reference wave and triangular carrier waves at different levels as shown above. The output voltage generated by Phase Disposition PWM technique is as below.

Supply Voltage : 24V

Load : 100+j10 Ohms

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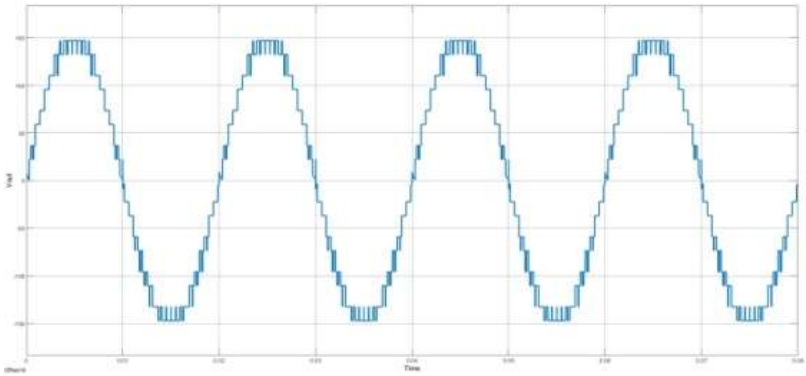

Fig16. 17 Level Output voltage waveform of Symmetric Cascaded Hybridised H-Bridge MLI with Phase Disposition PWM technique

A 17 level output voltage waveform is generated with a maximum voltage magnitude of 147V. The Total Harmonic Distortion of the output voltage waveform is calculated by applying the FFT analysis.

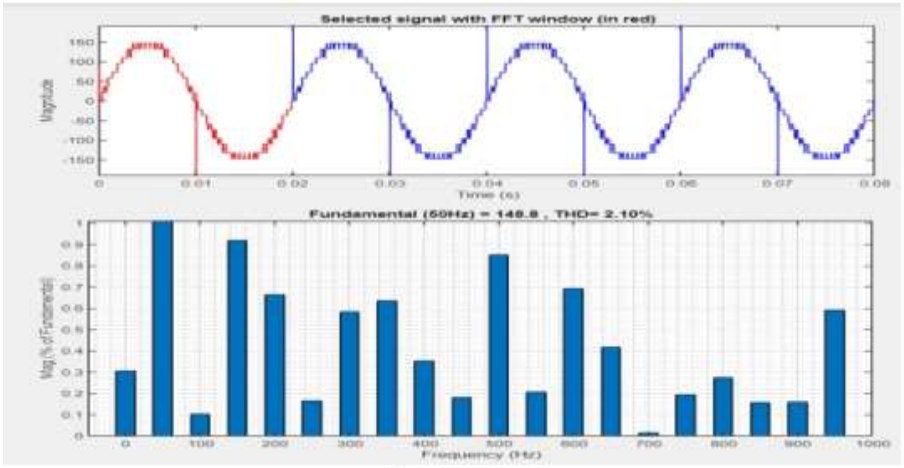

Fig17. %THD Calculation of 17 Level output Voltage waveform with Phase Disposition PWM technique

The THD of the output voltage waveform is 2.10%.

b) Phase Opposition Disposition technique :

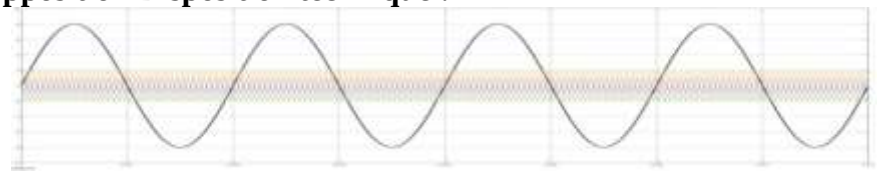

Fig18. Level 1 Phase Opposition Disposition PWM

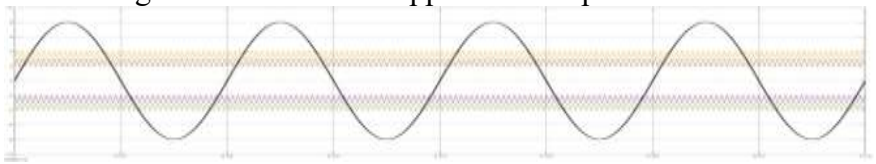

Fig19. Level 2 Phase Opposition Disposition PWM

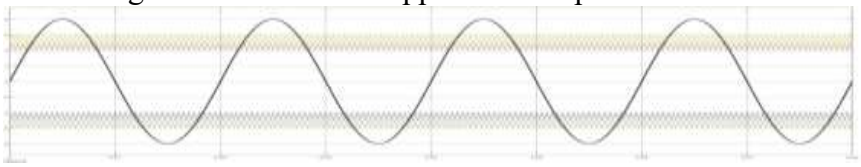

Fig20. Level 3 Phase Opposition Disposition PWM

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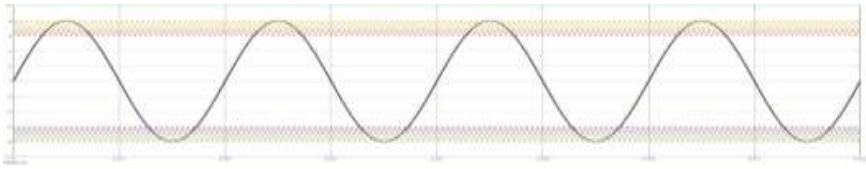

Fig21. Level 4 Phase Opposition Disposition PWM

The switching pulses are generated by sinusoidal reference wave and triangular carrier waves at different levels as shown above. The output voltage generated by Phase Disposition PWM technique is as below.

Supply Voltage : 24V

Load : 100+j10 Ohms

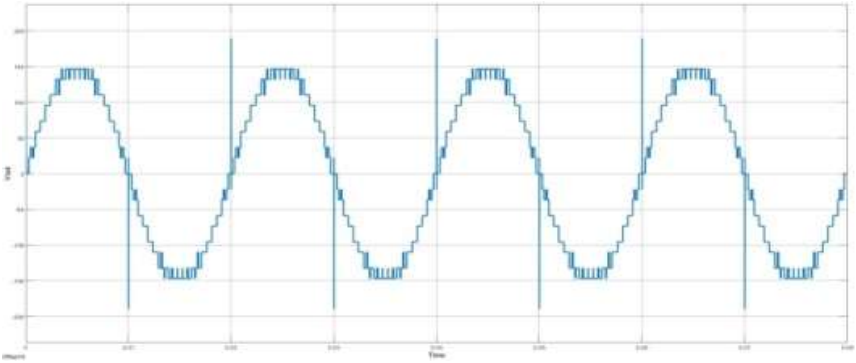

Fig22. 17 Level Output Voltage waveform for Symmetric Cascaded Hybridised H-Bridge MLI with Phase Opposition Disposition technique

A 17 level output voltage waveform is generated with a maximum voltage magnitude of 147V. The Total Harmonic Distortion of the output voltage waveform is calculated by applying the FFT analysis.

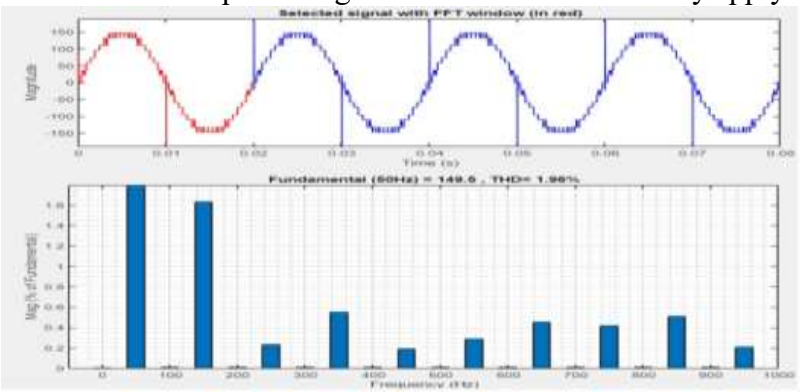

Fig23. %THD calculation of 17 level Output voltage waveform with Phase Opposition Disposition PWM technique

The THD of the output voltage waveform is 1.96%.

c) Alternative Phase Opposition Disposition technique :

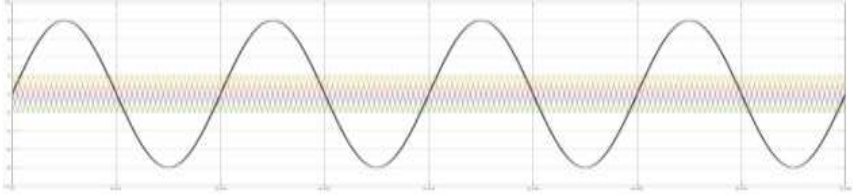

Fig24. Level 1 Alternative Phase Opposition Disposition PWM

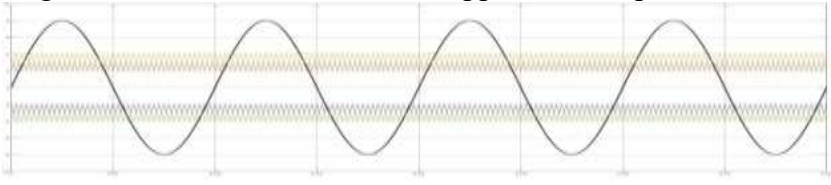

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Fig25. Level 2 Alternative Phase Opposition Disposition PWM

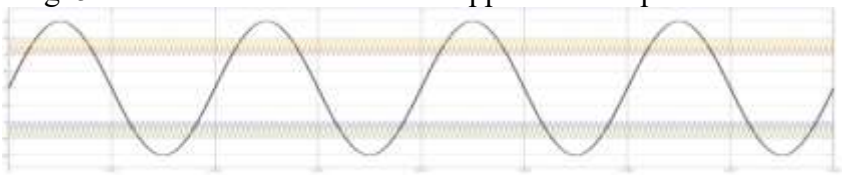

Fig26. Level 3 Alternative Phase Opposition Disposition PWM

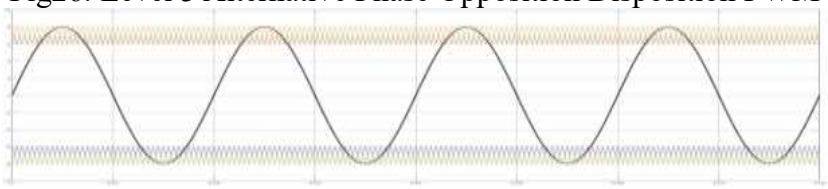

Fig27. Level 4 Alternative Phase Opposition Disposition PWM

The switching pulses are generated by sinusoidal reference wave and triangular carrier waves at different levels as shown above. The output voltage generated by Phase Disposition PWM technique is as below.

Supply Voltage : 24V

Load : 100+j10 Ohms

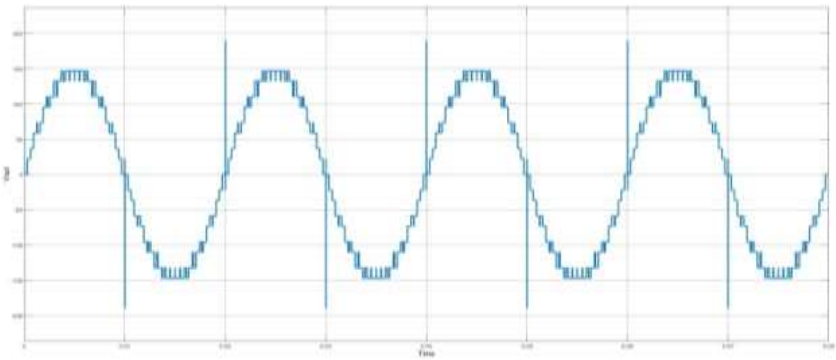

Fig28. 17 Level Output Voltage Waveform for Symmetric Cascaded Hybridised H-Bridge MLI with Alternative Phase Opposition Disposition PWM technique

A 17 level output voltage waveform is generated with a maximum voltage magnitude of 147V. The Total Harmonic Distortion of the output voltage waveform is calculated by applying the FFT analysis.

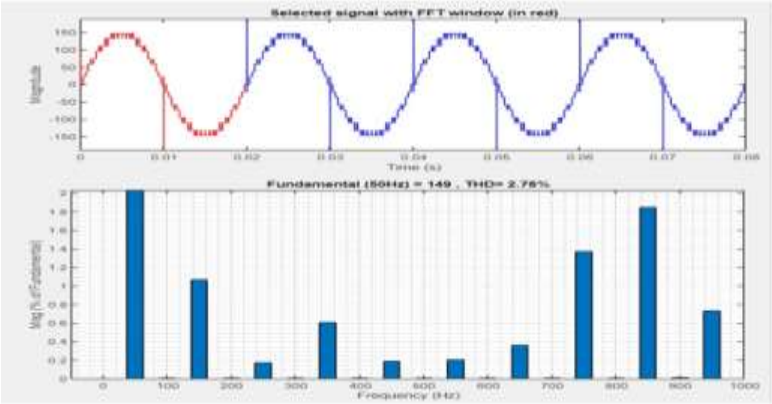

Fig29. %THD Calculation of 17 Level Output Voltage Waveform with Alternative Phase Opposition Disposition PWM technique

The THD of the output voltage waveform is 2.76%.

Performance Analysis of Symmetric Cascaded Hybridised H-Bridge MLI with PD PWM, POD PWM and APOD PWM

The maximum voltage of the output voltage waveform and total harmonic distortion of the output voltage waveform for different loads is calculated and tabulated as below :

1. Phase Disposition technique:

Input Voltage(V)	Load(Ohms)	Maximum Voltage (V)	%THD
24	10	+/- 139.5	2.05
24	100	+/- 147	2.08
24	10+j10	+/- 140	11.51
24	100+j10	+/- 147	2.10
24	100+j100	+/- 147	12.91

Table 3 : Maximum voltage and %THD calculation of Symmetric Cascaded Hybridised H-Bridge MLI with Phase Disposition PWM

2. Phase Opposition Disposition technique:

Input Voltage(V)	Load(Ohms)	Maximum Voltage (V)	%THD
24	10	+/- 139.5	2.02
24	100	+/- 147	1.87
24	10+j10	+/- 141.5	10.90
24	100+j10	+/- 147	1.96
24	100+j100	+/- 147	12.77

Table 4 : Maximum voltage and %THD calculation of Symmetric Cascaded Hybridised H-Bridge MLI with Phase Opposition Disposition PWM

3. Alternative Phase Opposition Disposition technique :

Input Voltage(V)	Load(Ohms)	Maximum Voltage (V)	%THD
24	10	+/- 139	2.74
24	100	+/- 146	2.53
24	10+j10	+/- 141	10.59
24	100+j10	+/- 147	2.76
24	100+j100	+/- 147	12.37

Table 5 : Maximum voltage and %THD calculation of Symmetric Cascaded Hybridised H-Bridge MLI with Alternative Phase Opposition Disposition PWM

From the tabulations above, it can be concluded that Phase Opposition Disposition technique has provided comparatively less harmonic distortions.

This cascaded multilevel inverter configuration can produce higher output voltages with reduced THD. But, if more higher voltage levels are required, the number of semiconductors and the DC voltage sources used increases. Thus reducing the quality of the output voltage and increasing harmonics and THD. To overcome this issue, asymmetric configuration can be used.

Implementation of 17 level Asymmetric Switched Capacitor Unit and Simulation results

The proposed switched capacitor unit topology for producing 17 level output voltage waveform consists of two input voltage sources, two capacitors, two diodes, ten semi conductor switches and two capacitors in two switched capacitor units. The pulses for the semi conductor switches are produced individually.

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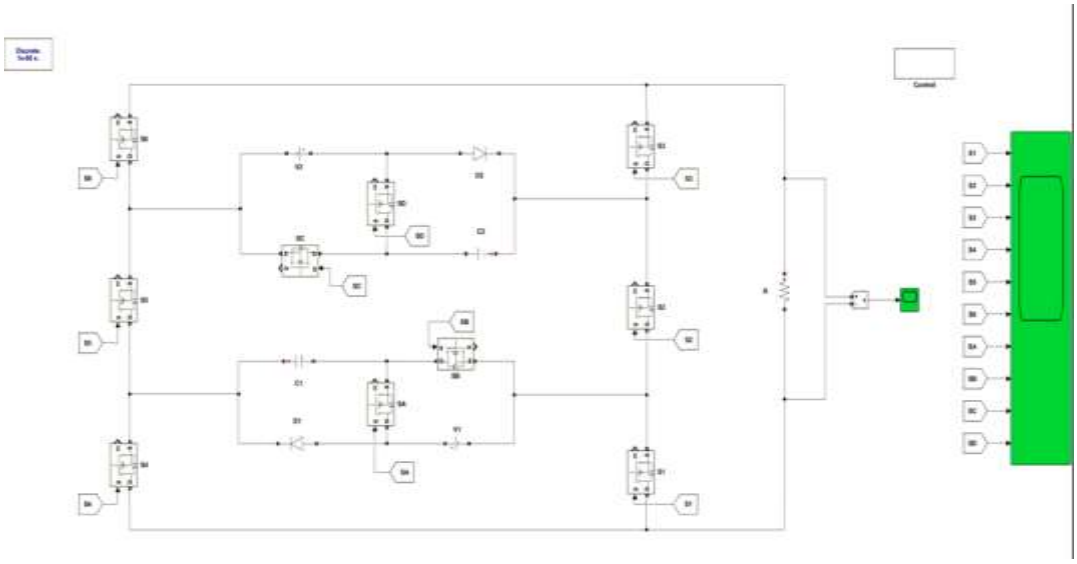

Fig30. 17 Level Asymmetric Switched Capacitor Unit MLI topolgy

The triggering pulses are provided to the semiconductor switches from the control circuit. The control circuit of the Asymmetric Switched capacitor unit is as shown below.

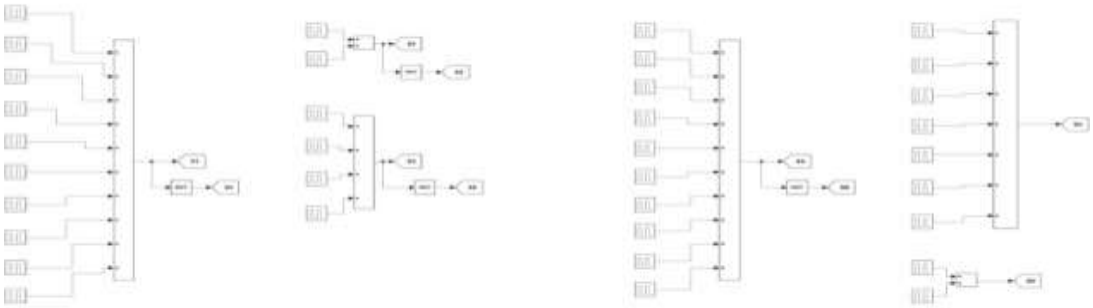

Fig31. Control circuit of Asymmetric Switched Capacitor Unit MLI

The control circuit for asymmetric switched capacitor unit MLI is developed using the below switching sequence. Switches S1 and S4 complement each other. Switches S2 and S5 complement each other. Switches S3 and S6 complement each other. Switches SA and SB complement each other.

The switching sequence for the asymmetric configuration is tabulated below.

Vo level	S_1	S_2	S_3	S_4	S_5	S_6	S_A	S_B	S_C	S_D
1	1	0	1	0	1	0	1	0	0	1
2	1	0	1	0	1	0	0	1	0	1
3	0	0	1	1	1	0	0	1	1	0
4	1	0	1	0	1	0	1	0	1	0
5	1	0	1	0	1	0	0	1	1	0
6	0	0	1	1	1	0	0	1	1	0
7	1	0	0	0	1	1	1	0	0	1
8	1	0	0	0	1	1	0	1	0	1
9	1	1	1	0	0	0	0	1	1	0
10	0	1	1	1	0	0	0	1	0	1
11	0	1	1	1	0	0	1	0	1	0

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12	1	1	0	0	0	1	0	1	1	0
13	0	1	0	1	0	1	0	1	1	0
14	0	1	0	1	0	1	1	0	1	0
15	1	1	0	0	0	1	0	1	0	1
16	0	1	0	1	0	1	0	1	0	1
17	0	1	0	1	0	1	1	0	0	1

Table 6 : Switching Sequence of Asymmetric Switched Capacitor Unit

The output waveforms of Asymmetric Switching Capacitor Unit control circuit are as below.

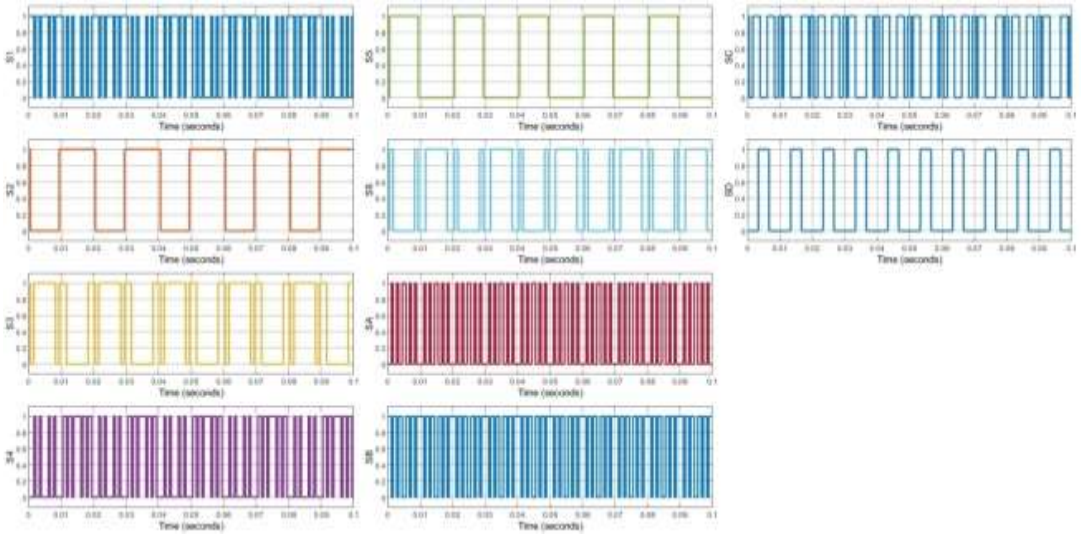

Fig32. Output waveforms of Asymmetric Switched Capacitor Unit Control Circuit

With the triggering pulses provided to the asymmetric switching capacitor unit, the output voltage waveform generated as in the below figure.

V1 = 24V

V2 = 48V

Load : 100+j10 Ohms

Load : 100+j10 Ohms

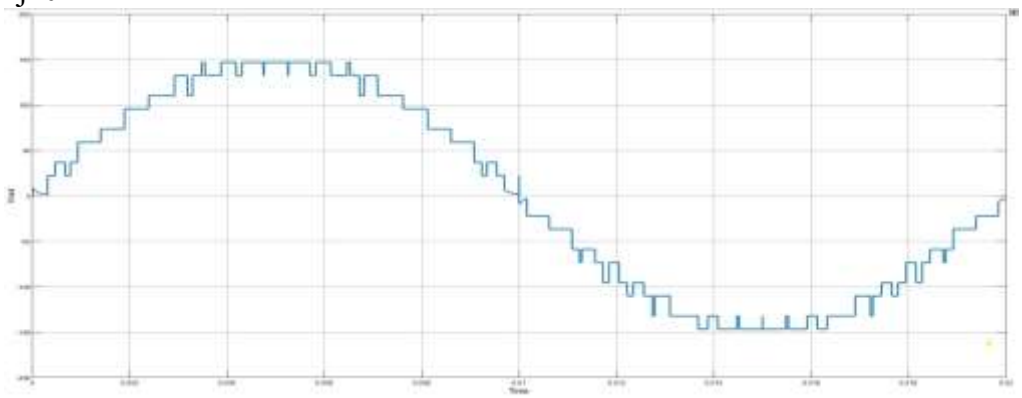

Fig.33 17 Level Output Voltage waveform of Asymmetric Switched Capacitor Unit MLI

The Total Harmonic distortion of the output voltage waveform is calculated using the FFT analysis.

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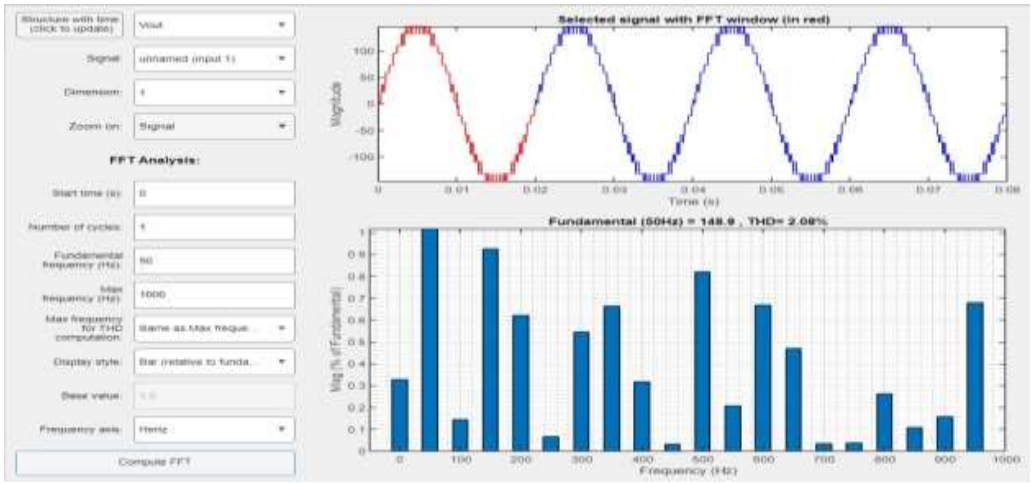

Fig.34 %THD Calculation of 17 Level Output Voltage Waveform of Asymmetric SCU MLI

Performance Analysis of Asymmetric SCU MLI

The total harmonic distortion of the output voltage waveform for different loads is calculated and tabulated as below :

Input Voltage(V)	Load(Ohms)	Maximum Voltage(V)	%THD
24	10	+/- 126	3.65
24	100	+/- 140	2.94
24	10+j10	+/- 130	9.07
24	100+j10	+/- 141	2.08
24	100+j100	+/- 141	10.19

Table 7 : Maximum voltage and %THD calculation of Asymmetric SCU MLI

Comparison of Symmetric Cascaded H-Bridge MLI and Asymmetric Switched Capacitor Unit MLI

MLI Configuration	No. of Switches	No. of Power Supplies	No. of Capacitors	%THD
Symmetrical Cascaded H-Bridge MLI	36	8	0	12.91% PD PWM – 2.55% POD PWM – 1.96% APOD PWM – 2.76%
Asymmetrical Switched Capacitor Unit MLI	10	2	2	2.08%

Table 8 : Comparison of Symmetric MLI and Asymmetric MLI

VII. Conclusion :

This work implements and analyses 17 level Symmetric Cascaded H-bridge MLI with different level shifted PWM techniques and 17 level Asymmetric Switched Capacitor unit MLI. The proposed configurations are tested for R-loads and RL-loads. The proposed multilevel inverter configurations maintain almost stable output voltage with reduced %THD. These topologies also use less number of power supplies and semiconductor devices. A THD of 1.96% is achieved with Phase Opposition

Disposition PWM technique for Symmetric MLI configuration and a THD of 16.01% is achieved with Asymmetric MLI configuration. Symmetric Cascasded H-Bridge multilevel inverter finds its application in static VAR applications, renewable energy and battery-based applications. Asymmetric Switched Capacitor unit MLI configuration has applications in designing electronic filters, telecommunication systems and power converters.

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