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MUX BASED CELL DESIGN FOR TESTING OF INTEGRATED CIRCUITS THROUGH SCAN INSERTION USING MENTOR GRAPHICS - TESSENT

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Abstract:

In the design of Integrated circuits defects arise in the fabrication process which leads to malfunctioning of the chip. The defect is a physical imperfection that occurs in the manufacturing process. These defects are tested with test logic that is to be inserted along with the actual logic that resides on the chip. The test logic will identify the manufacturing defects. The defects are analyzed in the form of logical faults. The chip logic consists of combinational logic gates and flip-flops. Fault may occur in the combinational logic or sequential logic. To target these faults due to defects with the help of test logic which is based on multiplexer logic. The project aims at adding the multiplexer logic to flip-flop will be used to identifying the defects, that cause faults will be analyzed using Mentor graphics.

Keyword : Mentor graphics, Tessent, Fabrication

I. Introduction

Design for Testability is a design method that makes chip testing feasible and affordable by including more circuitry on the chip. These DFT techniques are necessary to improve the digital circuit's quality and lower test costs while also streamlining test, debug, and diagnosis activities. Structured DFT techniques, in which direct external access is granted for storage elements, were adopted as a result of difficulties in monitoring and managing the internal states of sequential circuits. The term "scan cells" is frequently used to describe these modified storage components with direct external access. Currently, the most widely used structured DFT methodology is scan design. Selected storage components from a design are connected into several shift registers, referred to as scan chains, to provide them access from the outside. Scan design completes this process by substituting scan cells for all chosen storage elements, each of which has one shared or additional scan output (SO) port and one additional scan input (SI) port. One or more scan chains are formed by coupling the SO port of one scan cell to the SI port of the following scan cell. The DFT flow is represented below

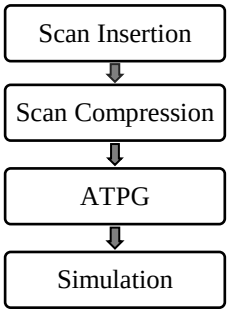

Figure 1: DFT FLOW

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A scan cell typically has two input sources from which to choose. In order to create one or more shift registers known as scan chains, the first input, referred to as the data input, is driven by the combinational logic of a circuit, whereas the second input, referred to as the scan input, is driven by the output of another scan cell. By attaching the output of the final scan cell in a scan chain to a primary output and the scan input of the first scan cell in a scan chain to a primary input, these scan chains are made externally accessible.

Given that a scan cell has two input sources, a selection mechanism is necessary to enable the scan cell to operate in both normal or capture mode and shift mode. In normal or capture mode, the option to update the output with the data entered is chosen. Scan input is chosen to update the output in shift mode. The contents of all scan cells can then be shifted out through one or more primary outputs while an arbitrary test pattern can be shifted in from one or more primary inputs to all scan cells as a result. The muxed -D scan, the clocked-scan, and the level-sensitive scan design are three popular scan cell designs that are discussed in this section (LSSD).

II. Literature

[1] The VLSI test scan architecture is not universal; depending on the design, a different form of scan architecture or a technique tailored to a particular type of scan architecture must be used. All different types of designs cannot be tested with a single scan. Each type of scanning architecture has unique benefits, drawbacks, performance characteristics, and applications.

[2] Defects could be anywhere on scan enable trees or scan clock trees. They will have an impact on shift, capture, or both operations. When the clock trees or scanners have several defects, it will be more challenging. To ensure the accuracy and resolution of diagnoses, algorithms have been devised.

The mux-based cell design, which is explored in more detail later in the paper, is a muxed-D full scan architecture used over a circuit design to produce DRC violations and other outcomes.

III. Proposed work

In this study, we demonstrate the scan insertion and scan compression steps of the DFT technique applied to a logic circuit with 40 flip-flops. It uses Mentor Graphics®, a leader in electronic design automation (EDA) technology and a provider of software and hardware design solutions. Making diagnoses requires the use of Mentor Graphics-Tessent. Data from manufacturing tests, scan test patterns, and design information were utilised by Tessent. Its diagnosis pinpointed the location and type of fault that was causing the failure. In the end, the corresponding DRC infractions are seen

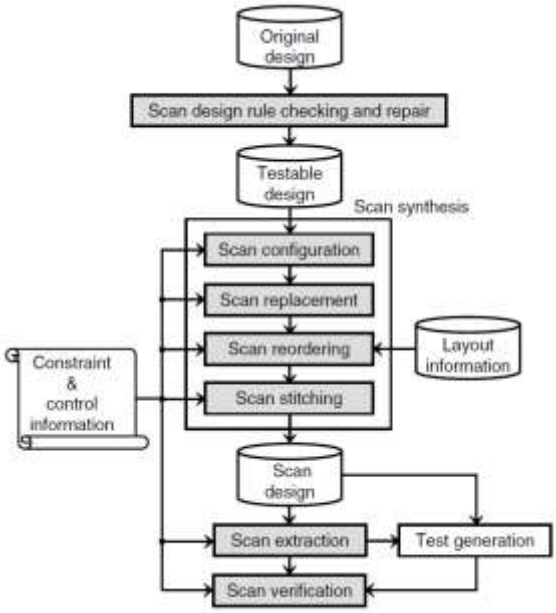

Figure 2: Scan Design Flow

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IV. Methodology

To transform the original design into a tested design, all scan design rule breaches must be found and fixed before a scan design can be implemented. The testable design can satisfy target fault coverage specifications, and the scan design will function properly after these violations are fixed. Certain clock control structures may need to be incorporated in addition to these scan design guidelines for at-speed delay testing. After scan synthesis, the scan design is typically additionally subjected to scan design rule checking to make sure there are not any new violations.

Some of the scan design rules that are verified:

scan design rules:

- For all state variables, only clock D-type flip-flops should be used.
- A minimum of one PI pin must be accessible for testing; additional pins may be used if they are available.
- Every clock must be managed by PIs.
- Flip-flop data inputs cannot be fed by clocks.

Scan Synthesis:

1. Scan Configuration

While configuring the scan design the following points are considered:

- The number of scan chains used
- The types of scan cells used to implement these scan chains
- The way the scan cells are arranged within the scan chains.

For the mentioned design in the paper, the Scan configuration is as below:

- The number of scan chains used- 5.
- The types of scan cells used to implement each scan chain- Muxed D- Scan cell.
- The scan cells are arranged within the scan chains in a clock domain with negative-edge and positive-edge

2. Scan Replacement

Here, all of the original storage components in the functionally tested design are replaced with equivalent scan cells through the process of scan replacement. A scan-ready design is frequently used to describe the testable following scan replacement.

3. Scan Reordering

In order to reduce the number of interconnect wires required to execute the scan chains, scan reordering is the process of rearranging scan cells in scan chains depending on the physical locations of the scan cells.

4. Scan Stitching

In order to create scan chains, all scan cells are stitched together in the last stage, known as “scan stitching”. According to the scan order, a process known as “scan stitching” entails joining each scan cell's output to its subsequent scan cell's scan input.

The below scan flip flop is added to the design of forty flip flops.

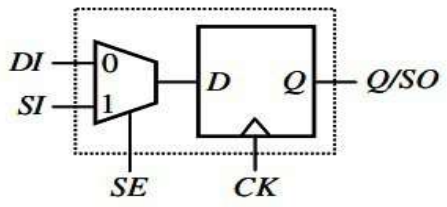

Figure 3: Muxed D-Scan Flip Flop

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V. Results

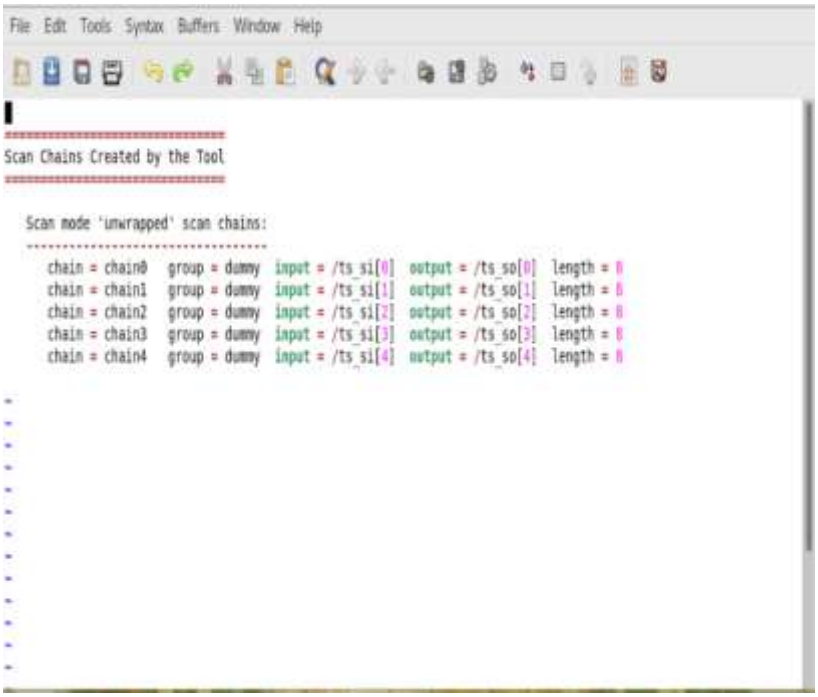

Figure 4.1: Report of resulted scan chain

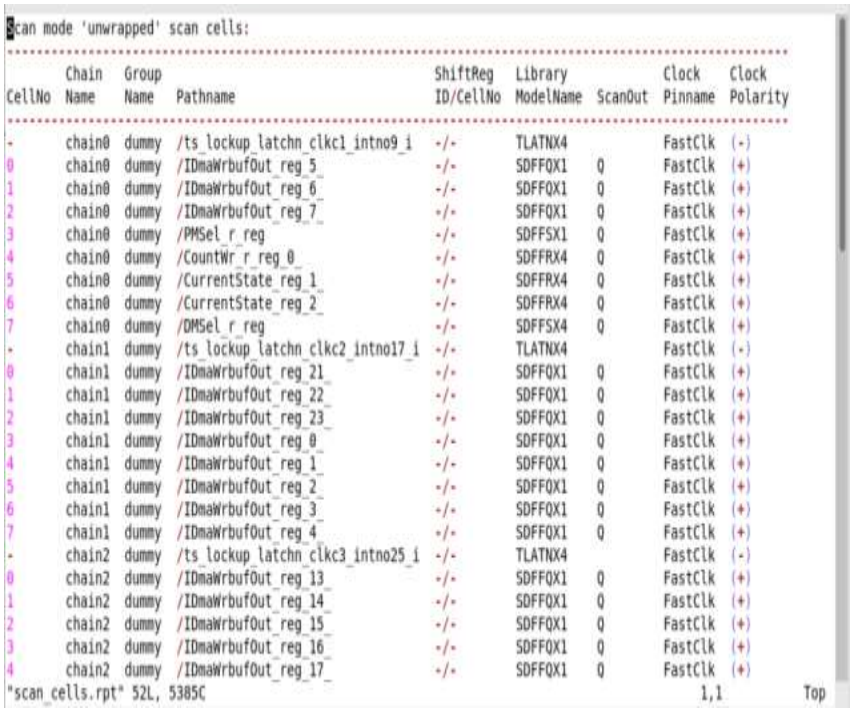

Figure 4.2: Reports of scan cells

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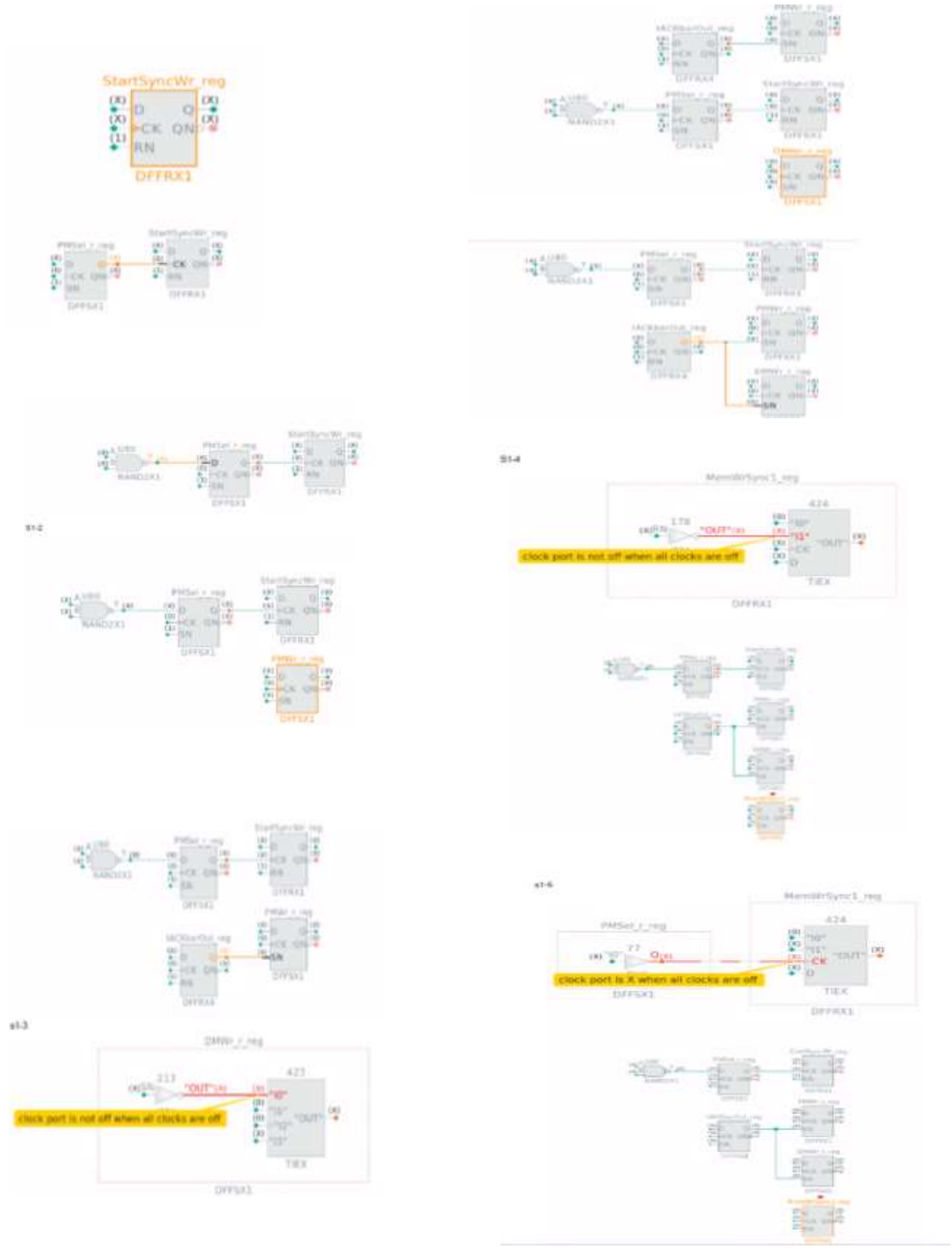

Figure 4.3: Reports of DRC Violations

VI. CONCLUSION:

An integrated circuit consisting of forty flip-flops is tested with a Mux-based cell design through scan insertion using the Mentor Graphics -Tessent. Through scan insertion, the additional test logic is added to implement DFT. The reports of scan cells and the scan chain are obtained. The ATPG file is also generated for the further implementation of DFT. Finally, in this paper, the Scan insertion and compression are presented and the DRC violations are found in the process and viewed by the tessent visualizer.

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