Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, January 2023

PERFORMANCE ANALYSIS OF NOVEL MOSFET ARCHITECTURE AS AN INVERTER

Aakansha, Manoj Kumar, Department of Electronics and Communication Engineering, Om Sterling Global university, Hisar, Haryana **aakanshabarala41@gmail.com[1], manoj10276@gmail.com[2]**

Abstract

In this manuscript, a new device structure working as an inverter (DGMOSFET-I) is proposed. The CMOS inverter is analyzed and working in a single device that incorporates NMOS and PMOS together. The lower transistor count is a major advantage of the proposed structure. This could enhance the growth of the industry by improving the power consumption. In the proposed device, a CMOS inverter uses a single substrate for both p-type and n-type devices. The reduction in the short channel effects provides a great advantage in achieving the performance of the device. In this paper, the proposed device is simulated at channel length 14nm. The OFF current of 10^{-9}A, subthreshold slope of 94.26mV/dec, threshold voltage of 0.18V is achieved. Also, the Voltage transfer characteristics (VTC), V-curve, SNM is calculated for the proposed CMOS inverter. In the proposed device, the reduction in the wells, junctions, oxide regions and simplicity in the fabrication of the device provides a boost to design such devices and leads to realization of such devices.

Keywords: MOSFET, Inverter, Double Gate, Subthreshold slope, Drain induced barrier lowering

1. Introduction

The growth of metal oxide semiconductor field effect transistor in the past few decades are accredited by the dimension scaling of the MOSFET. The increase in the packaging density and speed of the device are accompanied with the scaling of the device. This further increases the functionality of the device and reduces the power dissipation and chip cost. When the scaling of the device reaches below 22nm node, it welcomes some undesired effects called as short channel effects (SCE) [1-2]. The short channel effects starts deteriorating the performance of the device and thus carriers becomes uncontrolled. The intensification of the gate control can overcome the short channel effects and thus revamp the performance of the device. The different gate structures such as double gate [3-6], Tri-Gate, Gate all Around, Pie gate etc. increases the gate control over the carriers and thus SCE can be controlled even at lesser channel lengths. There are different architecture engineering being done by different authors in the literature such as dielectric engineering, Gate engineering, Material engineering, Oxide engineering, Core-shell engineering etc. to improve the performance of the device even at lesser channel lengths. Along with this, the circuit implementation using the proposed devices as an application has been covered in the literature. The common source amplifier using core-shell architecture, CMOS inverter using Dielectric pocket based double gate FET, and many more are available in the literature.

In this paper, we have proposed a double gate MOSFET architecture with highly improved performance working as an inverter. The most important characteristics of the proposed device lies in the fact that despite having a single transistor, a complete inverter action can be realized. Usually, a CMOS inverter is implemented using two types of transistor, N-type and P-type. The proposed device as an inverter has multiple advantages. The increase in packaging density, reduction in power dissipation, reduction in the number of transistor count for implementing the logic gates are all advantages of the proposed device. The proposed double gate MOSFET device as an inverter (DGMOSFET-I) consist of lesser regions, contacts and junctions. In the device, only one substrate is used to implement the inverter rather than two substrates in case of conventional CMOS inverter that also includes p-well or n-well. The complete CMOS inverter action is observed from the device in which both types of MOSFET (n-type and p-type) [7] are integrated into one called DGMOSFET-I. Further, the multifunctionality of the proposed device and reduction in the short channel effects will definitely extend the moore's law validity. In this paper, the detailed simulation of the proposed MOSFET as an inverter including the characteristics and calculation of the performance

parameters such as OFF current, ON current, ON/OFF current ratio, threshold voltage, subthreshold slope, drain induced barrier lowering has been performed for lower channel length. This paper covers the introduction of the DGMOSFET-I followed by the details of the device structure, simulation models, results and discussion and conclusion of the entire study.

2. Device Structure

The device DGMOSFET-I is designed using visual TCAD. The schematic of the device used for simulation is shown in figure1 The proposed device is observed such that both types of MOS are integrated into single device giving the characteristics of CMOS. The bottom gate and top gate of the proposed device controls the n-type and p-type MOSFET respectively. The source terminals of both n-type and p-type MOS are isolated by SiO2. The working of n-type and p-type MOSFET is made effective by selecting the proper work function of the gate material. The carrier mobility model which is an important parameter is selected for carrier transport. The Lombardi model which is an empirical model is used as mobility model in our simulation. This model basically consist of three components such as doping-dependent bulk mobility, mobility degradation due to acoustic phonon scattering, and mobility degradation due to surface roughness scattering. The Boltzmann transport carrier statistics is used during simulation [8].

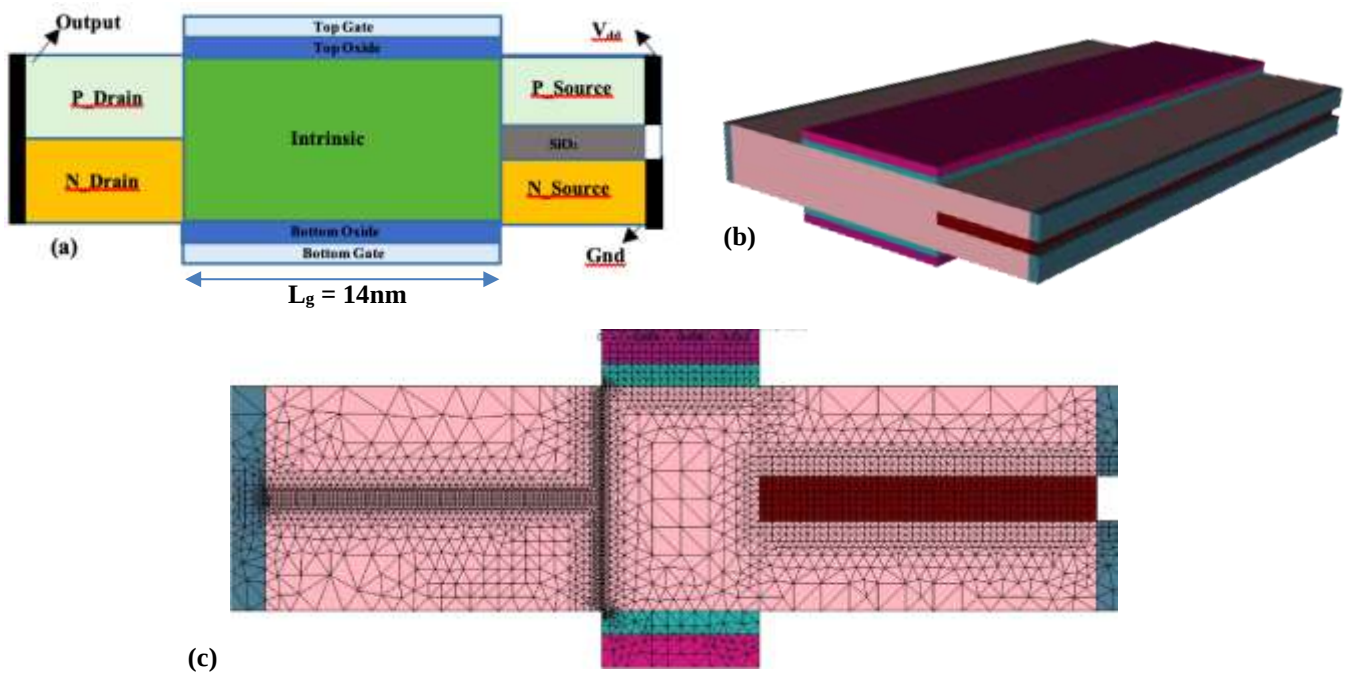

Figure 1. (a & b). Device Schematic of DGMOSFET-I in 2-D and 3-D view respectively c) Mesh structure of the proposed DGMOSFET-I.

Table 1. Device Parameters used during Simulation

Parameters	Values
Channel length	14 nm
n_i (intrinsic conc.)	$1\times10^{15}cm^{-3}$
N_drain	$1\times10^{20}cm^{-3}$
P_drain	$1\times10^{20}cm^{-3}$
N_source	$1\times10^{20}cm^{-3}$
P_source	$1\times10^{20}cm^{-3}$
Gate dielectric(k)	HfO_2=22

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, January 2023

Bottom Gate work function	4.6eV
Top Gate Work function	4.9eV

During the simulation of the proposed device, the impact ionization effect has not been considered. In the proposed device, it can be observed that there are less number of junctions, wells and oxide regions available as compared to conventional CMOS inverter [10]. This reduction in terms of junctions, wells exaggerate the performance of the device and reduces the short channel effects. This further leads to improvement in the speed and power of the device. The parameters considered for simulating the proposed device is tabulated in table 1.

Results and Discussion

The proposed DGMOSFET-I is known for its simplicity which motivates us to the study the performance of the inverter using double gate MOSFET. The working principal of the device exhibits the switching process of the inverter when gate voltage is changed in the NMOS and PMOS designed in a single device. When the input voltage is kept low, the formation of the channel gets start near to the top gate and as the source of the PMOS is kept at higher voltage therefore the output becomes high. When the input voltage is kept high, the formation of the channel gets start near to the bottom gate and as the source of the NMOS is grounded, therefore the output becomes low [9].

Further, the performance of the DGMOSFET as an inverter is studied at channel length 14nm. The different performance parameters such as threshold voltage, drain induced barrier lowering, subthreshold slope in linear and saturation mode are calculated. Also the detailed study related to the performance of inverter that includes, SNM curve, VTC curve are also analyzed.

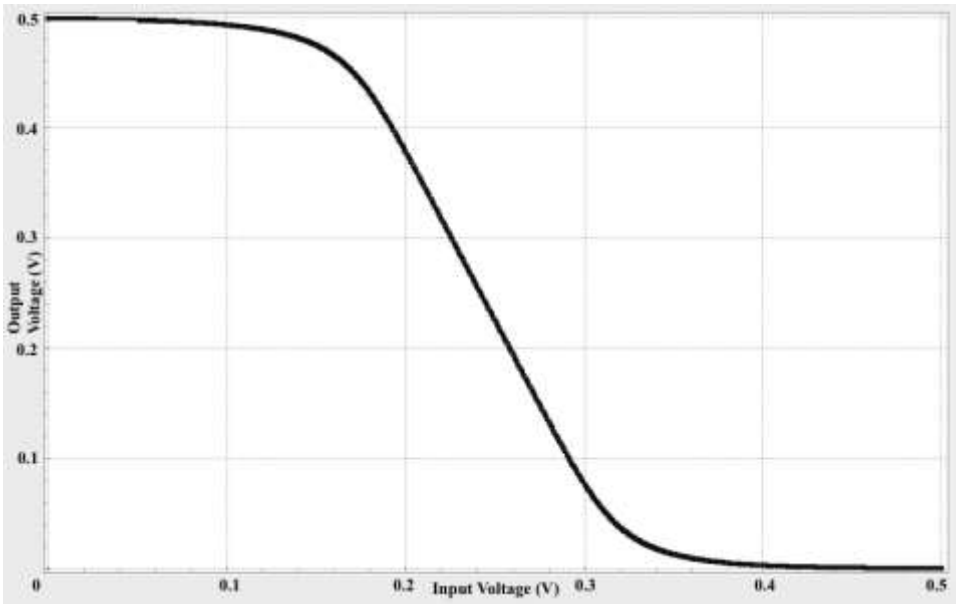

Figure 2. Voltage transfer characteristics of proposed DGMOSFET based Inverter

Figure 2 shows the voltage transfer characteristics of the proposed device at channel length 14nm. It has been observed that a sharp VTC curve is obtained for the device. The shard VTC curve exhibits the efficient working of the proposed inverter as compared to conventional CMOS inverter. The enhanced performance of the DGMOSFET in terms of SS, DIBL and other performance parameters exhibits the reduction in the delay while switching the signals. The sharp transition of the VTC curve is mainly due to lower OFF current of the device. The performance parameters calculated for the proposed DGMOSFET-I is presented in table 2.

Table 2. Performance parameters calculated for DGMOSFET-I

Parameters	**PMOS**	**NMOS**
Threshold voltage (V_{th})	0.206	0.183
Subthreshold slope (linear) (mV/decade)	103.84	94.26
DIBL (mV/V)	58	42

The threshold voltage for PMOS and NMOS are calculated as 0.206V and 0.183V. The subthreshold slope which is a basic feature of I-V characteristics. The steep subthreshold slope exhibits the faster transition between high (ON) states to low (OFF states). In the proposed device, the NMOS exhibits the SS of 94.26 mV/decade and PMOS exhibits the SS of 103.84mV/decade.

The best performance parameters of proposed double gate MOSFET helps to achieve the good performance of the inverter as an application.

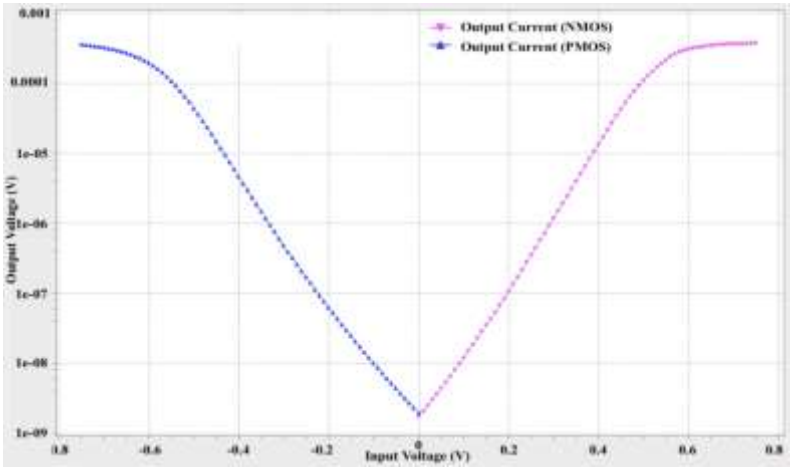

Figure 3. V-curve of proposed DGMOSFET.

Figure 3 shows the V-curve of PMOS and NMOS integrated in the single device. It is observed that the leakage current of both types of MOS are perfectly matched by suitable work function engineering. The leakage current is found to be $1x10^{-9}$A and ON Current are calculated to be 10^{-3}A. It is evident from the graph that NMOS exhibits larger ON current as compare to PMOS.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, January 2023

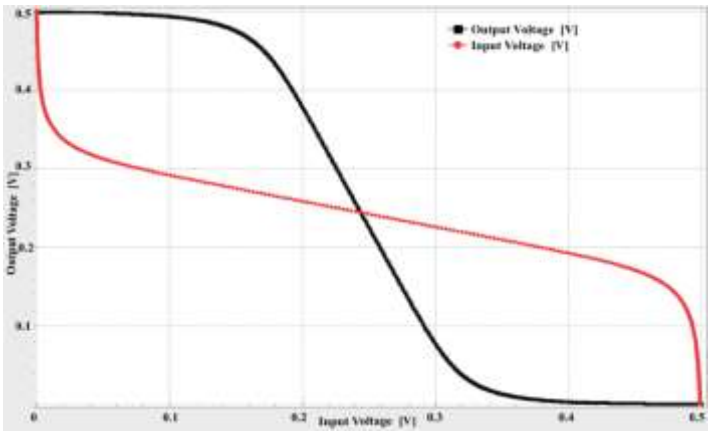

Figure 4. SNM of proposed inverter using DGMOSFET

Figure 4 shows the SNM of the proposed inverter using DGMOSFET which consist of NMOS and PMOS integrated in the single device. The graph shows the output characteristics along with the input voltage. Also, **figure 5** shows the transient curve of the proposed CMOS inverter made using the single device which has NMOS and PMOS integrated.

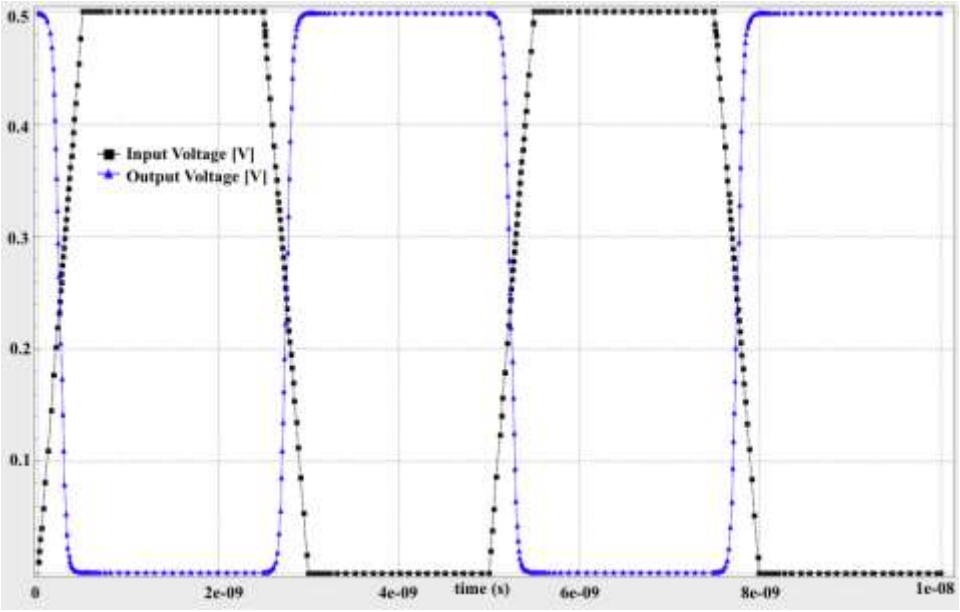

Figure 5. Transient curve of CMOS inverter designed as a single device DGMOSFET-I

Conclusions

A novel double gate MOSFET working as an inverter in a single device is proposed in this work. The proposed device works significantly for both p-type and n-type mode. This device reduces the junctions, wells, oxide regions in the device. This structure efficiently reduces the count of the transistors for designing the combinational circuits. The lower leakage current, lower subthreshold slope, lower DIBL, desired threshold voltage at lower channel length motivates the researcher to realize such device. The V-curve, SNM, VTC shows the potential of the device for being used as CMOS inverter.

REFERENCES

[1] Agostino F. D. and Quercia D., "Short Channel Effects in MOSFETs" pp.1–15, 11 December 2000.

[2] Chaudhry A. and M. J. Kumar, "Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review", *IEEE Transactions on Device and Materials Reliability*, vol. 4, issue 1, pp. 99-109, March 2004.

[3] X. Qian, W. Zheng, T. Yuan, "Analysis of Short-Channel Effects in Junctionless DG MOSFETs", *IEEE Trans. Electron Devices,* vol. 64, issue 8, pp. 3511–3514, 21 July 2017.

[4] Narula V. and Agarwal M., "Impact of core thickness and gate misalignment on rectangular core-shell based double gate junctionless field effect transistor", *Semicond. Sci. Technol.* Vol. 35, no. 3, 11 Febrary 2020.

[5] Fabio M. A., Antonio S., Marco B., Enrico Z., and Gaudenzio M., "Double control gate field-effect transistor for area efficient and cost effective applications.", *IEEE Electron Device Letters*, vol. 35, issue 11, pp.1073-1075, November 2014.

[6] Narula V. and Agarwal M., "Enhanced performance of double gate junctionless field effect transistor by employing rectangular core-shell architecture" Semicond. Sci. Technol, vol. 34, no. 10, 16 September 2019.

[7] Na, M. H.,Nowak E. J., Haensch W., and Cai. J., "The effective drive current in CMOS inverters" *in Digest. International Electron Devices Meeting*, pp. 121-124, san Francisco, USA, 08-11 December 2002.

[8] Semiconductor Device Simulator Version 1.7.2 Visual TCAD User's Guide .

[9] Loan, S. A., Kumar S., and Alamoud A. M., "A novel double gate metal source/drain Schottky MOSFET as an inverter", *Superlattices and Microstructures* , vol. 91, pp.78-89, march 2016.

[10] Suchismita D., Tewari S., Biswas A., and Mallik A., "Improved digital performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET in the nanometer regime", *Microelectronic Engineering*, vol. 211, pp.18-25, 15 April 2019.