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PARTIAL PRODUCT REDUCTION PROCESS BY INTEGRATING ADDITIONS AND ACCUMULATIONS INTO HIGH-PERFORMANCE MULTIPLY-ACCUMULATE UNIT

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ABSTRACT
This research suggests a pipelined Mac architecture with minimal power and fast performance. Carry propagation of ads has higher power consumption and longer route latency; to address this issue, we suggest a way. In this, we include a portion of additions into a procedure that only partially reduces the result. The PPR procedure of subsequent multiplication does not accomplish addition or accumulation of MSB bits. The total number of carries is meant to be accumulated by a small size adder in order to properly contrast with surplus in the PPR process. Using XilinxISE14.7, the efficacy of the suggested technique is calculated.
Keywords: MAC unit, dadda multiplier, Arithmetic circuits, alpha-bit adder

Introduction
In the proposed method we use two stage MAC unit with 8 and 16 bit. In Partial Product Generation (PPG) process, PPR performed in the first stage, in the second stage performs the $(k+\alpha)$-bit addition to produce the accumulation result. The main trademark of this proposed architecture is mentioned below: To reduce the lengths of carry propagations, we integrate a part of additions into the PPR process. To handle overflow in the PPR process, a α-bit adder is used to count the total number of carries. By applying the gating technique, the second stage can only be executed in the last cycle (of the entire sequence of multiply-accumulate operations) for power saving.

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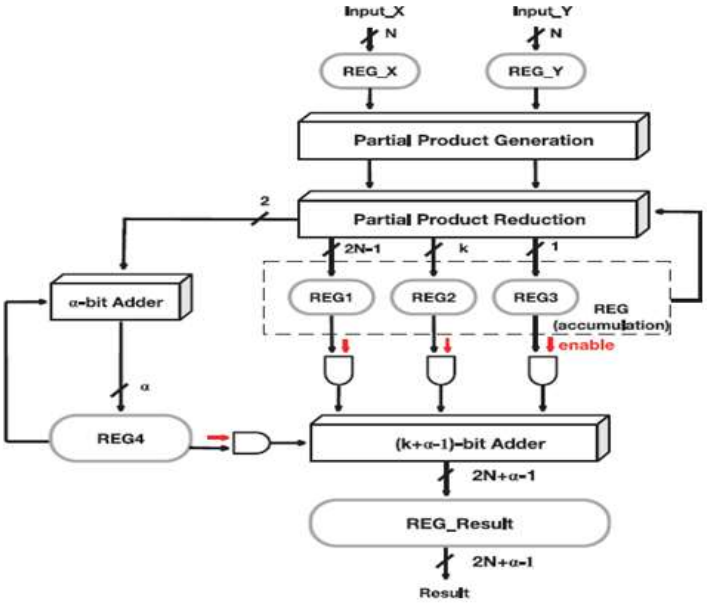

Fig.1. Architecture of Proposed MAC Unit

The proposed architecture of MAC shown in above figure. Our PPM (for the PPR process) is composed of two PPMs: one PPM is derived by the PPG and the other PPM is derived by the accumulation. In the first stage of proposed MAC, the final addition of higher significance bits is not performed. Register *accumulation* is used to store the PPM derived by the accumulation. Thus, register *accumulation* includes three parts: REG1 (i.e., the first row) has *2N-1* bits, REG2 (i.e., the second row) has *k* bits, which can define by the user, and REG3 (i.e., the third row) has *1* bit. In the PPR process, we adopt the Dadda tree approach to reduce our PPM to two rows. After our PPM is reduced to be two rows, we perform the *(2N-k-1)*-bit final addition. Since we use an *(2N-k-1)*-bit adder for the addition of the last two rows obtained by the Dadda tree approach, a larger *k* can have a smaller carry propagation in the *(2N-k-1)*-bit adder. However, since the final addition and accumulation of *k* higher significance bits are performed in the PPR process of the next multiplication, a larger *k* results in a larger PPM for the PPR process. In the second stage of the proposed MAC unit, we produce the accumulation result. The inputs of the second stage include register *accumulation* (consisting of REG1, REG2 and REG3) and register REG4. In the proposed MAC unit, the accumulation has been done in both the α-bit addition and the next PPR process. Thus, if we only need to obtain the final result in the last cycle, we can disable the $(k+\alpha)$-bit addition in other cycles for power saving.

Advantages

Low power consumption

Carry propagation is not considered in this method and hence delay will be reduced

Applications

DSP

Image processing

Audio Applications

Related Work

Two carry propagations—adds in multiplication and additions in accumulation—must be carried out in the

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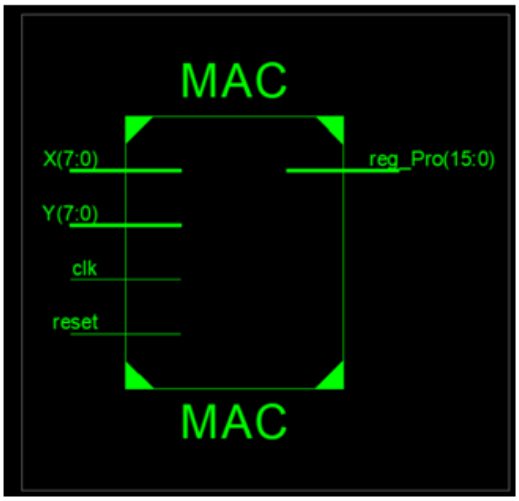
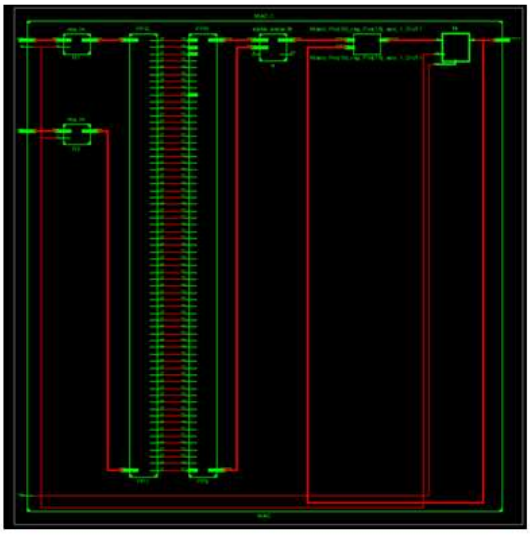
traditional MAC unit. The dada multiplier is used for multiplication in the MAC unit. The Dadda method varies from the Wallace method in that it only uses the bare minimum of full and half adders to achieve predefined stage heights. The stage height restrictions are as follows: #2, #3, #4, #6, #9, #13 #19 #28 #42 The size of each stage is 1.5 times that of the stage above it. The usage of complete adders, which take three partial products and turn them into two partial products, produces the 1.5 reduction ratio. Thus the maximum height of the succeeding stage is ⅔ that of the previous stage. In doing this, Dadda seeks to optimize the area of the multiplier by using the fewest number of adders to reach the CPA stage.

SIMULATION RESULTS

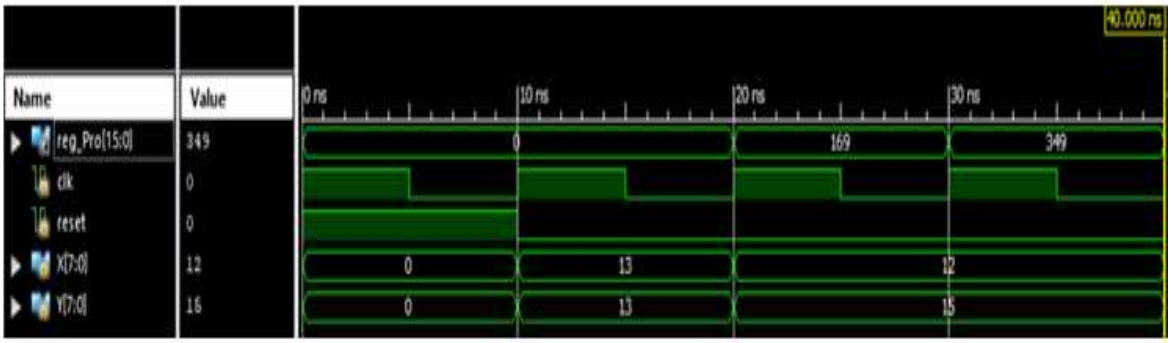
RTL



INTERNAL BLOCK DIAGRAM



SIMULATION RESULTS



CONCLUSION

We have seen different application of MAC unit for the various application. MAC unit designed with various multiplier among them Booth's multiplier is having highest operating speed and consumes less power. MAC unit is high in demand in Digital signal processing to provide the basic hardware for the systems. MAC unit is in use for all type of arithmetic operation such as addition multiplication, division, squares and square-root. MAC unit must be superior in terms ofarea, delay, power consumption, speed and complexit

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