

**POWER FACTOR CORRECTION TECHNIQUE ON NEW TOPOLOGY USING PFC BOOST CONVERTER****¹D.Subramaniyam, ²K.Rajkumar, ³P.Shoba, ⁴Shahed Ahmed Khan**^{1,2,3}Assistant Professor, ⁴UG Student, ^{1,2,3,4}Dept. of Electrical and Electronics Engineering, Visvesvaraya College of Engineering and Technology, Mangalpalle, Telangana, India.**ABSTRACT**

Investigated is the future of control methods for Power Factor Correction (PFC) converters. Review and analysis of the primary control strategies for absorbing sinusoidal input currents in boost PFCs. A few experimental findings for a PFC supported by the Sepic topology are described, allowing comparison of converter performance with various control strategies. Its generalization to other converter topologies is also considered. Last but not least, information about control ICs created expressly for Power Factor Correction applications is provided, along with certain considerations about dynamic operation.

Keywords: Power factor correction, control technique strategies

INTRODUCTION

There are various factors contributing to the increased focus on the quality of the currents that electronic equipment is absorbing from the service line. In reality, a low PF lowers the amount of power (ability) that is available from the utility grid, but a high (THD) harmonic distortion of the line current results in EMI issues and cross-interferences across other systems linked to the same grid via the line impedance. According to this viewpoint, the typical rectifier, which uses a diode bridge by a filter capacitor, performs inadequately. As a result, there are several efforts underway to create interface technologies that enhance the power factor of typical electronic loads.

An faultless power factor corrector (PFC) should emulate a resistor on the surplus side while maintaining a reasonably regulated output voltage [1]. In the case of sinusoidal line voltage, that implies that the converter must draw a sinusoidal current from the utility; so as to try and do that, a suitable sinusoidal reference is usually needed and therefore the authorized objective is to force the input current to follow, as close as possible, this current reference.

The most desired topology in PFC applications is certainly the boost topology, shown in Fig.1 together with a generic controller.

A diode rectifier effects the ac/dc conversion, while the controller operates the switch in such a way to properly shape the input current i_g in keeping with its reference. The output capacitor absorbs the input power pulsation, allowing a little ripple of the output voltage V_L .

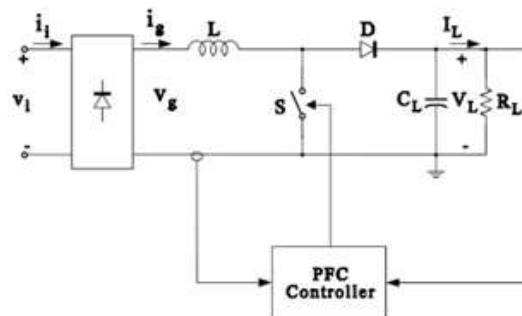


Fig 1- Principle scheme of PFC boost converter

The boost topology is incredibly simple and allows low-distorted input currents and nearer to unity power factor with different control techniques.

Moreover, the output capacitor is an efficient energy storage element (due to the high output value of voltage) and the ground-connected switch simplifies the drive circuit. The main disadvantages of this topology are:

- 1) start-up over currents, because of the charge of the massive output capacitor;
 - 2) lack of current limitation during overload and short circuit conditions, because of the direct link between line and load;
 - 3) difficult injection of a high-frequency transformer for insulating the input and output stages;
 - 4) output voltage always greater than peak or maximum input voltage.
- In spite of these limitations, many PFC's supported the boost topology have been proposed in the literature. Various control strategies have also been implemented.

In the following, the most popular control techniques are reviewed and compared, in order to focus on advantages and problems of each solution, also referring to the availability of commercial control IC's.

REVIEW OF PFC CONTROL TECHNIQUES

current reference amplitude. In this way, the reference signal is naturally synchronized and always proportional to the line voltage, which is the condition to obtain unity power factor.

As Fig.2 shows, the converter operates in Continuous Inductor Current Mode (CICM); that means that devices current stress also as input filter requirements are reduced. Moreover, with continuous input current, the diodes of the bridge will be slow devices (they operate at line frequency). On the another hand, the hard turn-off of the freewheeling diode increases losses and switching noise, calling for a fast device. Advantages and disadvantages of the solution are summarized hereafter.

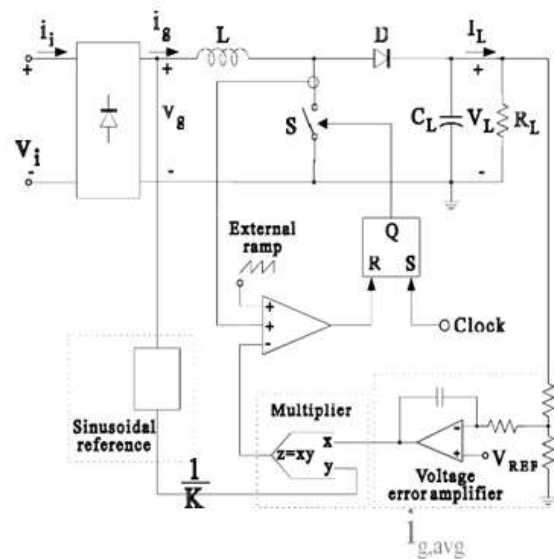


Fig.2 - Peak current control scheme

In the following, we will check with the boost PFC, even if many of the discussed control techniques can even be used with other topologies.

Peak current control

The basic schematic of the peak current controller is shown in Fig.2, along with a typical input current waveform [2-6]. As we could see, the switch is turned on a constant frequency by a clock signal, and is turned



off when the adding of the increasing positive ramp of the inductor current (i.e. the switch current) and an external ramp current (compensating ramp) reaches the sinusoidal current reference. This reference is usually obtained by multiplying a scaled exact copy of the rectified line voltage v_g times the output of the voltage error amplifier, which sets the

Advantages:

- constant switching frequency;
- only the switch current must be sensed and can be accomplished by a current transformer, thus avoiding the losses due to the sensing resistor;
- no need of current error amplifier and no need of its compensating network;
- possibility of a true switching current limiting.

Disadvantages:

- existence of sub harmonic oscillations at finite duty cycles greater than 50%, so a compensating ramp is needed;
- input current distortion which increases at maximum line voltages and light load and is damaged by the presence of the compensation ramp control was more sensitive to commutation noises.

The input current distortion are often reduced by changing the present reference wave shape, for instance introducing a dc offset, and/or by introducing a soft clamp. It's shown that even with constant current reference, good input current wave forms are often achieved. Moreover, if the PFC is not calculated for universal input operation, the duty-cycle can be kept below 50% so ignoring also the compensation ramp.

obtainable commercial integrated circuits IC's for the peak current control are the ML4812 (Micro Linear) [3] and TK84812 (Toko).

Average current control

This is another control method, which allows a much better input current wave forms, is that the average current control represented in Fig.3 [4,7-10]. Here the inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator. In this way the inner current loop used to reduce the error between the typical input current i_g and its reference. This later is obtained within the same way as within the peak current control.

The converter works in (CICM), therefore the same assumptions through with respect to the maximum current control are often applied.

Advantages:

- constant switching frequency;
- no need of compensation ramp;
- control is less delicate to commutation noises, due to current filtering;
- better input current waveforms than for the maximum current control since, near the zero crossing of the line voltage, the duty cycle is close to one, so reducing the dead angle in the input current [4] a current error amplifier is needed and its compensation network design must take into account the different converter operating points during the line cycle.

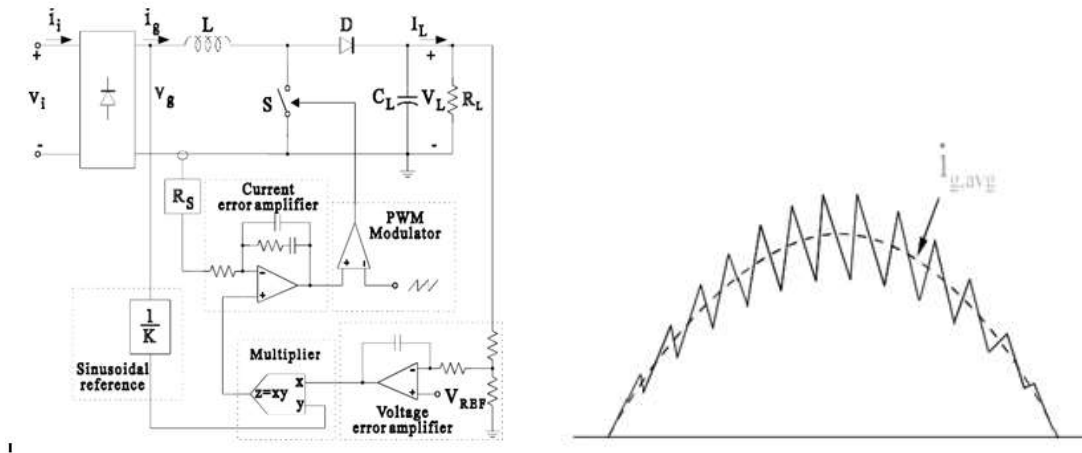


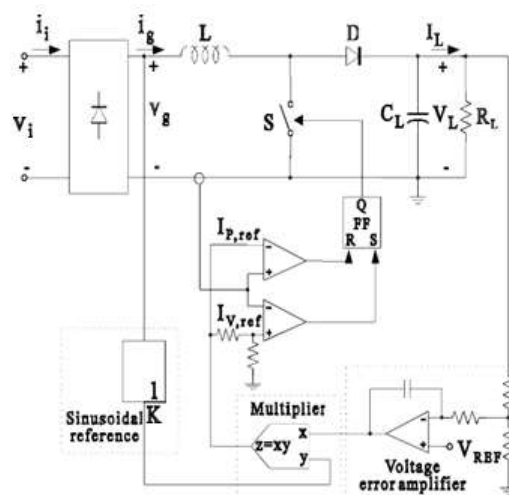
Fig.3 - Average current control scheme

This control technique is becoming very popular and detailed design criteria can be found in [4,7,8,10]. Many control IC's are available from different manufacturers: UC1854/A/B family (Unitrode) [7,10,12], UC1855 (Unitrode) [11], TK3854A (Tokyo), ML4821 (Micro Linear), TDA4815, TDA4819 (Siemens), TA8310 (Toshiba), L4981A/B (SGS-Thomson) [13], LT1248 [14]

Hysteresis control

Fig.4 shows this kind of control within which two sinusoidal currents taken as $I_{P,ref}$, $I_{V,ref}$ are given rise to, one for the maximum and therefore the other for the valley of the inductor current. From this control technique strategy, the switch is on, when the inductor current goes down the lower of the reference current $I_{V,ref}$ and the switch is turned off when the inductor current goes above the upper of the reference $I_{P,ref}$, giving rise to a variable frequency control [16-18].

Also with this control technique, the converter will work in CICM.



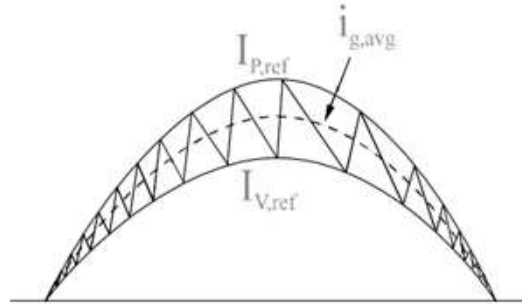


Fig.4 - Hysteresis control scheme

Advantages:

- no need of compensation ramp;
- low distorted input current waveforms.

Disadvantages:

- variable switching frequency;
- inductor current must be sensed;
- control sensitive to commutation noises.

In order to avoid unwanted switching frequency, the switch will be kept open near the zero crossing of the line voltage so introducing dead times within the line current. An analysis of the power factor as a function of those dead times are often found in [16,17]. A control integrated circuit IC which implements this control technique is that the CS3810 (Cherry Semiconductor) [19].

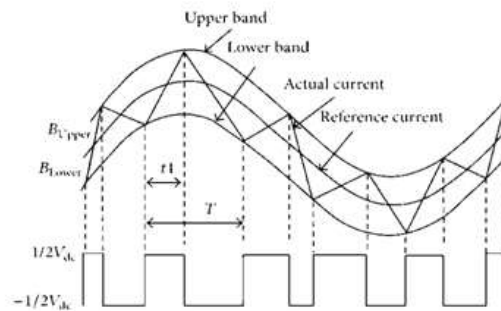
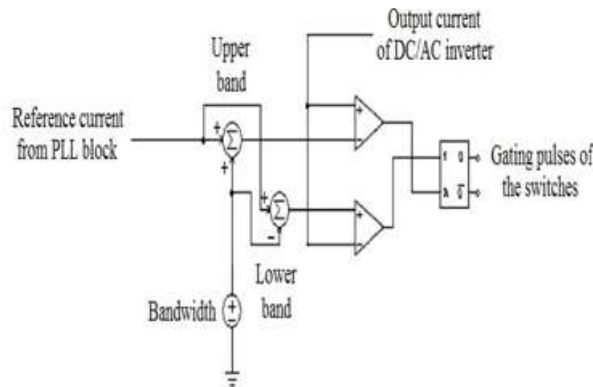


Fig 5 Pulse depending upon the actual current waveform



.Fig.6 Hysteresis band

The control scheme adopted in this proposed technique is very simple and can be practically implemented easily. Fig 6.8 shows the block diagram representation of the adopted control scheme v_0^* is the reference voltage that is expected at the out of the boost converter & v_0 is the actual output of the boost converter. The error in the output voltage is given to the voltage controller.

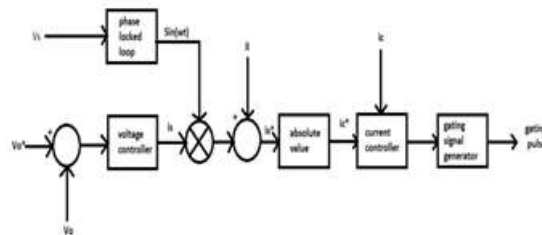


Fig.7 Adapted control scheme for the proposed powerfactor correction technique

The voltage controller (P controller) processes the error signal and produces appropriate current signal (i_s). The current signal (i_s) is multiplied with unit sinusoidal template which is produced by using phase locked loop (PLL) to supply $i_s \sin \omega t$. The load current i_l subtracted from the $i_s \sin \omega t$ to produce the reference current signal i_s^* . As the boost inductor current can't be alternating, the absolute circuit gives the absolute value of the reference current signal i_s^* that is i_c^* . The actual signal (i_c) and the required reference signal (i_c^*) are given to the current controller to produce the proper gating signal. The current controller adopted may be a hysteresis current controller. Upper and lower hysteresis band is created by adding and subtracting a band “h” with the reference signal i_c^* respectively shown in the Fig 6 & 7. The inductor current is forced to fall within the hysteresis band. When the current goes above the upper hysteresis band i.e., i_c^*+h , the given gate pulse is removed resulting the current forced to fall with the current will flow through the load. When the current goes below the lower hysteresis band i.e., i_c^*-h , the pulse is given to the switch, that the current increases linearly. In this way the switching of the power switch can be done to track the reference current command & the resultant current drawn by both the loads will be nearly sinusoidal with low harmonic content and low total harmonic distortion (THD); hence the power factor of the supply availability are often improved

SIMULATION RESULT

The proposed power factor correction technique is simulated by using MATLAB software and the results

obtained are shown below. The values taken in the simulation circuit are given in the below table. The different results are shown & explained briefly.

TABLE 1: PARAMETER VALUE TAKEN FOR SIMULATION

SL.NO.	NAME	VALUE
1.	Supply voltage	230V,50HZ
2.	Source Impedance	0.1mH
3.	Boost Inductor	2mH
4.	Output of boost converter	300V
5.	Non-linear load	20mH,500 Ω, 100μF
6.	Boost converter	470μF, 100 Ω, 10mH
7.	Hysteresis band	0.05

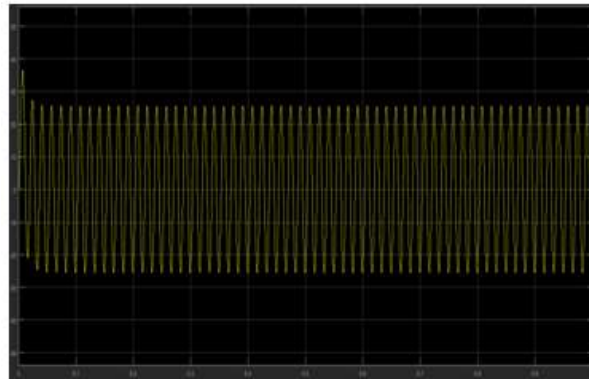


Fig 8.1 Without PFC boost converter input current wave

Fig. 8.1 shows different wave forms of the system feeding to a non-linear load. As the capacitor is disconnected in the load side to hold the DC output voltage, when the instantaneous value of the supply voltage is more than DC output voltage current will be supplied by the source. So the current is pulsating type which is shown in the Fig.8.1. Generally this pulsating type current contains large amount of harmonics, mainly dominant lower order harmonics which when enters into the system results damage to the other loads connected at point of common coupling (PCC). Fast Fourier transform(FFT) analysis of the supply current is given in the Fig. 8.2 As the harmonic content is very high in the supply current, the total harmonic distortion of the supply current is 242% & the power factor of the system is very poor & of the order of 0.38 lagging.

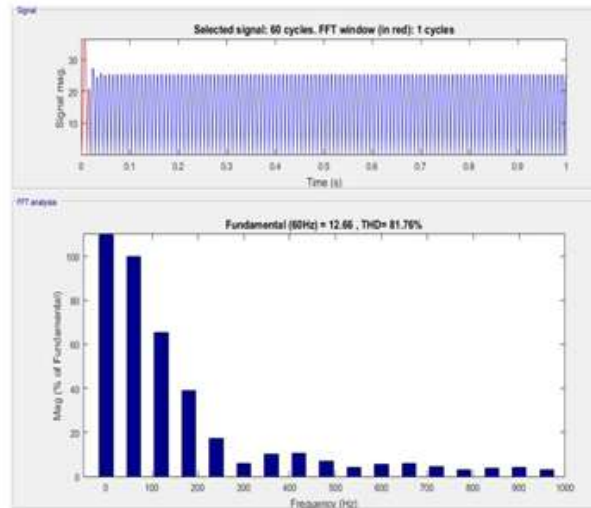


Fig 8.2 FFT analysis of input current wavewithout PFC boost converter

Fig.9 shows different waveforms of the system after compensation using PFC boost converter. As we know, the more harmonics content in the supply current increases the total harmonic distortion (THD) the system THD=81.76% hence the overall power factor of the system decreases. This harmonic current should be removed at the point of generation. So to remove the harmonic current generated by the non-linear load, a PFC boost converter is connected in shunt with the non-linear load & the compensating current is shaped in such a way that the total current drawn by the total arrangement becomes sinusoidal.

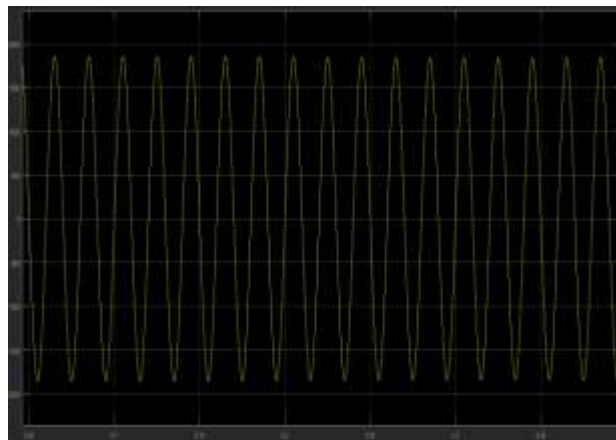


Fig9.1With PFC boost converterinput current waveform

The source feels the total arrangement to be resistive load and supply nearly sinusoidal current with nearly unity power factor. The current drawn by the non-linear load is shown in Fig.8.1 and the compensating current waveform is 9.1 Shown in the Fig.9.1 resulting supply current to be nearly sinusoidal. Using FFT analysis, we can see the harmonic content in the supply current with proposed technique is almost neglected. The lower order harmonics content in the load current almost removed and only fundamental current drawn from the supply shown in Fig.9.2, resulting THD=25.01%.

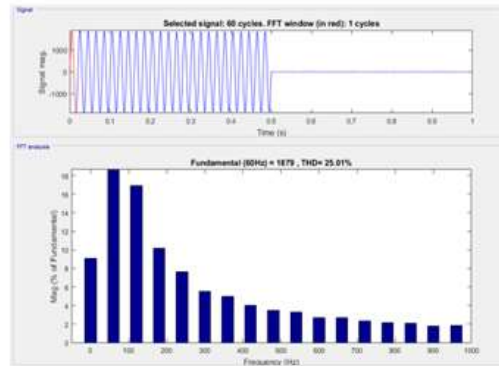
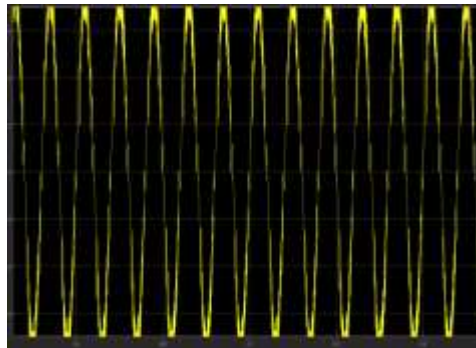


Fig 9.2 FFT analysis of input current waveform with PFC boost converter



Sl.	Parameter	With out PFC	With PFC	Non-linear and PFC
1.	THD	81.76%	25.01%	25.01 %
2.	POWER FACTOR	0.3	0.989	0.989
3.	CURRENT SHAPE	Pulsating	Pulsating	Nearly Sinusoidal

Fig 10.1 Non-linear load with PFC boostconverter input current waveform

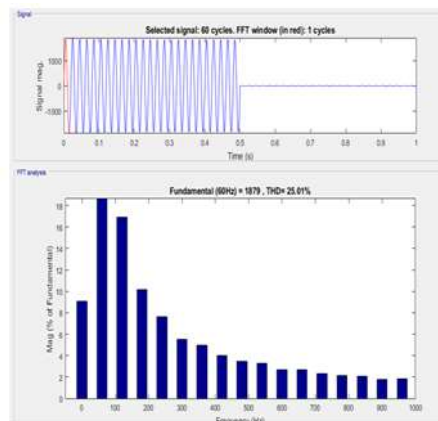


Fig 8.6 FFT analysis of input current wave of non-linear load and PFC boost converter

The fig 10.1 shows the input current waveforms of PFC boost converter with Non linear load and the FFT analysis of that type of load was shown in fig 10.2. Here, we observe the THD reduces to 25.01% . The comparison table was drawn below with the values of THD, Power factor and Current shaping for the circuits of without PFC, with PFC and with both PFC and non-linear load

CONCLUSION

This paper has presented one new and Interesting AC/DC boost converter for PFC applications. Without using any dedicated converter, one converter can be used to climate the harmonics current generated by the other non-linear load, with the help of simulation study, it can be included that, this configuration removes almost all lower order harmonics hence with this configuration we can achieve power factor nearer to unity, THD less than 5% however, this technique can be limited to application where the non-linear load current is less and fixed. besides the literature review has been developed to explore a perspective of various configuration offer power factor correction techniques.

FUTURE SCOPE

For this work the Boost PFC Converter with different controllers are realized with the help of MATLAB/Simulation, which can be analyzed in real time simulator for the consideration of practical applications. Also, the hardware implementation can be realized practically with suitable control technique. The switching losses can be considered and suitable soft switching technique can be introduced. Some special suitable optimization technique can be employed to ensure the very high dynamic stability and very wide stable operating range.

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