Industrial Engineering Journal
ISSN: 0970-2555
Volume : 51, Issue 8, August : 2022

PARITY-PRESERVING GATES IS MODELLED USING VERILOG HDL AND STIMULATED IN XILINX SOFTWARE FOR PERFORMING ALU OPERATIONS

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ABSTRACT
With the development of MOSFETs in the 1960s, the semiconductor industry has seen great improvements in terms of speed and device performance owing to device scaling, but power dissipation has also been a significant issue. Researchers are looking for a game-changing technology since gadget scaling has hit its limit. Reversible computing is one of the VLSI industry's growing topics. This technology's zero power dissipation in reversible logic circuits has drawn the attention of researchers in major part. Here, research into creating an ALU with reversible quantum gates is being suggested. The suggested ALU may detect a single bit error in addition to performing both arithmetic and logical operations, which can be chosen depending on the situation. The design uses Fredkin and CNOT gate, which are parity preserving gates. The proposed design is modelled using Verilog HDL and stimulated in Xilinx software. The Design is focused on reducing the amount of gates, quantum cost, garbage outputs and ancillary inputs or constants inputs.

INTRODUCTION

Reversible circuit synthesis has recently become more and more important, offering alternatives to traditional Boolean networks. Two significant findings served as the impetus for reversible computing. Such circuits have two advantages over conventional circuits: first, they consume less energy, and second, they are intimately related to a number of cutting-edge technologies like quantum circuits. In 1961, Landauer demonstrated that irreversible circuits always use power and release heat at a minimum rate of kTln2 for any little amount of information erasure, where k is the Boltzmann constant and T denotes temperature. Later, Bennett showed that in theory, arbitrarily small or zero energy dissipation is merely possible if no information is lost during computation. This is good for reversible circuits as input and output data is processed without losing any of the original information. Though the fraction of the facility consumption in current VLSI circuits due to information loss is negligible, this is often expected to vary as increasing packing 2 densities force the facility consumption per gate operation to decrease, making reversible computation a beautiful alternative. Studying the reversible circuits enriches our knowledge of quantum computation, as reversibility is an integrated part. Additionally, the applications of reversible circuits are found in low power CMOS designs, adiabatic circuits, cryptography, optical computing and digital signalprocessing.

EXISTING METHOD AND PROPOSEDMETHOD

EXISTING METHOD

In computing, an arithmetic and logic unit may be a combinational digital circuit that performs arithmetic and logical operations. An ALU consists of Adder, Subtractor, Multiplexer, Demultiplexers, Shift registers etc. and are designed with MOSFET transistors. The MOSFET transistors utilized in digital circuits, which uses irreversible logic gates. And it's certain limitations like more power dissipation, spaceconsumption, propagation delay.

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PROPOSED METHOD

In proposed method, a 4-bit ALU architecture is designed using parity preserving gates. Reversible computing does not allow for any bit loss of information, thus power dissipation is either zero or negligible. Here we can detect faults by parity checking in reversible gates. Here Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the Modelsim logic simulator is used for system-level testing. The design has improvements in all the metrics considered for evaluation in compared with the existing designs of ALU.

REVERSIBLE CIRCUITS

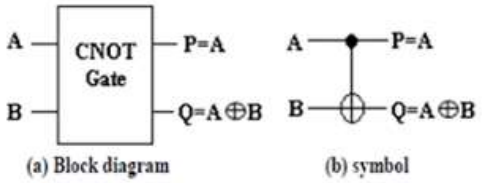
Reversible circuits are studied extensively to seek out an alternate solution to classical design. Some unique properties of reversible logic are identified to facilitate the synthesis and testing of circuits and in particular their applications in several arena of computation. The quantum realizations of reversible gates are exercised to relate reversible logic to quantum circuits.

REVERSIBLE FUNCTION

An nxn reversible circuit realizes an n-input/n-output function where each input vector maps bijectively to a singular output vector. The reversible circuits allow no fan-out and no feedback path.

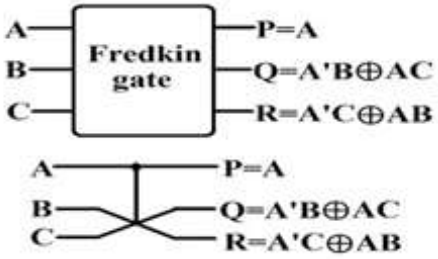
Irreversible functions differ from their reversible counterpart in two aspects. First, the number of inputs and outputs are not equal. A reversible gate is an N-input N-output logic device that gives one to at least one mapping between the input and therefore the output. It not only helps us to work out the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Reversible logic gates also are called as parity preserving gates. The parity preserving reversible logic gates are a category of reversible logic gates with the extra property that the parity of the input is same because the parity of the output. A reversible gate are going to be parity preserving if the EXOR of the inputs matches the EX-OR of the outputs.

The gates used in this project are CNOT GATE- The controlled NOT gate is a quantum logic gate. The another name of CNOT gate is Feynmann gate.This is 2x2 matrix of inputs and outputs. One output is same as the input and the another output is xor operation of inputs. The CNOT gate is shown in below fig(1).



Fig(1): CNOT Gate

FREDKIN GATE- A Fredkin gate has 3 inputs and gives 3 outputs. The output is a combination of multiple logics like and, or and xor. This gate is used to implement various other digital logics which is otherwise not possible with CNOT gate. Its quantum cost of five which is high. Fig(2) shows the logic function implemented by Fredkin gate.



Fig(2): Fredkin Gate

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REVERSIBLE ARITHMETIC AND LOGIC UNIT

An arithmetic logic unit is a multi-functional circuit that performs one of several possible functions on two operands Aand B depending on control inputs.

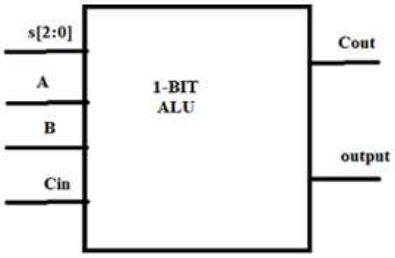
Instead of constructing several single-function circuits this module offers programmability with less gate cost. However, the combination of several functions into a single unit requires additional control lines and circuit resources.

In this thesis, we implement a reversible ALU having operations of a conventional irreversible ALU. For the ALU design we need to concentrate on including as many arithmetic and logic operations as possible in a simple design with maximum efficiency and minimum possible cost.

Hence, the reversible ALU presented here includes most operations available in conventional irreversible ALU.

1-BIT ARITHMETIC AND LOGIC UNIT

The schematic diagram of single-bit RALU is shown inbelow figure.



Fig(4.1): 1-bit ALU

The below Fig.(4.2) shows the architecture of single-bit Reversible Arithmetic and Logical unit using CNOT and Fredkin gates. And Table 4.3 shows the reality table of Fig.4.2. A novel one bit ALU architecture is meant using parity preserving Fredkin and CNOT gates. Table-1 represents the reality table of the ALU design. S2 is that the control signal which selects either the arithmetic or logical output. As discussed earlier the Fredkin gate used has three inputs and sum. A number of outputs and also CNOT gate has two inputs and outputs. The fig(3.2) shows the architecture of the proposed ALU where top portion represents the arithmetic unit and therefore the bottom portion represents the logical unit. The 1s and 0s at the input sides of gates in figure 6 are the ancillary inputs and G represents the rubbish outputs. Also intermediate outputs are represented for understanding the intermediate operations of 1 bit ALU. The design uses Fredkin and CNOT gates. Fredkin gate 7 selects arithmetic or logical unit based on the selection signal. A and B are the inputs and S0, S1, S2 and Cin are the bits used to select the type of required operation. The design has a quantum cost of 44, the number of gates count is 16, the constant or ancillary inputs is 4 and thegarbage output obtained is 11. The design has hug improvement in all the metrics for evaluation in compared with the existing designs of ALU.

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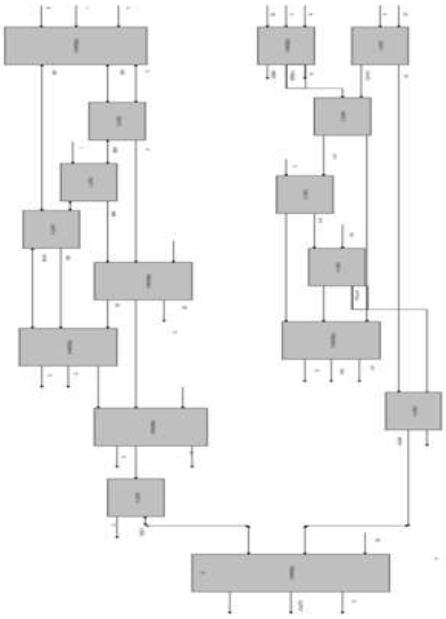
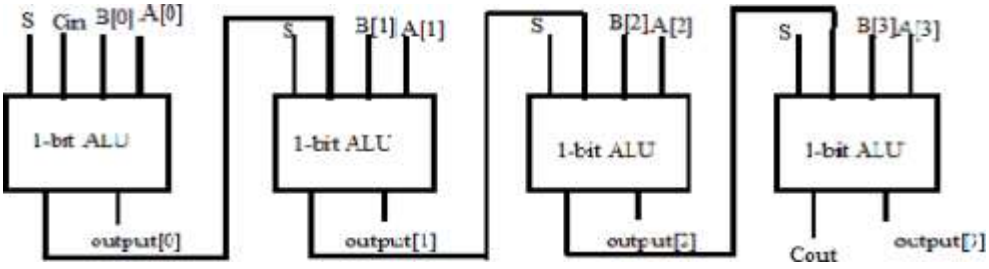
S2	S1	S0	Cin	Operation
0	0	0	0	A
0	0	0	1	A+1
0	0	1	0	A+B
0	0	1	1	A+B+1
0	1	0	0	A
0	1	0	1	A-1
0	1	1	0	A-B
0	1	1	1	A-B-1
1	0	0	0	A|B
1	0	0	1	~(A|B)
1	0	1	0	A&B
1	0	1	1	~(A&B)
1	1	0	0	~(A^B)
1	1	0	1	A^B
1	1	1	0	A
1	1	1	1	~A

Table(4.3): Truth table of 1-bit RALU



Fig(4.2): 1-Bit RALU Architecture



ADVANTAGES

- Duplication of input through output.
- Recovers bit-loss.
- Heat management.
- Energy dissipation is less.

- Power management.

Fig(4.4): Schematic of 4-bit RALU

- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.

Designing low power arithmetic and data path for

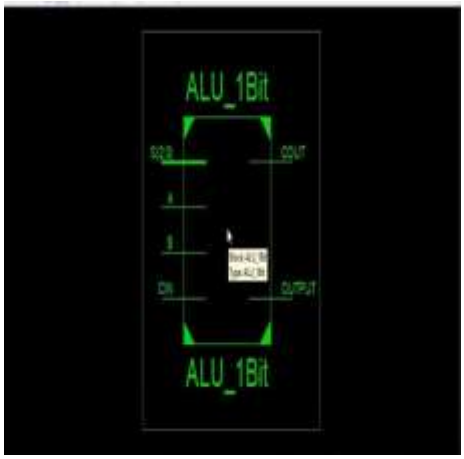
Multiple operations in a single cycle.

DISADVANTAGES

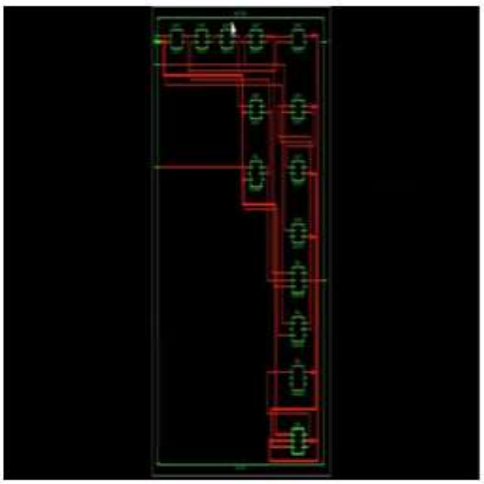
- However, in order to get the benefits of reversible computation, the reversible machine must actually be run backwards to attain its original state. If this step is not taken, then typically the machine becomes clogged up with digital heat, and is thus rendered unable to perform further useful work.
- We must make sure that our computation wasperformed with no errors otherwise chaos may result when the machine is run backwards.
- The synthesis of reversible circuits is restricted to 'Fan-out' and 'Feedback'.

RESULTS

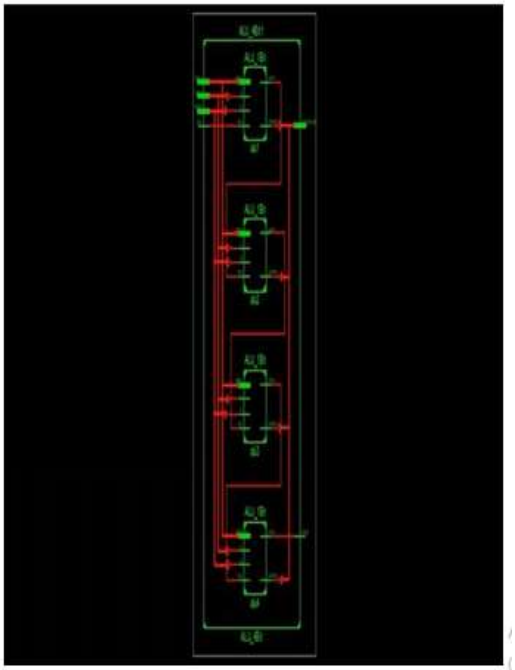
We validated the reversible functionality through simulation for the proposed design of reversible ALU (Fig. 6.3 design of reversible 4 bit ALU). Functional verification of the design is done using Verilog HDL with Xilinx Software. This provides an inference thatthe design has improved performance in all aspects ascompared to the existing design. The basic rule for the reversible logic is it must consists of same number ofinputs and outputs and this condition is satisfied. The improvement obtained is in constant inputs and garbage outputs. The ancillary inputs were decreased by 66.67% and the garbage outputs was also decreased by 31.25%.



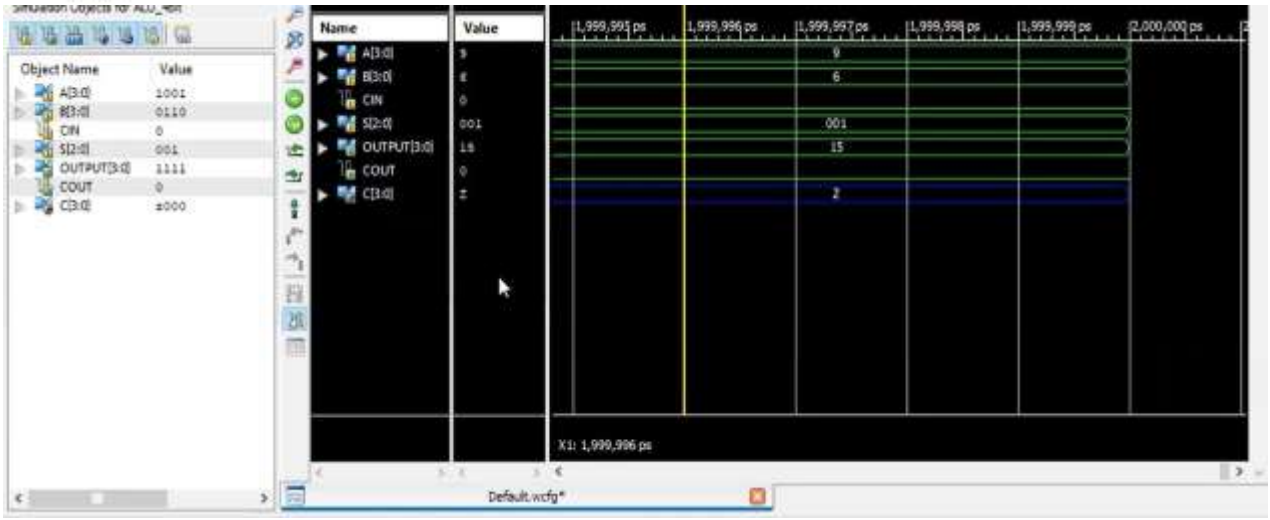
Fig(6.1): Schematic of reversible 1-bit ALU



Fig(6.2): Design of reversible 1-bit ALU



Fig(6.3): Design of reversible 4-bit ALU



Fig(6.4) Simulation of 4-bit ALU

The below Fig.6.4 illustrates the random simulation of a 4-bit RALU. The Output node shows that the according to the control signals. For each control combination we check to random inputs and outputs for example, for control S2S1S0=001 and inputs A=1001 and B=0100, the RALU performs an ADD operation hence the output becomes output=1111. Note that the garbage output are hidden in the display.

Conclusion

This paper has detailed the discussion on Reversible logicgates and therefore the three parameters which are ancillary inputs, garbage outputs, and quantum cost. Existing reversible gates are discussed along with parity preserving Fredkin and CNOT gates. The ALU was designed and implemented using Verilog HDL to verify its functionality in Xilinx. The performance was analyzed and improved efficiency was obtained. This design can be further extended to design multiple bit ALUs with parallel computation.

Future Scope

This can be extended further in the development of advanced work of digital design. The forthcoming computer chips are limited by Moore's law, hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor which is capable of ultra-high speed and infinitesimally low power computing.

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