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A UART SERIAL COMMUNICATION MODULE IMPLEMENTATION ANALYSIS USING VHDL AS THE DESIGN LANGUAGE

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ABSTRACT
UART, or "Universal Asynchronous Receiver Transmitter," is a serial communication protocol that is frequently utilized for low-latency, low-bandwidth, and affordable data transmission among a computer and its peripherals. On occasion, we can get away with implementing the bare minimum of UART's capabilities when it comes to actual production. The baud rate generator, receiver, and transmitter are UART's three key parts. The UART built in verilog can be used with an FPGA for small, dependable data transfer. This is really important for SOC layout. The simulation's outcomes match the UART protocol exactly. A receiver/transmitter (UART) interface is used by a number of electrical devices. UARTs are now frequently built into microcontrollers. A microprocessor known as a UART (Universal Asynchronous Receiver/Transmitter) controls the interface between a computer and its associated serial peripherals. The computer has an RS-232C Data Terminal Equipment (DTE) program so it can "speak" to modems and other serial devices. Modems and other devices that connect with one another outside of a network using serial transmission. Using the Universal Asynchronous Receiver/Transmitter (UART), each bit in a byte is transmitted one at a time. The bits are assembled back into bytes at the receiving end using a second UART. The main method for converting serial data to parallel data is the incorporation of each UART.Digital information (bits) is delivered through a single cable as opposed to multiple lines, which results in a huge cost savings when compared to parallel transmission.

1. INTRODUCTION
More than 90% of the available space is already taken up by System-on-a-Chip (SoC) integrated memory, and by 2014, this percentage is predicted to reach 94%. Therefore, embedded memory will outperform SoCs in terms of performance and yield. Random oxide pinholes, random leakage flaws, obvious assembly as well as processing faulting, particular processing problems, misalignment, obvious photo flaws, different defects and imperfections significantly lower memory manufacturing yield. Numerous redundancy techniques [3-6] have been developed as to increment the production and dependability of embedded memory. The data storage array has redundant rows and columns. Redundant rows and columns are advantageous for word-oriented memory cores because they guard against data loss in the event of a power outage.All of these redundancy strategies' space and complexity costs need to be taken into consideration in embedded memory architectures. The compiler is utilized to assemble SRAM for multiple purposes; hence, the BISR should not change any of the different faculty in SRAM. To calculate this difficulty, we present a novel redundancy method. It is possible to select some common words that are already present in the embedded memory to use as redundancy rather than adding new words, rows, columns, or blocks. A memory test is essential in front turning to redundance

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in fixing. The addition of additional circuits utilizing the 1970-proposed Design for Test (DFT) methodologies improves the test ability. A BIST circuit can control a DFT circuit more quickly and effectively than an external tester (ATE). On the other hand, Memory BIST only handles the screening of manufactured components and not the loss of parts as a result of manufacturing issues. The main objectives of BISR approaches are embedded-memory testing, fault-address saving, and redundancy installation. The authors of this paper describe a novel memory BISR method based on two steps of serial redundancy analysis (RA). The BISR circuit and an effective repair method for embedded memory with numerous redundancies are introduced in this paper. The previous BISR techniques have all been successful at fixing memory, but none of them have demonstrated how to stop a fault address from being saved more than once..

1.1 BUILT-IN-SELF-TEST

The testing module for the circuit is internally located in Built-In Self-Test. Consequently, Built-In Self-Test (BIST) is described as a mechanism that enables a machine to test itself. "Built-in self-testing," often known as BIST, is a technique for adding hardware and software capabilities to integrated circuits in order to reduce the requirement for automated test equipment. By employing their own circuits (ATE), the circuits can test their own functionality (functionally, parametrically, or both). BIST is regarded as a Design-For-Testability (DFT) method since it streamlines and expedites a chip's electrical testing. Practically any electronic circuit can use the BIST principle.

1.2 BIST schematic

The schematic of BIST is shown in below:

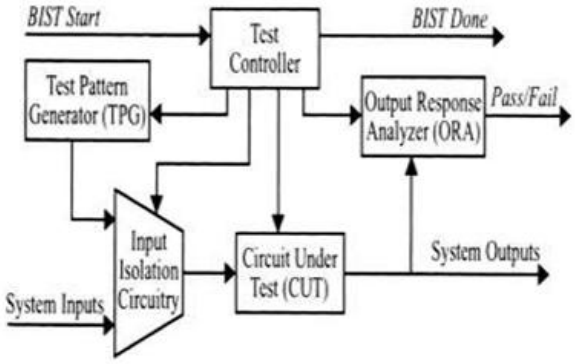

Fig.1. 1BIST schematic basic diagram

A DFT method called built-in self-testing (BIST) uses the system's resources to validate code. Performance considerably improves because testing is included into the hardware. The BIST schematic is illustrated in Figure 1, which calls for three additional pattern maker An analysis tool for responses and a test regulator for a digital circuit.

As a structure generator (LFSR), you utilize a counter, a linear feedback shift register, or a read-only memory (ROM) with pre-stored patterns. The phrase "response analyzer" refers to a compactor that keeps responses or an LFSR that could be used to examine a signature. All of the building blocks are activated by a signal from a controller. There are substantial drawbacks when linear feedback shift register [LFSR] architecture is used, as it is with BIST. The electrical device pioneer more switching activity into the CUT than would typically happen during testing. The end effect is excessive power dissipation and the resulting design time penalty.

1.3 BUILT-IN-SELF-REPAIR FOR MEMORY

Built-In Self Test (BIST) is a promising and practical method for testing VLSI systems and devices.

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BIST offers a number of advantages, such as the capacity to do high-velocity testing, extremely high fault coverage, the absence of the requirement for manual test development, and a reduced reliance on pricey third-party testing infrastructure for the application and monitoring of test patterns. Because of this, BIST lowers testing costs. BIST techniques come in two flavours: offline and online. An offline BIST architecture can attempt in either natural status or test mode. Regular procedure does not include the BIST circuitry. The Test Generator (TG) supplies inputs to the circuit under test (CUT), and the Response Verifier (RV) records the outputs. After testing is finished, the consequence verifier's contents are tested to determine the CUT status. Off-line testing methods are unable to find temporary flaws since they need continuous monitoring of the CUT outputs. Regular CUT operations must be suspended while an offline BIST is being executed. Therefore, if the CUT is essential to the circuit's functionality, the circuit's overall performance will suffer. It has been proposed that concurrent BIST techniques for input vector monitoring, which take advantage of input vectors coming at the CUT's inputs during normal operation, can reduce this performance reduction.

1.4 Logic Built In Self Test (LBIST)

In a conventional LBIST, linear feedback shift registers (LFSRs) are used to create pseudo-random test designs that are used on the test circuit. The circuit's condensed reaction in response to such patterns is then obtained using multiple input signature registers (MISRs). An erroneous MISR yield can be used to identify a broken circuit. There are many ways to supplement pseudorandom test patterns. Traditional LBIST has the drawback of needing thousands of pseudorandom patterns to be practical in ordering to achieve sufficient fault coverage. This shows that the amount of time needed to run tests for some programmes may be excessive. The standard procedure for testing an IC involves inserting it into an ATE, which will then be used to generate test stimuli and assess the performance. This technique cannot be used when soldering the IC to the finished product board because all pins are being utilised. Reducing the number of pins necessary for testing an integrated circuit (IC) after it has been soldered onto a board for a finished product is one possibility. To do this, additional logic for circuit verification may be programmed into the IC. Logic BIST (LBIST) is the method's main concept., which isa self test mechanism for digital circuits, asshownin Figure.

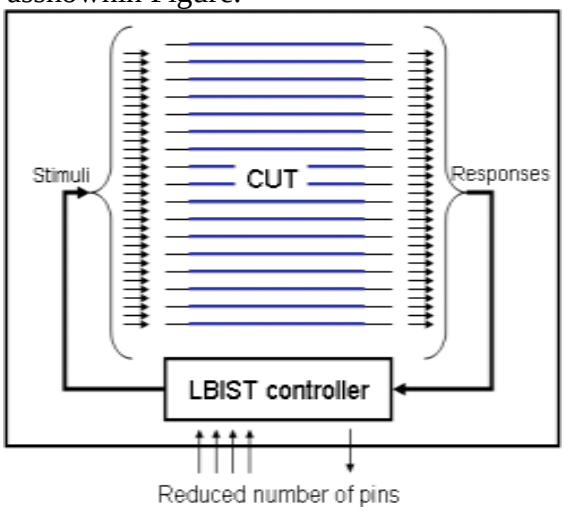

Fig.2.General LBIST scheme

The most often used LBIST design is the STUMPS architecture, which is depicted in Figure. To produce inputs for the internal scan chain of the device, It employs a pseudo-random patterns power generation system/linear feedback shift register (PRPG/LFSR) to start a functional cycles to record the device's answer and then condense the recorded reaction into a MISR. Any modifications to the MISR's

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test signature reveal a hardware issue with the gadget.

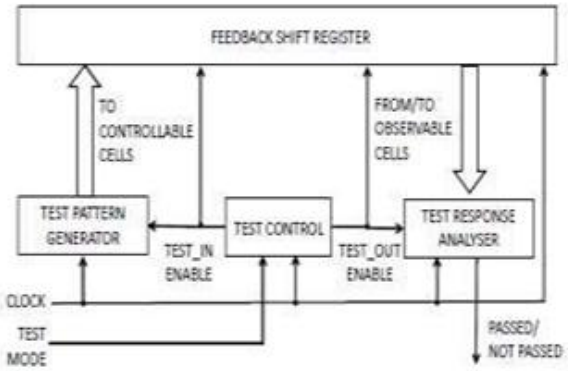

Fig.3. illustrating presented technique

The technique utilized in this work offers a straightforward mechanism for creating and tracking individual flip-flops, much like the old scan architecture. Flip-flops are linked together but not in scan, but rather in scan chains. Rather, we add the following modifications to the original FSR so as to facilitate the test mode:

1) As illustrated in Fig. 3.3, we multiplex the input for every programmable cell (b), where the active input of the multiplexer is the original flip-flop's (MUX) input. The test input of the MUX is connected to the test patterns (TPG) so as to construct test patterns.

We replicate the outcomes from to each one visible cell (c), as seen in Fig. 3.3. By means of a switch, the replicated signal is sent to the Test Responding Analyzer (TRA). The flip-flops' multiplexed outputs, referred to as outputs when testing mode is active, serve as inputs for the combinational logic. In combinational logic, flip-flops having switches on the output function as outputs. This enhances the ability to control and see the system being tested, much like a scan design, and enables sequential logic to be evaluated similarly to combinational logic.

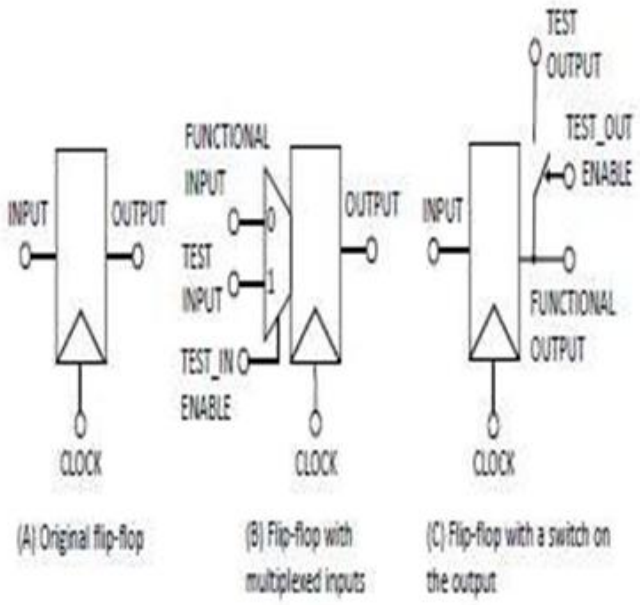

Fig.4. Alterations of FSR flip-flops to support test mode.

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2. RESULTS

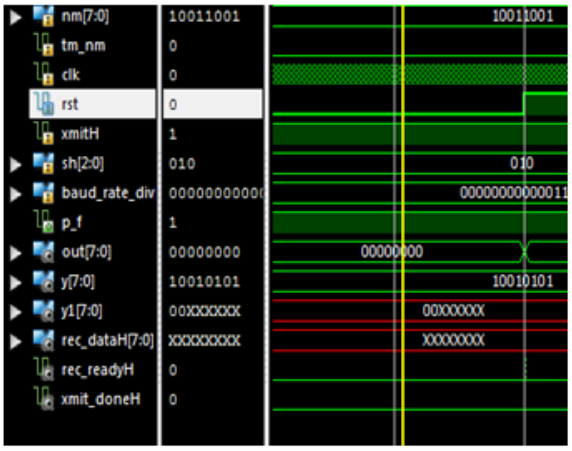


Fig.5. Representation Consequence for top module(rst=0,tm_nm=0)

If we initialise the circuit with rst=0, it will run in normal mode and do nothing (the output will rely on the user's input). Because CUT forbids us from seeing anything else, if we set rst=1, we won't see any output and will only see xxxx. Set baud div to 4'h000f to have output in CUT start when the baud rate reaches 9,600 bits per second.

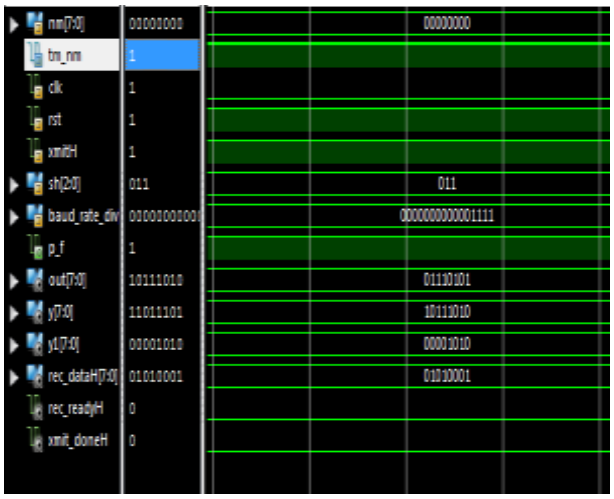
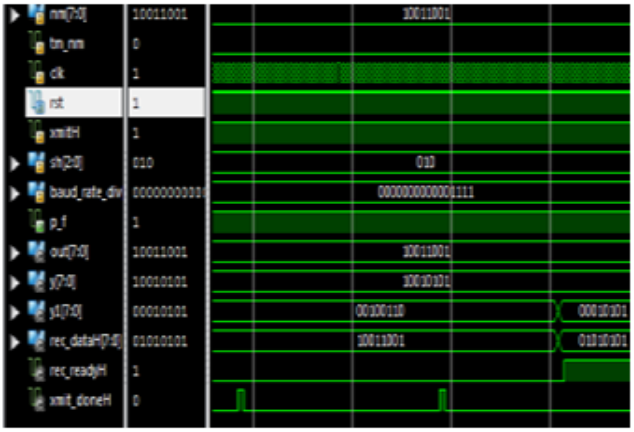


Fig.6. Representation Consequence for top module (rst=1,tm_nm=1)



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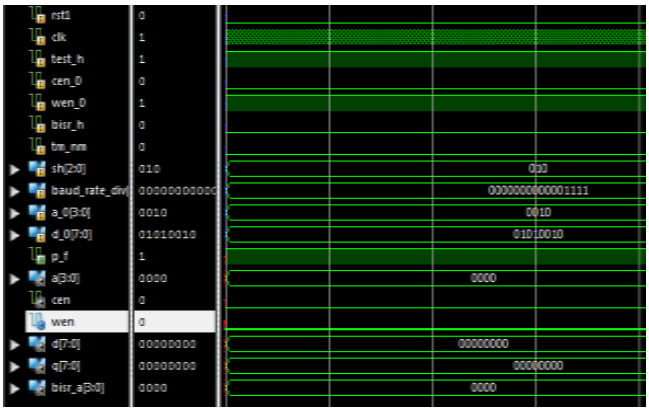

Fig.7: Representation Consequence for BISRrst=0(rd=0,wr=1)

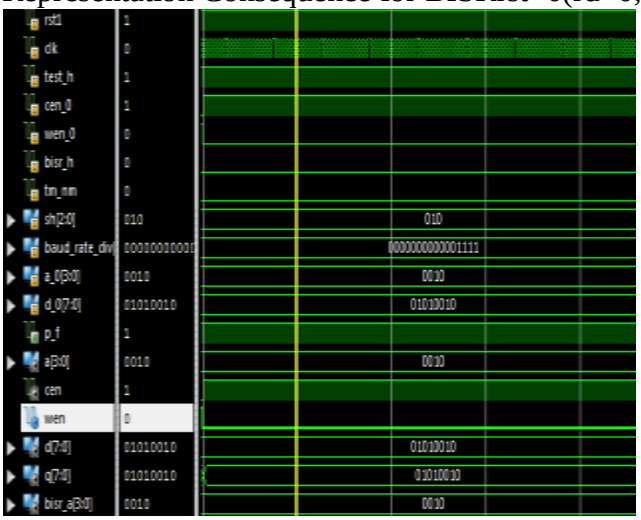

Fig .8: Representation Consequence for BISRrst=1(rd=1,wr=0)

CONCLUSION

The UART components are implemented in this architecture using VHDL as a design language. Simulations and validation have been carried out utilizing Quartus II software and an Altera Cyclone series FPGA chip EP2C5F256C6. The findings are trustworthy and credible. The comprehensive, highly adaptable, and useful as a reference design. The field of electronic design will be significantly impacted by this design, especially since SOC technologies is at an emerging maturity level.

REFERENCES

1. Towit: Semiconductor Industry Association," International technology road map for semiconductors (ITRS),2003edition,"Hsinchu,Taiwan,December 2003.
2. IBMJournalofResearchandDevelopment,Volume24,Issue3,Pages398-409, May 1980, C. Stapper, A. Mclaren, and M.Dreckman,"Yield model for Productivity Optimization of VLSI Memory Chips with redundancy and Partially excellent Product."
3. IEEE Transactions on Computer-Aided Design, volume 9, issue 3, pages 323-328,March1990,W.K.Huang,Y.H.shen,and F. lombrardi, "New methodologies for repairsof memory with redundancy by row/column deletion for yield increase."
4. P. Mazumder and Y. S. Jih, “A new built-inself-repairtechniquetoVLSImemoryyieldenhancementbyemployingneuraltype

circuits,"IEEEproceedingsonComputerAidedDesign, vol. 12, No. 1, Jan, 1993.

5. A BISR (built-in self repair) circuit forembeddedmemorywithmultipleredundancies,H.C.Kim,D.S.Yi,J.Y.Park,andC.H.Cho,VLSI andCAD6thInternational Conference, pp. 602-605, Oct.1999.
6. "EfficientBISRTechniquesforWord-OrientedEmbeddedMemorieswithHierarchical Redundancy," Shyue-Kung Lu,Chun-LinYang,andHan-WenLin,IEEEICIS-COMSAR,pp. 355-360, 2006.
7. A Designer's Guide to Built-In Self-Test,by C. Stroud, published by Kluwer AcademicPublishersin 2002.
8. In2009,researchersM.Karunaratneand B.Oomannpublished"YieldgainusingmemoryBISR-acasestudy"intheIEEEMWSCASproceedings,onpages699-702.
9. High efficiency memory BISR with twoserial RA stages utilising spare memories, I.Kang, W. Jeong, and S. Kang, IET Electron.Lett.,vol. 44,no. 8,pp. 515-517,Apr. 2008.
10. Forexample,see"ABISR(Built-InSelf-Repair)circuitforembeddedmemorywith multiple redundancies," by Heon-cheolKim,Dong-soonYi,Jin-youngPark,andChang-hyunCho,publishedinProc.Int. Conf.VLSICAD,October1999,pages602-605".