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A NOVEL MULTI-CELL DC-AC CONVERTER FOR APPLICATIONS IN RENEWABLE ENERGY SYSTEMS

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ABSTRACT – Any device that gathers electricity from various sources and stores it in batteries or super capacitors needs a DC-AC converter. This covers solar panels, fuel cells, and other similar technologies. The converter under discussion connects several H-bridge inverter stages in series to generate alternating current (AC) using a new multi-cell architecture. Hbridge DC connections are used by the system to insert and remove DC. With a low-voltage, high-current MOSFET in every switching cell, the suggested DC-AC converter outperforms standalone DC-AC converters in terms of efficiency. Both blended PWM mode and low cell voltage can be used simultaneously. As a result, less filtration is needed for the AC discharge. This study looks at recommended circuit design, crucial component location methods, and system performance. The show ends with an exhibit that includes a two-kilowatt laboratory setup.

Keywords: Multi-cell converter, DC-AC converter, Renewable energy systems, Power electronics

1. INTRODUCTION

Dual-mode setup Besides DC-AC converters and batteries, distributed energy systems use fuel cells, solar panels, and supercapacitors. This presentation will cover domestic solar power converter functioning and benefits. Please review the following essentials: 50–200 volts and 0.5–2 kW are the voltage and power ranges. Another vital power source is accessible. Most voltages are 230 or 240. DC-AC converters protect the structure from DC input and AC output in 4Q mode. Production of reactive electricity is possible. Create a reliable and efficient application conversion system. Figure 1a shows typical complete bridge circuits. Line-frequency alternators change current. Connections require certain conductors. New power MOSFETs boost H-bridge and DC-AC efficiency. At line frequency, system efficiency drops below 90%, while power transformers function at 95%.

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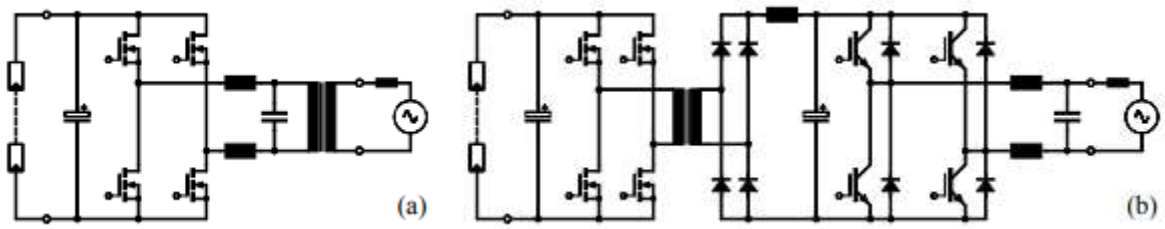

The solar power converter architecture is shown in Figure 1. Installation includes a MOSFET-H bridge and line-frequency isolation transformer. A high-frequency isolation transformer with a MOSFET DC-DC converter or a single-cell IGBT four-quadrant DC-AC converter are more options. Other high-frequency DC-DC isolation methods exist. All-in-one bridge DC-AC converters can be permanently hooked into wall sockets. Figure 1b shows that reducing mains transformer capacity increases efficiency and power density. This graphic shows the high-frequency isolation transformer's low losses. Consider inverter and line-side rectifier losses. IGBTs with power stages are common. They lose half-load efficiency at 400V DC. MOSFETs outperform IGBTs in current-independent on-state voltage loss. Operational point voltage reduction determines IGBT power requirements.

Figure 1 shows strategy similarities. Figure 1b shows a power-density-optimized high-frequency transformer. Illustration 1 shows how two motions fuse to form AC voltage. Increasing the switching frequency to eliminate current harmonics may bring harmonic effects into the main current, lowering system efficiency.

2. MULTI-CELL CONVERTER

By utilizing low-voltage power MOSFETs, an innovative circuit architecture resembling high-power converters has been developed. The intended application of the circuit design is in decentralized systems that are independent of a centralized power facility. One can create a compact device that surpasses its rivals by employing this approach, all the while circumventing complexities associated with converter topology. The subsequent enumeration comprises the fundamental elements of the methodology that was formulated:

DC input voltage:	U_1	=	100V (80...120V)
AC output voltage:	U_{AC}	=	$230V_{rms}$
rated power:	P_N	=	2 kW
efficiency:	η	>	94% @ rated power

• high-frequency isolation stage

• Low-voltage MOSFETs (majority carrier devices)

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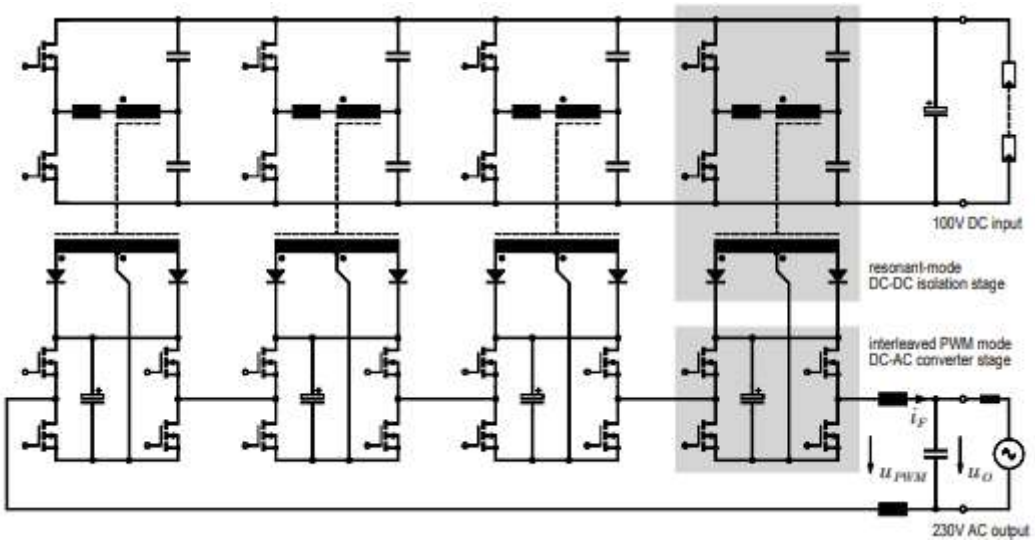

Fig.2: Basic circuit topology of the proposed DC-AC multi-cell converter based on high-frequency resonant-mode DC-DC isolation stages feeding interleaved PWM mode MOSFET DC-AC cells connected in series on the AC output (N=4 cells).

Figure 2 shows the circuit. AC is created by series-and-parallel converter cells. High-frequency separation connects the DC voltages of cells via full-bridge inverters. Since low-voltage devices employ series-connected inverter stages, they utilize the same semiconductor technology.

At a specific frequency, a capacitively linked half bridge converter runs in series resonant mode. Configuration of pulse breadth is its sole purpose. During continuous transmission, resonant networks reduce on-state and switching losses when the switching frequency exceeds the natural frequency. This occurs when free flow produces no current or voltage. For each DC-AC phase, the system DC input voltage is proportional to the DC link voltage. PWM regulates the AC output current and voltage of a DC-AC converter. In all cells, interleaved PWM modes reduce filter workload by half. Because the reference voltage and cell voltage output diverge somewhat, this is the case. At a low PWM switching frequency, switching losses in each DC/AC cell are diminished. The stabilizing capacitor can be paralleled with the isolation stages at the DC input to reduce ripple current.

3. SERIES-RESONANT ISOLATION STAGE

Series-resonant isolation was chosen because power transistors function better without voltage or current. Inductance rises from transformer leaks. Restricted blocking voltage. We need leak-proof flyback converter transformers. Good sense is lacking. Our current understanding proposes lowering primary and secondary connection capacitance first. Architecture generates voltage. Only low-coupling capacitance PWM DCAC cells may generate common mode current. The circuit design minimizes costly transformer leakage.

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Connects to transformer's copper main winding. You may have heard "bow winding principle." Secondary windings require care. Serial resonance circuits benefit from its rapid leaking and low coupling capacitance.

Analysis of the Stationary Operating Behavior

The following sections discuss stationary activity. Find the secondary center before translating. Figure 3a shows a diode with a lower forward voltage than bridge rectification. The center receptacle rectifies output voltages below 120V using 400V diodes. Bridge rectification just requires a 200V diode. A center-tapped bridge rectifier with two 200V devices and a 400V diode is more efficient despite having a higher on-state voltage.

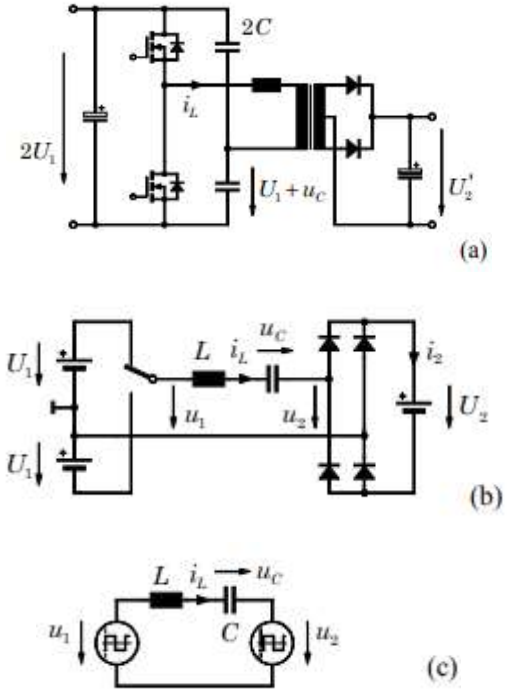

Fig.3: Circuit diagram of the series resonant converter (a) and corresponding equivalent circuits (b,c).

	$u_1 > 0$	$u_1 < 0$
$i_L > 0$	Ⓐ $\Delta U = U_1 - U_2$	Ⓑ $U_1 + U_2$
$i_L < 0$	Ⓓ $U_1 + U_2$	Ⓒ $\Delta U = U_1 - U_2$

Tab.1: Operating states of the series resonant converter

As seen in Figure 3(b,c), this circuit requires only the bridge rectifier. The system's four steps depend on input and reflected voltage polarities. Control circuit u1 and resonant current Li's direction u2. Tab 1 lists A–

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D states. Case A has perpendicular voltages u1 and u2. Build this little differential in the LC series circuit using U = U1 - U2. As the system revolves around [+ΔU,0], its center of gravity is there. Figure 4a displays the resonant network's Z0 = L/C impedance. Unlike its switching frequency (Fs), the system's intrinsic frequency (π LC) is 1/(2) 0f. Inversion of u1 occurs instantly if the high-side transistor is isolated before iL reaches zero. In state B (Figure 4(b)), the sum of U1 and U2 significantly reduces current along the circle axis [−(U1 + U2,0)]. The rectifier diodes' iL current changes from positive to negative in one second because u2 and u1 are negatively polarized. The "C" jurisdiction. State D begins at instant 3 when the lower power transistor trips and its center point is [+(U1 + U2, 0]]. Currently, the pathway center is [ØΔU,0]. Cycle terminates at 4 ms.

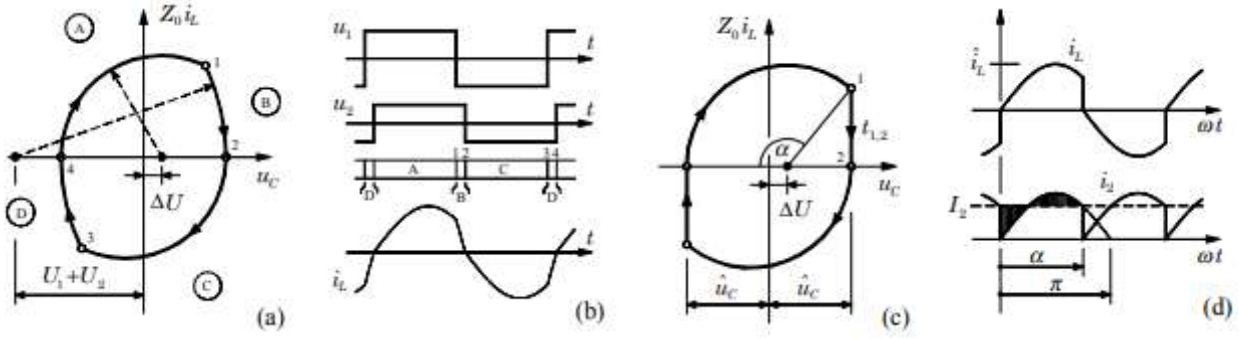

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Fig.4: System trajectory (a) and time behavior (b) of the series resonant converter; (c), (d): simplification valid for ΔU << U1 ; i 2 : output current of rectifier (cf. Fig.3 (b)).

The series resonant converter stage's minimum value of ΔU need to be significantly less than U1. Inductance, or L, is the most likely place where a transformer may have leakage. If there is leakage, the characteristic impedance, Z L/C 0, will be different. Figure 4(c) shows the actual route of the system, which should remain unchanged if the data is accurate. The impact of states B and D on i2 (t1,2 → 0) is seen in Fig. 4(c). Raise the inclination of the motion.

The equation $\alpha = \frac{\pi}{f_S / f_0}$ (1)

$$(\hat{u}_C + \Delta U)\cos(\pi - \alpha) = \hat{u}_C - \Delta U \quad (2)$$

And $Z_0 I_2 = (\hat{u}_C + \Delta U)\frac{1}{\alpha}\int_0^{\alpha}\sin(\omega t)\,d\omega t$ (3)

can be written according to the geometrical relations given by Fig.4 (c) and according to the fact that the average value of i_2 (i.e., the rectified inductor current i_L) in the stationary case is defined by the load current I_2 . Evaluation of Eq.(3) and rearranging using Eq.(2) finally leads to

$$\Delta U = I_2 \cdot R_{out} \quad \text{with} \quad R_{out} = Z_0 \frac{\frac{\alpha}{2}}{\tan^2\frac{\alpha}{2}} \quad (4)$$

$$\hat{u}_C = \frac{\alpha}{2} Z_0 I_2 = \frac{I_2}{4 f_S C} \quad (5)$$

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The output voltage (U2) is mostly determined by the load current (I2) when the switching frequency (α) remains constant. Figure 5 shows a path with a constant output resistance for all currents passing through it. This shows that the converter's output impedance is near to quasiohmic. When current travels through the commutation inductances of a line commutated converter, the voltage at the output decreases linearly. The commutation voltage drop of this system is similar to this. An exact calculation as given in results in an output characteristic described by ellipses (cf. thin curves in

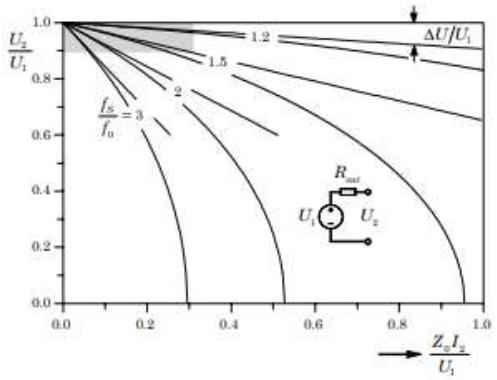

Fig.5: Output characteristic of the series resonant converter for fixed frequency operation above the natural frequency.

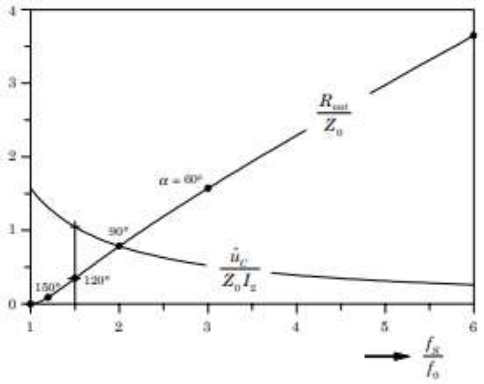

Fig.6: Dependency of the output impedance R_{out} and of the capacitor peak voltage value on the switching frequency.

Kindly see Figure 5. See Figure 5 for an illustration of how the streamlined method correctly determines the operational zone (ΔU < 10%) of the suggested system. A strong positive association has been observed between switching frequency and output impedance, as illustrated in Figure 6. Rout →0 and 0 f f S → are both possible vectors that can be used. As a result, S—the expected property of stiff output—should be negative. In order to reduce the quick response time, especially at high voltage, it could be possible to remove Rout's dual function as an output filtering capacitor and a damping resistor, as shown in Figure 5. For power transistors to operate at a neutral voltage, there must be a non-zero current, or iL. Any remaining

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electrical current will build up in the capacitance between the source and discharge if you don't do this. Usually, the goal is to create a harmonious network that runs between 5.0 and 1.0 S in frequency.

Practical Design and Realization

The following are the stage combinations for DC-DC isolation in a multi-cell converter: As mentioned earlier, the primary characteristics encompass a four-cell arrangement boasting a rated power output of 2 kW.

DC input voltage: U_1 = 100V (80...120V)
DC output voltage: U_2 = U_1 (1:1 transf. ratio)
rated power: P_N = 500 W
switching frequency: f_S = 100 ... 125 kHz.

Both applications used SiliconMAX PSMN035-150P power MOSFETs (TO220, 150V, 35mΩ). By increasing discharge, the IR2113 driver circuit speeds MOSFET gate turn-off. Additionally, two BC327 PNP transistors are used. The transformer's center-tapped rectifier secondary has a MUR1640 (2x8A, 400V) diode. Power transformers use "bow winding principle." N1 = 5 2.5-mm copper bows are joined to the primary winding E42/21/20 ferrite core (N87). The converter's secondary windings (N2 = 2 x 10 turns, −1mm) are constructed using standard methods for a 1:1 voltage transfer ratio. Figure 7 depicts the small transformer coil former construction with required creepage and clearance distances. The dimensioning data given before causes a peak flux density of B ≈ ˆ 100mT resulting in core losses of

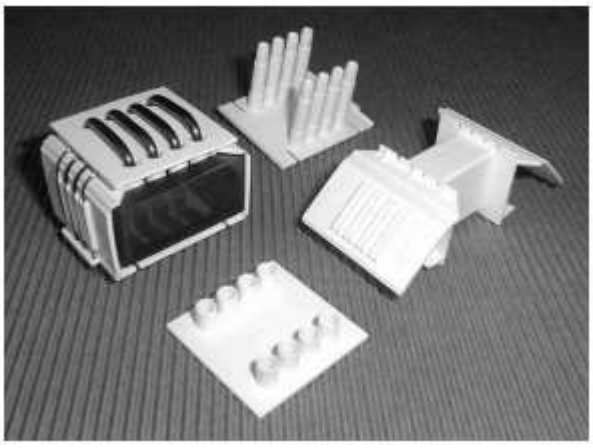

Fig.7: Transformer of the resonant 500W DC-DC converter using ″bow winding″ technique (shown here for N1=4) for direct PCB mounting and components of the coil former.

$P_{Fe} \leq 3W$ @ (U1 = 120V, f_S = 125kHz, T = 100°C) as specified by the data sheet. Although the proposed winding technique does not show very tight coupling, the stray inductance of the transformer is too low and a small additional choke (5 turns of litz wire on a single ETD29 leg (half core set)) has to be used for adjusting the natural frequency of the resonant circuit to f0 ≈ 80 kHz. With the applied resonance capacitors (2x5x0.1µF polyester foil type components in parallel, C = 1 µF) for f_S = 125 kHz this results in

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$L = 4\ \mu H$ $\quad Z_0 = \sqrt{L/C} = 2\ \Omega$

$\frac{f_S}{f_0} = 1.5$ $\quad \alpha = 120°$

$R_{out} = 0.7\ \Omega$ $\quad \hat{u}_C = 16\ V\ @\ I_2' = 4\ A$

Concerning R_{out} it has to be noted, that R_{out} specifies the output impedance related to the primary side of the transformer; this value has to be multiplied by $(N_2/N_1)^2 = (10/5)^2 = 4$ for characterizing the output (load-side) behavior of the converter.

Laboratory Prototype System – Measurements

The wave patterns seen in Figure 4 mostly match the results from the laboratory model (see Fig. 8), with the exception of the rectifier diodes' large reverse recovery current (I RR = 3.5A). A di/dt value of 40A/µs is indicated in the MUR1640 datasheet. An efficiency of 96.3% was obtained by testing the loss at the designated power level of 500W and switching frequency of 110 kHz (Figure 9). Effective rates in partial load zones might reach up to 97%. It is possible for reverse-biased diodes to account for up to 50% of total energy losses. The dual-thyristor method demonstrates the possibility of achieving total zero-voltage switching throughout the load region through the use of a driver stage that is intrinsically capable of turning on at uDS = 0.

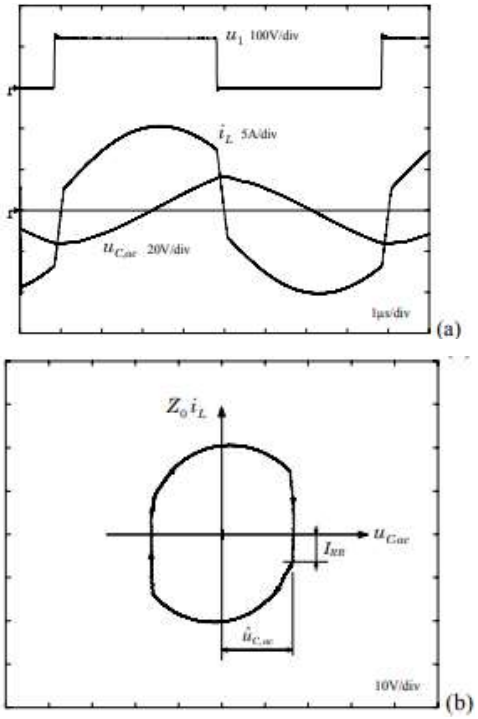

Fig.8: Measured voltage and current wave shapes (a) and measured system trajectory (b) of the laboratory prototype of the series resonant DC-DC converter; parameters: $U_1 = 120V$, $f_S = 125kHz$, $P \approx 440W$.

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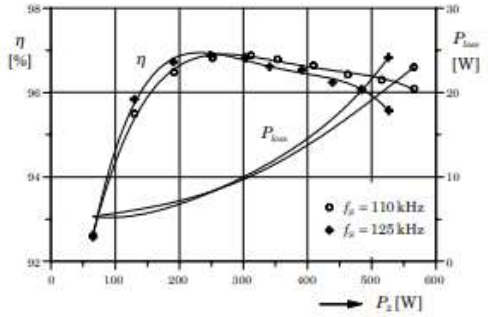

Fig.9: Measured losses and efficiency of the prototype DC-DC isolation stage; parameters: U_1 = 120V.

of synchronous rectification circuit extensions as will be proposed. Furthermore, the switching losses could be optimized by implementation of a load-dependent interlock delay time of the driver stage or,

4. MULTI-CELL DC-AC CONVERTER

The DC-AC converter's multi-cell class-D switch-mode amplifier generates 230Vrms AC. This multi-cell layout works well because interleaved PWM mode cell toggling decreases output current variations by N2 (where N is the number of cells). A second-order LC output filter on N3 decreases filtering capacitor voltage disturbance. A 4 N reverberation decrease is 64%. This lowers device PWM switching frequency. fPWM (1 kHz one-cell toggling) was used. FIGURE 6: Interleaved pulse width modulation device. Stacking flip-flops creates four squares. Four-stage signaling analog processors. The integrator produces four phase-shifted triangle signals. Comparators of PWM communicate. Using inexpensive optocouplers (SFH606) separates the switching cell's mobile driving stages from the PWM generator. Standard 0.5W DC-DC converters power IR1111 gate driving circuits. The multi-cell inverter driving stages are on the 1.8W control board.

Each 1:1 DC-AC converter power phase can use 16 PSMN035-150P MOSFETs, or 4x4. This multi-cell architecture can generate a range of voltage strengths, as shown by prototype system testing (Figure 10a for uPWM converter output voltage). Figure 10(b) shows a multi-level approach and output filter inductor current fluctuation (iF) (L=2mH). The filter capacitor (C=3µF) controls the system's AC output voltage (uO). The unprocessed output voltage uPWM has just 2NfS harmonic components, according to Fourier analysis (Figure 11). Consider fS values of 1, 8, 16, or any other frequency rationally. Interlaced PWM removes low-frequency components.

Figure 12 shows that the DC-AC converter's goal of high efficiency was met. This happens because the power transistors have a low RDS and almost no switching losses. But it has to.

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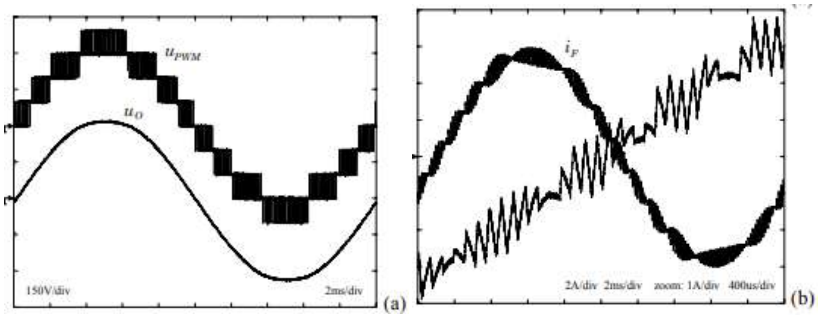

Fig.10: AC output voltage (u_{PWM} : before filtering, uO : after LC-output filter having ≈2kHz roll-off frequency (a) and output filter inductor current (b) of the DC-AC converter laboratory prototype; parameter: f_S = 1kHz.

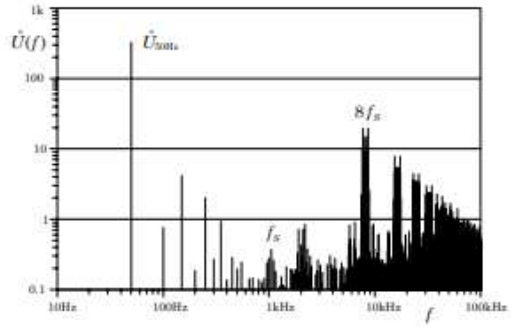

Fig.11: Frequency components of the unfiltered converter output voltage u_{PWM} . The harmonics in the frequency range 100...700Hz are due to an non-ideal behavior of the dutycycle limiting stage which is required to guarantee the operation of the charge-pump of the IR2111 driver).

The utilization of accurate testing equipment is particularly crucial when assessing losses in high-efficiency converters. Inaccurate measurements can significantly affect the efficacy and loss parameters of the research converter. Greater care must be taken when comparing and calculating data derived from samples collected using a variety of measurement instruments and systems.

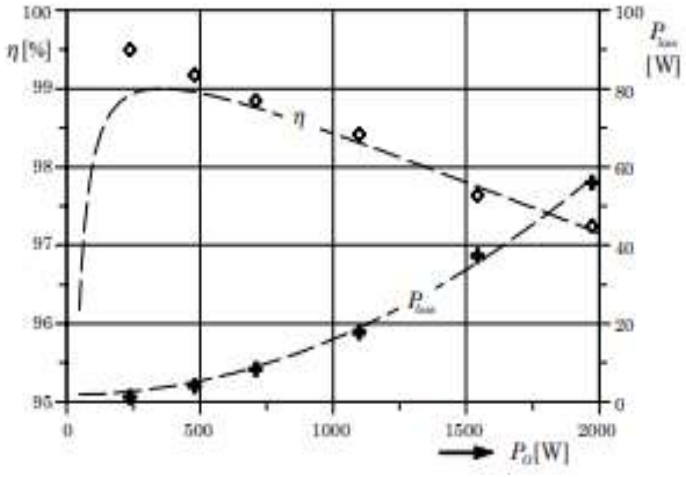

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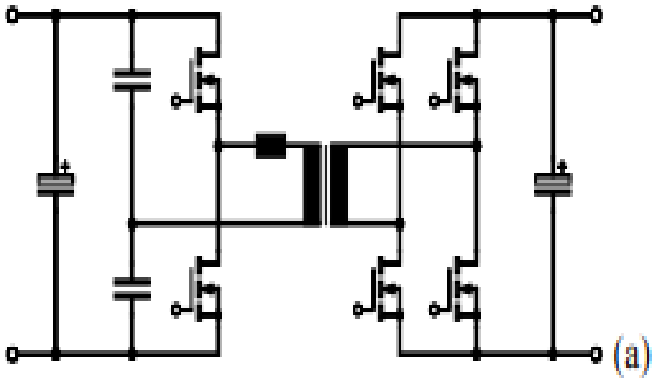
Fig.12: Efficiency and losses of the DC-AC converter. The characteristics shown by the dashed curves give an approximation based on an ideal 230V voltage source with 0.75Ω output resistance and 1.8W permanent no-load losses. Furthermore, the diagram demonstrates the sensitivity to measurement errors especially for very high efficiency values because the dashed curve in any case defines an upper limit for the efficiency.

5. CONCLUSIONS – FUTURE DEVELOPMENTS

The proposed multi-cell multi-level converter uses lower-voltage MOSFETs to convert energy to 230VRMS mains voltage. The low active voltage drop decreases conduction losses in these devices. A low switching frequency is needed for pulse width modulation in a single cell to reduce mains power supply switching losses. However, reduced mains current harmonics positively affect each cell's switching process. Low converter losses, high efficiency. Since DC-PWM converters regulate system voltage, comparable MOSFET devices in DC-DC and DC-AC converters power floating DC-AC stages.

A downside of the 2kW prototype is its 12 half bridge driver circuits and 24 transistors. Accessible power semiconductors improve heat dispersion and system cooling by reducing transistor losses. The prototype DC-AC converter generates 50% (1kW) electricity without a heat sink.



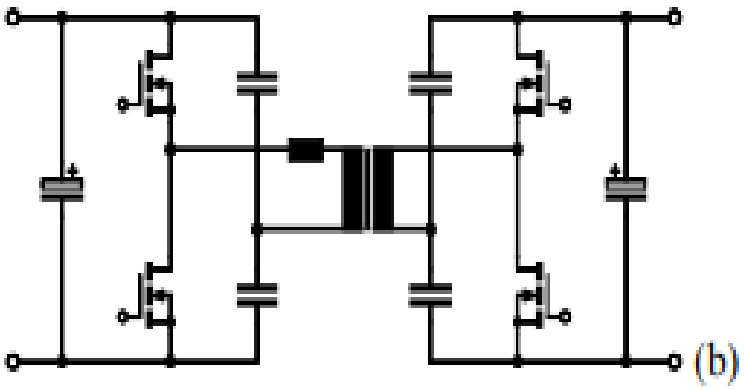


Fig.13: Extension of the resonance-mode DC-DC converter to synchronous rectification (a) and to bidirectional operation (b).

DC-DC isolation stage synchronous rectification could accelerate future advances since diode on-state losses cause most system losses. A superior full bridge circuit is shown in Figure 13(a). A shared converter I/O transistor should help most carrier electronics. Figure 13(a) shows two-way converter. Charge UPS, supercaps, batteries. Universal multi-cell DC-AC converters work. Potential reactive gridless electricity.

Figure 13(a) shows converter secondary DC current path core saturation. Transformer winding resonance capacitor or secondary side blocking capacitor in Figure 13(b) prevents this. Multicell converters help remote solar farms (Figure 14). Adjustable input chokes lower high-common-mode solar panel voltages. Figure 14 illustrates non-isolated multi-cell solar converters. It works, thus this style will be noticed. Simple DC input voltage control lowers AC harmonics. Decentralized solar power converters may help.

REFERENCES

[1] A. C. Rufer, N. Schibli, Ch. Briguet, "A Direct Coupled 4-Quadrant Multilevel Converter for 162 /3Hz Traction Systems", Proc. of the 6th Int. Conf. on Power Electronics and Variable Speed Drives, Nottingham, UK, 23–25 Sept., pp. 448– 453, 1996.

[2] H. Ertl, J. W. Kolar and F. C. Zach, "Analysis of a Multi-Level Multi-Cell Switch-Mode Power Amplifier", Proc. of the 41st Int. Conf. on Power Electronics and Intelligent Motion, Nürnberg, Germany, June 6–8, pp. 491–497, 2000.

[3] Y. Cheron, T. Meynard and C. Goodman, "Soft Commutation", Chapman & Hall (Kluwer Academic Publishers), Dordrecht, 1992.