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FIRST ORDER SIGMA-DELTA MODULATOR WITH LOW-POWER CONSUMPTION IMPLEMENTED IN AMS 0.35 µM CMOS TECHNOLOGY

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ABSTRACT: This paper describes the design of a switched-capacitor discrete time first-order Delta-Sigma modulator. The goal of this modulator is to convert eight bits of analog data into digital data. To perform properly, operational transconductance amplifiers must be capable of producing a wide range of output voltages and modest amounts of direct current while consuming low power. The modulator achieved an SNR of 49.25 dB using 0.35um CMOS technology, an 80 KHz signal bandwidth, and a 64 oversampling rate, according to the modeling results. 5.5 milliwatts of electricity were applied at a 1.5-volt source voltage.

Index terms: *Analog-to-Digital conversion, Delta-Sigma modulation, CMOS technology, Transconductance operational amplifier.*

1. INTRODUCTION

For a long time, high resolution has been accomplished in consumer audio devices such as mobile phones and MP3 players via Sigma-Delta (□�Y) Analog to Digital Converters (ADC). DS converters, or digital-to-analog converters, are useful in applications that require bandwidth and low-cost, high-resolution data. As a result, they are frequently thought to be useful for a wide range of applications. I-converters use analog (�Δ modulators and complicated digital filters.

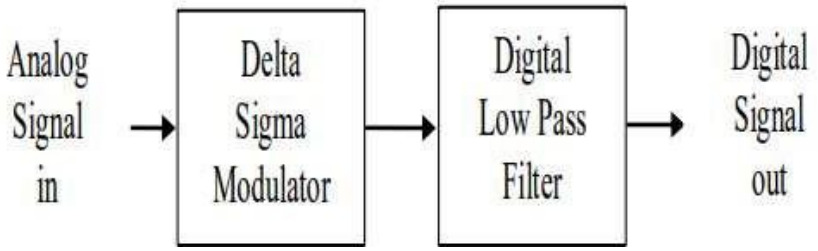

Figure 1: An illustration of the analog-to-digital converter.

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The modulator's error is determined by the high-performance amplifiers' linearity and noise levels. Sigma-delta modulators allow for erroneous analog circuits by trading off amplitude resolution for temporal resolution. Oversampled converters are common in digital audio because of their ability to handle narrow bandwidths. Figure 1 shows the block schematic for a ↄΔ modulated analog-to-digital converter. Omega-sigma converters use oversampling. Oversampling happens when the input signal is sampled more than once per Nyquist frequency cycle. This technology's ability to use analog signal processing circuits with lesser precision than the converter and 1-bit ADC is a key advantage. To obtain high resolution with ΔΔ, the hardware must function at an oversampled rate, exceeding the bandwidth of the utmost signal. Complex digital circuitry is thus necessary. Sigma-delta modulators of the first order are simple, reliable, and stable. Figure 2 shows the modulator.

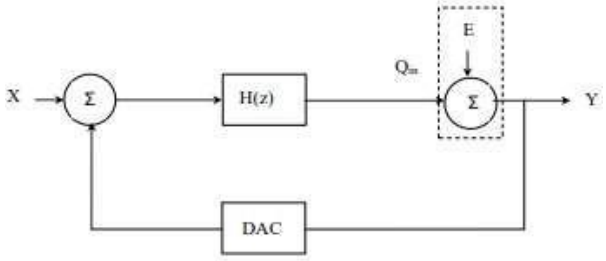

Figure 2: The first-order ΔΔ modulator can be described using a linear model.

The linear modulator system has a single input and one output. STF (z): System Signal Transfer Function

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \quad (1)$$

NTF (z): Noise Transfer Function

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \quad (2)$$

The output signal is generated by superimposing noise and input signals. The signals are then filtered independently using their respective transfer functions.

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \quad (3)$$

To achieve the desired z-domain output, choose the loop filter, signal transfer function, and noise transfer function for a theoretical first-order ΔΔ modulator.

$$STF(z) = z^{-1} \quad (4)$$

$$NTF(z) = (1 - z^{-1}) \quad (5)$$

Solving (1) and (4) gives:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (6)$$

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A loop filter is a simple integrator that may be built with switched capacitor techniques. The transfer functions of a generalized Lth order ΔΣ modulator are as follows:

$$STF(z) = z^{-L}$$

$$NTF(z) = (1 - z^{-1})^{L} \quad (7) \text{ \& } (8)$$

Integrators, which are fundamental components, are necessary to build a transfer function of the Lth order. When modulator orders surpass one, the NTF frequency response incorporates high-pass filter features. Order L increases the amount of energy lost at low frequencies due to quantization error. What is the output signal from the ideal linear model?

$$Y(z) = X(z).z^{-L} + E(z).(1 - z^{-1})^{L} \quad (9)$$

Analog and digital circuitry are linked by an analog-to-digital converter (ADC). They are critical components in many systems. The DS reduces the circuit's efficacy by prioritizing rate above accuracy. This is an excellent approach for acquiring precise ADCs. The discrete time Δ modulator effectively decreases noise and operating amplifier gain by noise shaping, capacitive matching, and oversampling. It is hence ideal for low-voltage applications. A wireless receiver's principal function is to retrieve modulated baseband signals transmitted via a radio frequency carrier wave. When designing a low-power, high-performance integrated radio frequency receiver in CMOS, noise, linearity, and power consumption must all be carefully considered. To achieve the goal, as illustrated in Table 1, each receiver and radio system component must be inspected. The user sets the data rate, modulation, hopping bandwidth, and baseband.

Table 1: Specifications of the receiver sensor

Direct conversion receiver	
Base band frequency (fb)	80 Khz
Modulation scheme	BFSK
Hopping bandwidth	7 MHz (863-870) MHz
Data rate (D)	20 Kbps

2. BACKGROUND WORK

ANALOG TO DIGITAL CONVERTERS TYPES

The functioning of oversampling and Nyquist-rate A/D converters differs. The first technique, depicted, samples the digital circuit's input signal at a rate fsamp larger than fin. The comparable value is three. Prioritize noise production and modulation to accomplish exact conversions. Increase the resolution (N) of the analog-to-digital converter and use a Nyquist-rate analog-to-digital converter to improve the signal-to-quantization noise ratio (SQNR).

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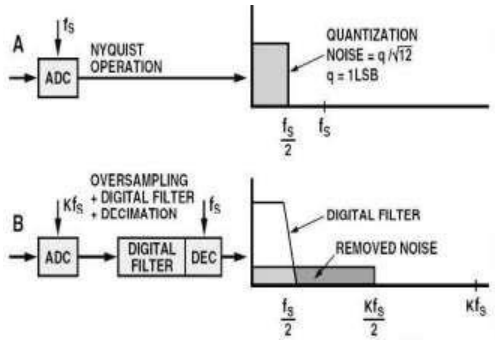

Fig.3. ADCs with oversampling and the Nyquist rate. The sampling rate, abbreviated as fsamp, is the sampling frequency. On the contrary, the fin represents the frequency of the incoming signal.

oΔ ADC and Nyquist-rate ADC have marginally different operational properties. Oversampling and noise shaping have an effect on signal variations. These parameters control the cacophony of sampled signals. The phrase "Over Sampling Ratio (OSR) ADC" refers to a system where the sampling ratio (SR) is more than one (see Figure). 1(B).

SECOND ORDER ΣΔ MODULATION

A classic analog-to-digital converter (ADC) that uses a second-order sigma-delta modulator is commonly used. This modulator resolves the equation in the z-domain.

$$W(z) = K(z) + S(z)(1 - 2z^{-1} + z^{-2}) \quad (10)$$

The input signal, quantization error process, and output Z transformations are represented by W, K, and S, respectively. Noise transfer functions for first and second-order modulators.

Compared to the second order ΔΔ NTF, the first order NTF limits quantization noise in the low signal band frequencies more. The second order ΄YΔ system reduces and shifts noise power outside the signal's bandwidth and band. The diagram shows the second-order modulator. The fourth digit.

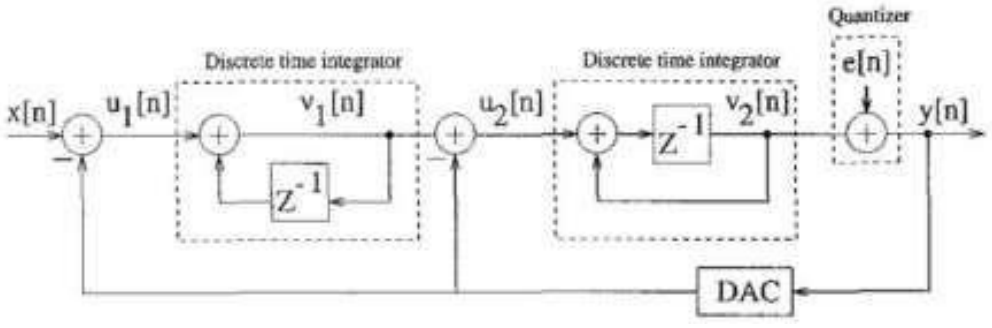

Fig.4. Sigma-delta modulator of order two.

The structure illustrated in Figure 4 is implemented by two integrators. The second signal transfer function is z -1/1-z-1, whereas the first is 1/1-z-1. The signal-to-noise ratio can be determined by applying a lowpass filter to the modulator output.

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L + 10)\log\left(\frac{f_s}{2f_B}\right) \quad (11)$$

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$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^4}{5}\right) + 50\log\left(\frac{f_s}{2f_B}\right) \quad (12)$$

Again, letting $\frac{f_s}{2f_B} = 2^r$, power is (σ_x^2), L represents the modulator order, then:

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^4}{5}\right) + 15.05r \quad (13)$$

Each additional r adds 2.5 bits of precision or 15 decibels of SNR. The enhancement is slightly superior to that of a first-order Ση. Additionally, it affects the power or variance $\sigma e2$.

THIRD ORDER SIGMA-DELTA MODULATION

A low-noise, precise output system requires high-order noise transfer functions (NTFs) to maintain noise outside the signal's bandwidth or to reduce noise power. For a given signal bandwidth, a lower sampling rate can nonetheless yield a comparable level of precision. This minimizes the need for analog device velocity. Hx=z-1 is the signal transfer function, while He=(1-z 1) M is the noise transfer function, which has M zeros at z=1. Using transfer functions, one can create an order M modulator. By applying the second-order structure shown in the picture. By connecting an integrator between the summer node input and the first integrator of the second order modulator, the system transforms into a third-order modulator with a signal transfer function (STF) of 1/(1 - z -1).

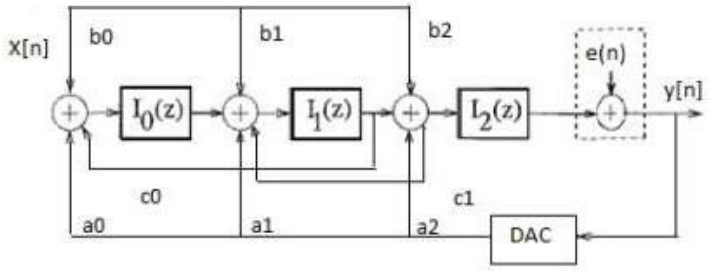

Fig.5. Topology of third-order modulators.

Deducting -y[n] from the difference between x[n] and y[n] of the additional integrator yields the new integrator output. This output serves as the input for our feedback cycle. When compared to lower order modulators, the third order modulator's Noise Transfer Function (NTF) efficiently pushes quantization noise to higher frequencies outside of the intended range. Within the range of a third-order modulator, the maximum SNR is

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^6}{7}\right) + 70\log\left(\frac{f_s}{2f_B}\right) \quad (14)$$

$$\text{Let } \frac{f_s}{2f_B} = 2^r, \quad (15)$$

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^6}{7}\right) + 21.07r \quad (16)$$

The third order modulator's signal-to-noise ratio (SNR) improves by 21 dB with each triple of the OSR. The increase in resolution bits is 3.5. To convert a 20 kHz signal to 23 bits, the modulator needs the following: modulator order (r), 10.24 MHz sampling frequency (fs), and input signal frequency (fB).

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3. DESIGN OF DELTASIGMA MODULATOR

The majority of devices are first-order ��Δ modulators, which are more stable than second- and third-order circuits. Each ��Δ modulator requires an integrator, which often uses CMOS technology. Sigma-delta modulators of the first order are simple, reliable, and stable. First-order ΄YΔ modulators are more energy-efficient and compact than other types. The effective bit count of a Ÿ (Neff) converter is calculated by:

$$N_{eff} = \frac{1}{2}\log_2\left[(2N-1)^2(2L+1)\,OSR^{2L+1}/(\pi)^{2L}\right] \quad (17)$$

The Over Sampling Ratio is calculated using N (quantization circuit bits, N = 1) and L (modulator order, L = 1).

$$OSR = \frac{F_s}{2\times f_b} \quad (18)$$

With an OSR of 64, the base band frequency (fb) is 80 KHz, while the sampling frequency (Fs) is 10.240 MHz. Manufacturing defects in the parasite modulator diminish both the signal-to-noise ratio (SNR) and the bit count, yielding a theoretical value of 8.14 bits. The eight-bit architecture is used to reduce power consumption and utilization. Figure 6 shows the functional diagram of a first-order modulator generated with Simulink in MATLAB. A conductor is used instead of a single-bit DAC. A sinusoidal signal at 20 kHz and 0.4 V is used as input, and the signal obtained by one integrator is linked to the comparator at the output.

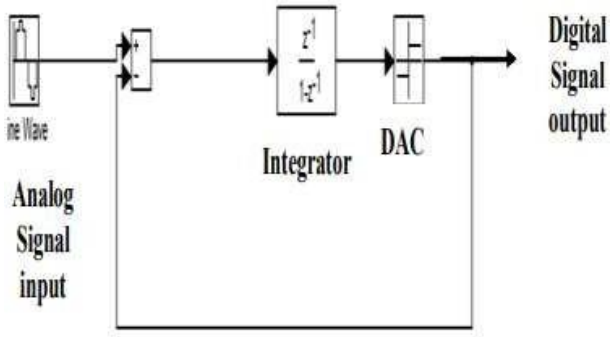

Figure 6: Diagram of the First Order ‹Δ Modulator

Figure 7 shows the modulated output of the scope layered with the input signal.

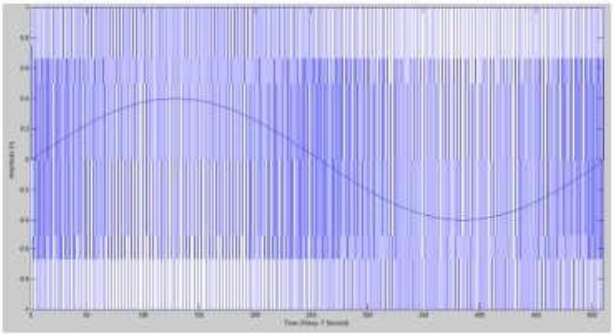

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Figure 7Initial Order Diagram for the Sigma-Delta Modulator Block

A system's SNR is determined by performing a discrete Fourier transform (DFT) on the sampled output signal. The SNR is 99.25 dB, as illustrated in Figure 8 by plotting the logarithm of the signal's amplitude vs frequency.

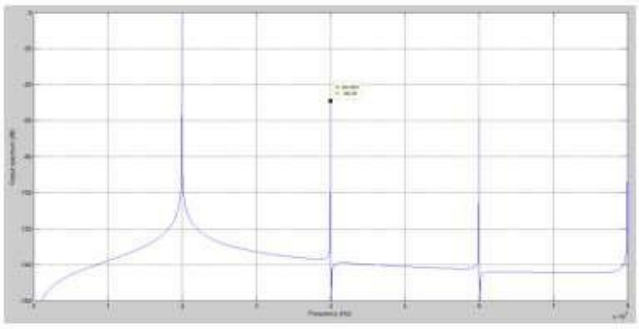

Figure 8: Zooming into the frequency spectrum of a modulated signal

Figure 9 shows second-order noise shaping, which transfers the majority of noise to higher frequencies. The use of a digital low pass filter helps restore the original signal.

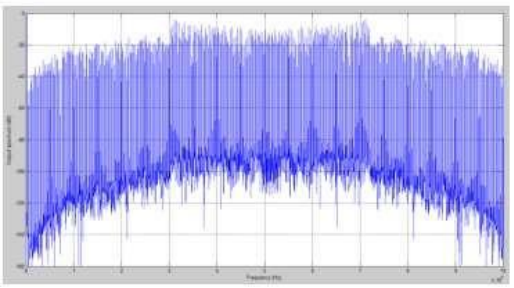

Figure 9: Analysis of the spectrum of the modulated signal.

Figure 10 shows the block schematic for a first-order ΔΔ modulator. The system's components include a DAC, an integrator, and a comparator. Switches Q and Q' apply the +Vref or -Vref reference node voltages, depending on whether the comparator output is positive or negative. The amplifier-based integrator sequentially exploits phases ʃ1 and 2.

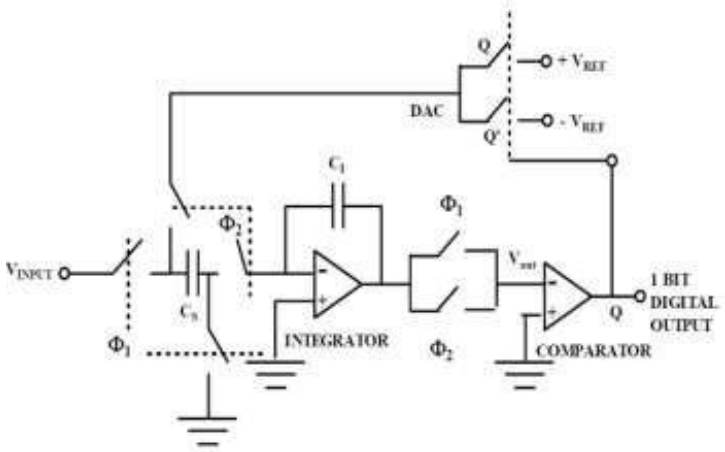

Figure 10: First-order, fully integrated Sigma-delta modulator.

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The operational transconductance amplifier (OTA) in a □◆Δ modulator needs a wide bandwidth and high voltage gain at low frequencies. The latter reduces quantization noise, whereas the former controls modulator bandwidth. Figure 11 shows an OTA's updated current source. M1 and M2 are P-channel MOSFET inputs. Devices with N- or P-channel MOSFET inputs work. PMOS input devices are more widespread because to their lower 1/f noise and faster slew rate. PMOS input devices lower voltage sensitivity and increase power supply rejection using current mirrors. The operational amplifier's current mirror circuit used M3 and M4 N-channel MOSFETs in its early phase. Second operational amplifier stage transistor M7 is a P-channel common source amplifier. Updated source architecture includes correction and polarization.

The polarization block has four transistors (M12, M13, M14, and M15) with different input voltages and resistances. M9–M11 transistors form a correction block. Balancing M10 and M11 drain-source voltages minimizes duplication mistake. Using an amplifier between the mirror's input and output transistors (M10 and M11), this equivalence is achieved accurately and linearly. Due to amplifier output current at its gate, transistor M9 has a high output impedance. An amplifier between the mirror's input and output transistors improves current copying. The amplifier was K-designed. Tanno. Figure 12 shows two NMOS transistors (MN1 and MN2). Our zero source gate voltage places MN1 in moderate inversion. This design saves voltage and power by running in the linear or saturation area. To maximize power dissipation and semiconductor area, conventional amplifiers use four transistors. K's method. Tanno's high output resistance, low bias current, tiny chip size, and low voltage operation are advantages. Therefore, voltage-to-current converters adopt this arrangement. Formula for total amplifier gain:

$$A_v = g_{m1}\left(r_{ds2} // r_{ds4}\right).g_{m7}\left(r_{ds6} // r_{ds7}\right) \quad (19)$$

The i-th transistor has drain-to-source resistance (rds) and transconductance (gm), where i is one, two, four, six, or seven.

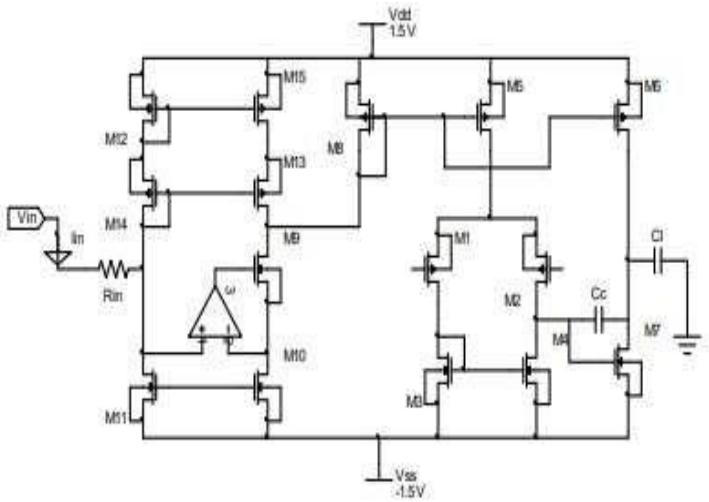

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Figure 11: An antenna for functional transconductance with adjustable current.

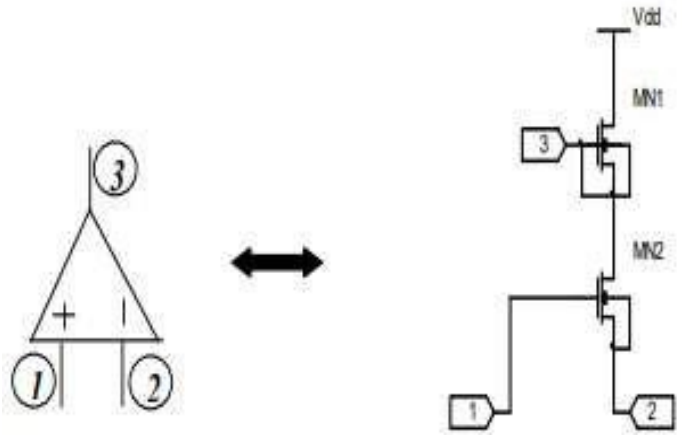

Figure 12: The configuration of the twin transistor amplifier

Figure 13 shows the output frequency response of our 0.35µm OTA simulated using Tspice and the BSIM3V3 transistor model at a power supply voltage of ±1.5V. The bode diagram depicts numerous key frequencies and phase margins, such as the cut-off frequency of 97 kilohertz, the open loop gain of 60 dB, and the high gain-bandwidth product of 82 MHz. For polarization, 10µA of input current (or -1V of Vin) is flowing through M8.

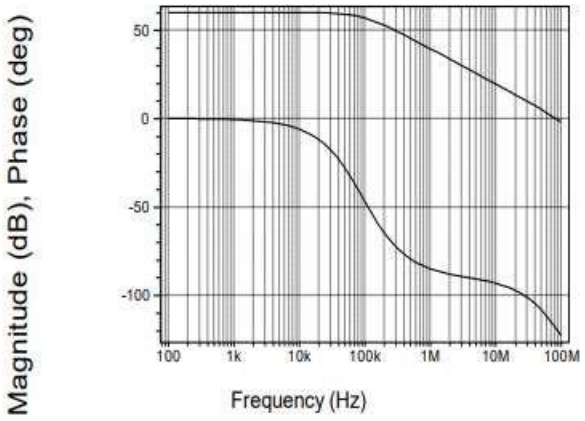

Figure 13: An operable transconductance amplifier responds to frequency.

4. RESULTS AND COMPARISON

The fabrication of modulators makes use of 0.35um CMOS. At 80 kHz, the oversampling ratio is 64 while the bandwidth is maintained. Table 2 summarizes the modulator's features.

Table 2: Specific modulator specs

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Parameters	Value
Technology	0.35 µm
Order of modulator	1
Sampling Frequency (clock)	10.24 MHz
Signal Band width	80 KHz
Over sample Ratio(OSR)	64
References	±1V
Maximum Input	1 V_{pp}
Supply voltage	±1.5V
Resolution	8-bit
Signal to Noise Ratio (SNR)	49.25 dB
Quantizer resolution	1 bit
Power consumption	5.5 mW

The ΄YΔ modulator design limits are mostly determined by present technology limitations and sampling rates. The table below compares the published and current works of three well-known designers. This work uses a 0.35 µm CMOS technology to achieve 8-bit resolution while consuming less power than previous studies.

Table 3: A comparison table of emerging trends and familiar designs (*)

Resolution	OSR	SNR (dB)	Speed (MHz)	Power (mW)	Process (CMOS)	Signal Band width
14-bit	24	85	2.2	200	0.35µm	100 KHz
11-bit	10	62.5	300	70	0.13µm	15 MHz
14-bit	96	85	53	15	0.18µm	300 KHz
16-bit	128	-	5.12	2.6	0.18µm	20 KHz
8-bit	64	49.7	1.024	6.6	0.6µm	8 KHz
8-bit *	64	49.25	10.24	5.5	0.35µm	80 KHz

5. CONCLUSIONS

To save power, the modulator uses switched-capacitor techniques. It is made with 0.35 µm CMOS technology and has an 8-bit resolution. Compared to other ΎΥΔ modulators, the first-order single modulator outperforms them in terms of performance, stability, area, and system characteristics, including power consumption. A 1.5 V power supply consumes 5.5 mW of power.

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