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LOW POWER DELAY PRODUCT SRAM CELL DESIGN AND ANALYSIS USING REVERSIBLE GATES

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ABSTRACT
The use of electronics in different fields has risen in recent years, necessitating more memory for storing and processing data. Because of its fast speed, SRAM is used in this type of application. SRAM aids in data quality access. SRAM is really important. Each bit is stored in a latching circuit, which serves as a cache memory in the devices. Cache memory operates at a high pace and consumes a lot of power. Devices that consume less power and operate at a rapid pace are required by current technology.
When you use a lot of memory, you use a lot of electricity. For memory cells, several SRAM factors, including as speed and power, must be enhanced. This necessitates the use of SRAM in conjunction with modern technology.The reversible logic gates were implemented and compared for power and delay. The low power reversible logic gates were used to propose a SRAM cell which has lower PDP.All the designs were implemented in 16nm technology using Hspice tool.
Keywords: 16 nm CMOS technology, Delay, Power consumption, Reversible logic, High Speed, SRAM.

1. INTRODUCTION

Since the 1960s, reversible gates have been studied. Reversible gates dissipate less heat, which was the original motivation (or, in principle, no heat). If we consider a logic gate to be consuming its input, information is lost because the output contains less information than the input. Because of thermodynamic entropy (Landauer's principle), this loss of information loses energy to the surrounding area as heat. Another way to think about it is that when charges in a circuit are grounded, they flow away, carrying a small amount of energy with them. A reversible gate only switches states, and because no information is lost, energy is conserved.
Reversible logic has received a lot of attention in recent years because of its ability to reduce power dissipation, which is a key requirement in low power VLSI design. It has numerous applications in low-power CMOS and optical data processing, DNA computing, quantum computation, and nanotechnology. Irreversible hardware computation wastes energy due to information loss. According to Landauer's research, every irreversible bit operation dissipates at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1(joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which the operation is performed. At room temperature, the heat generated by the loss of one bit of information is very small; however, when the number of bits increases, as in the case of high-speed data transmission, the heat generated increases dramatically.
Sithara Raveendran and Y.B. Nit hin Kumar proposed inexact signed Wallace tree multiplier design using reversible logic. In this 4:2 compressor is proposed using reversible logic gates which is able to reduce reversible logic realization metrics like garbage outputs, gate count, quantum cost [1].
M. Kiran Kumar and M. Shanthi designed new gates called KS, KIRS, KIRANTHI which are formed from the garbage outputs of reversible gates in efficient way [2].
Reversible system design for CMOS circuits with perfect or 100% Concurrent Error Detection (CED) capability has been proposed by Sajjad Parvin and Mustafa Altun. They presented Even Target - Mixed

Polarity Multiple Control Toffoli as a new fault-preservative reversible gate library for this purpose (ET-MPMCT). They were able to verify that the evenness/oddness of applied 1's at input is retained at all levels of a circuit, including the output level, by employing ET-MPMCT [3].
Reversible logic gates were previously implemented in superconducting circuits as adiabatic-reversible gates, which are powered with a sufficiently slow clock. In contrast, we are studying ballistic-reversible gates, where fluxons serve to both encode the information and power the gates. No power is applied to the gate apart from the energy of the input fluxons, and the two possible flux polarities represent the bit states [4].

2. STATIC RANDOM ACCESSMEMORY

SRAM (static random access memory) is a type of random access memory (RAM) that keeps data bits in its memory as long as power is available. Unlike dynamic RAM (DRAM), which must be refreshed on a regular basis, SRAM does not require this, resulting in improved performance.
Personal computers, workstations, routers, and peripheral devices all employ SRAM: CPU register files, internal CPU caches, external burst mode SRAM caches, hard disc buffers, router buffers, and so on. SRAM is commonly used in LCD panels and printers to keep the image displayed.
Ashish Sachdeva, Vinay Tomar designed Decoupled 9Transistor SRAM which minimizes power dissipation and maintains stability during read, write operation [5].
Vishal Sharma, Neha Gupta designed 11T SRAM which confirms its reliability for Internet of Things (IoT) based health monitoring system executes improved write and read ability using data dependent feedback and read decoupled access path mechanism [6].
WEI-XIANG YOU, PIN SU, and CHENMING HU suggested a new 8T non-volatile SRAM (nvSRAM) cell that uses both ULP and ferroelectric FinFETs to provide energy-efficient and low-latency store/recall operations. Unlike other types of non-volatile SRAM that require additional circuitry or non-volatile memories connected to a standard 6T SRAM cell to achieve nonvolatility, the proposed hybrid nvSRAM cell reduces the area penalty by embedding non-volatile ferroelectric FinFETs in a 6T SRAM cell without sacrificing cell stability, read/write performance, or power consumption [7].
Carbon nanotube (CNT) field-effect transistor-based static random- access memory (SRAM) arrays (CNFETs).
We show that 1 kbit (1024) 6 transistor (6T) SRAM arrays constructed with complementary metal-oxide-semiconductor (CMOS) CNFETs (totaling 6144 p- and n-type CNFETs) work perfectly without any per-unit modification. CNFET SRAM can be built directly on top of computational logic to create three-dimensional integrated circuits, and CNFET circuits can use metal routing above and below the CNFET device layer[8].

3. REVERSIBLE GATES

We have examined six reversible gates. Those are Feynman gate, Fredkin gate, Toffoli gate, Peres gate, Sayem gate and DKGgate.

Feynman Gate

The Feynman gate is also known as the controlled-not-gate (CNOT). It has two inputs (A and B) and two outputs (A and B) (P, Q). P=A, Q=A XOR B determines the outputs. A signal can be copied using this gate. Due to the fact that fan-out is not permitted in reversible logic circuits, the Feynman gate is employed to replicate a signal.

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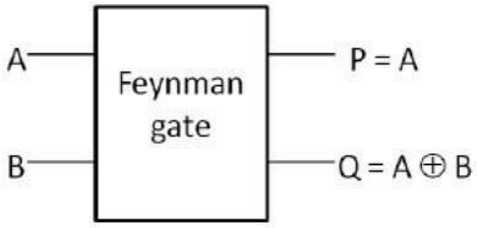

Fig.1: Block diagram

Table 1: Truth Table

A	B	C	D
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fredkin Gate

Edward Fredkin designed the Fredkin gate (also known as the CSWAP gate or conservative logic gate), which is a reversible computing computational circuit. It is universal, which means that it can be used to construct any logical or mathematical action. The Fredkin gate is a three-input, three-output circuit or device that transmits the first bit unmodified while swapping the following two bits if and only if the first bit is 1.

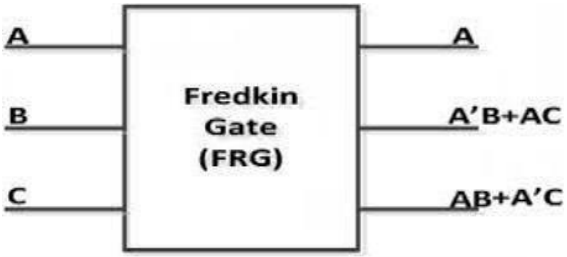

Fig.2: Block diagram

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

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1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 2: Truth Table

Toffoli Gate

The Toffoli gate (also CCNOT gate), created by Tommaso Toffoli, is a universal reversible logic gate in logic circuits, meaning that it can be used to build any classical reversible circuit. It's also known as the "controlled-controlled-not" gate because of the way it works. It contains 3-bit inputs and outputs; if the first two bits are both 1, the third bit is inverted; otherwise, all bits are unchanged. By the pigeonhole principle, any reversible gate that consumes its inputs and allows all input calculations must have no more input bits than output bits. There are two possible reversible gates for each input bit. One of them isn't one of them. The identity gate, on the other hand, maps its input to its output in the same way.

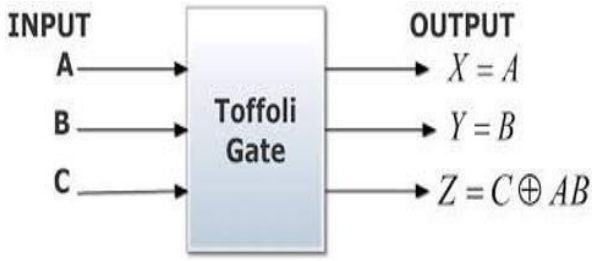

Fig.3: Block diagram

Table 3: Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

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1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Peres Gate

The Peres gate is a simple reversible logic gate that can be found in many different reversible circuits. The design of a Peres gate inside a lithium-niobate-based Mach-Zehnder interferometer using electro- optic effect is proposed in this study. Peres gate applications such as full-adder circuits and flip-flops are also discussed.

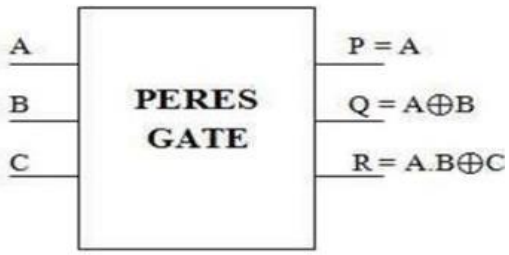

Fig.4: Block diagram

Table 4: Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1

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1	1	1	1	0	0

Sayem Gate

SG Gate, PFAG Gate, PFAG Gate, PFAG Gate, PFAG Gate, Sayem gate is another name for SG gate [31]. It's a four-way reversible gate. I V = (A, B, C, D); O V = (A, A'BAC, A'BACD, ABA'CD); I V =(A, A'BAC, A'BACD, ABA'CD); O V = (A, A'BAC, A'BACD, ABA'CD), where I V and O V are input and output vectors, respectively. The quantum cost of the SG gate has yet to be published in the literature. Sayem gate is made up of a reversible Fredkin and Feynman gatecombination.

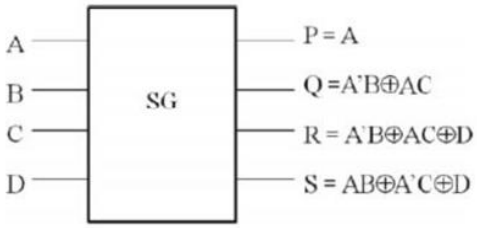

Fig.5: Block diagram

Table 5: Truth Table

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1

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1	1	1	1	1	1	0	0

DKG Gate

A reversible 4* 4 DKG gate [6] that can function as a reversible Full adder and a reversible Full subtractor on its own. It may be verified that the input pattern that corresponds to a specific output pattern can be determined uniquely. It can be used as a full adder or a full subtractor. The suggested gate functions as a reversible Full adder if input A=0, and as a reversible Full subtractor if input A=1

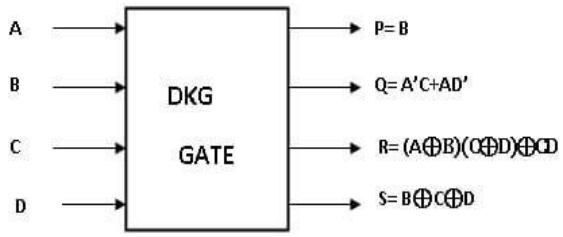

Fig. 6: Blockdiagram

Table 6: TruthTable

A	B	C	D	P	Q	R	S
0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	1	0	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	1	1
1	0	1	1	0	0	1	0
1	1	0	0	1	1	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	1	0	0
1	1	1	1	1	0	1	1

4. COMPARISON AND SIMULATIONRESULTS

All reversible gates are simulated using Hspice software with 16 nm technology. Parameters such as the total power dissipation and delay for all reversible gates are also compared here. The simulation results from

Table 7:Comparison of delay in 16 nm technology (nS)

Gate	0.7V	0.8V	0.9V	1.0V	Average
Feynman	0.013	0.0102	0.0089	0.078	0.0099
Toffoli	--	0.0067	0.0045	0.0026	0.0034

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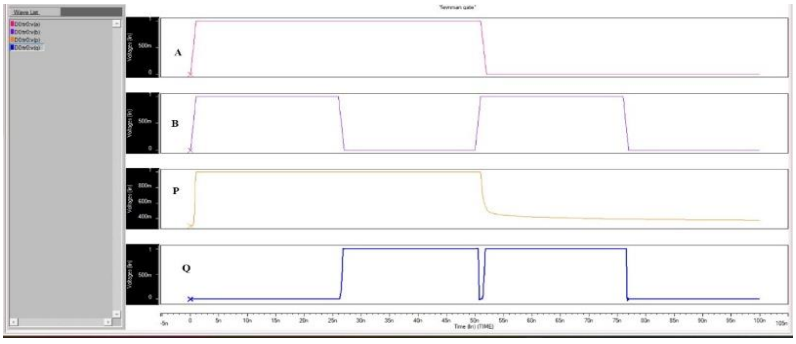
Fredkin	0.087	0.048	0.038	0.037	0.0525
Peres	1.79	149	1.34	1.22	1.46
DKG	7.33	6.76	6.67	0.095	5.21
Sayem	--	6.44	6.45	6.46	4.83

Table 8: Comparison of power dissipation in 16 nm technology (uW)

Gate	0.7V	0.8V	0.9V	1.0V	Average
Feynman	1.662	3.071	4.894	7.138	4.191
Toffoli	--	1.001	1.107	1.416	0.881
Fredkin	0.197	1.207	4.023	7.318	3.186
Peres	0.096	0.17	0.24	0.32	0.206
DKG	0.042	0.069	0.112	4.64	1.215
Sayem	--	0.162	0.165	0.168	0.143



(a)

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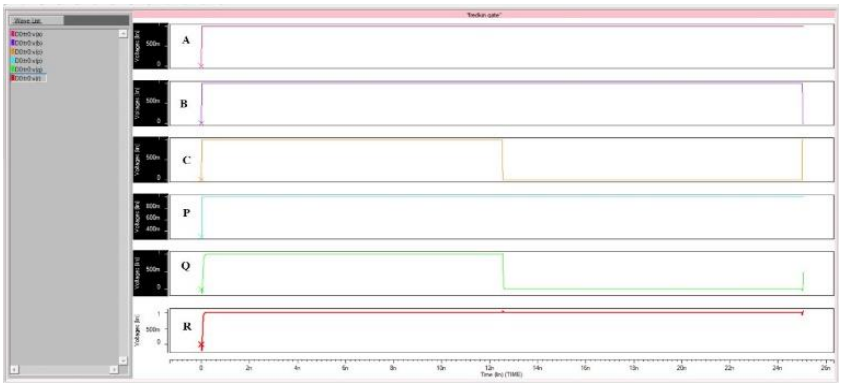
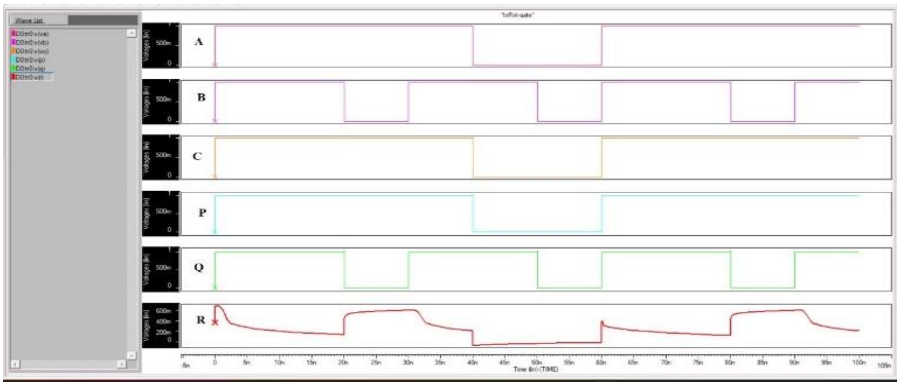


(b)



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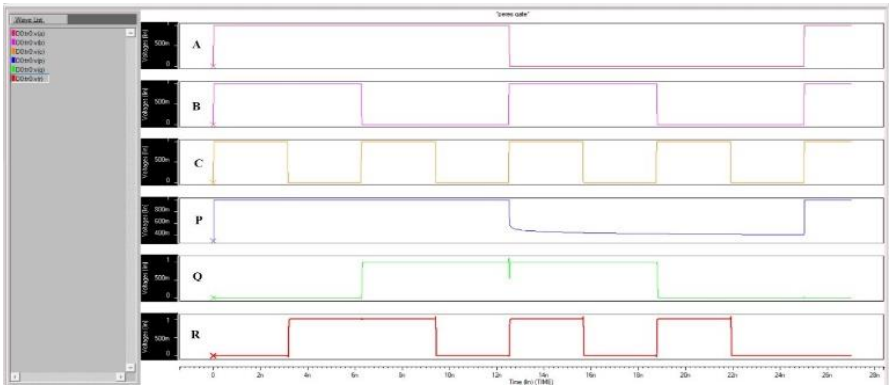

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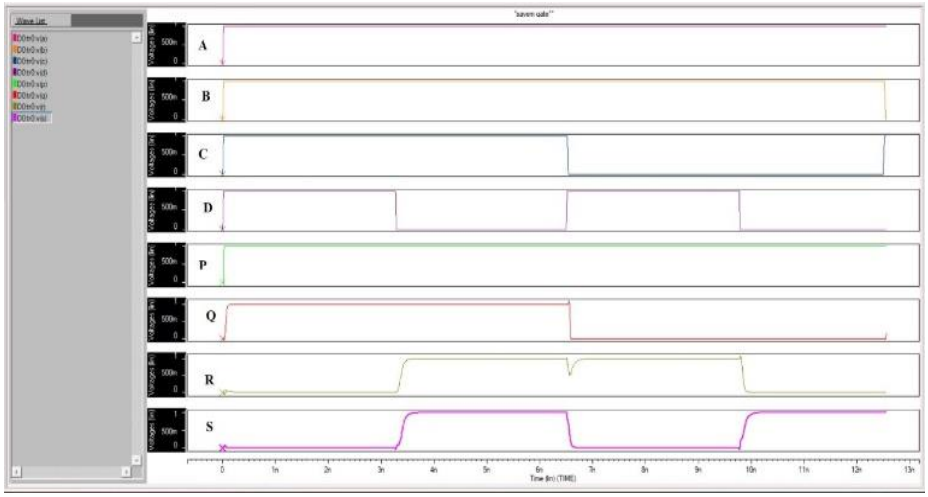
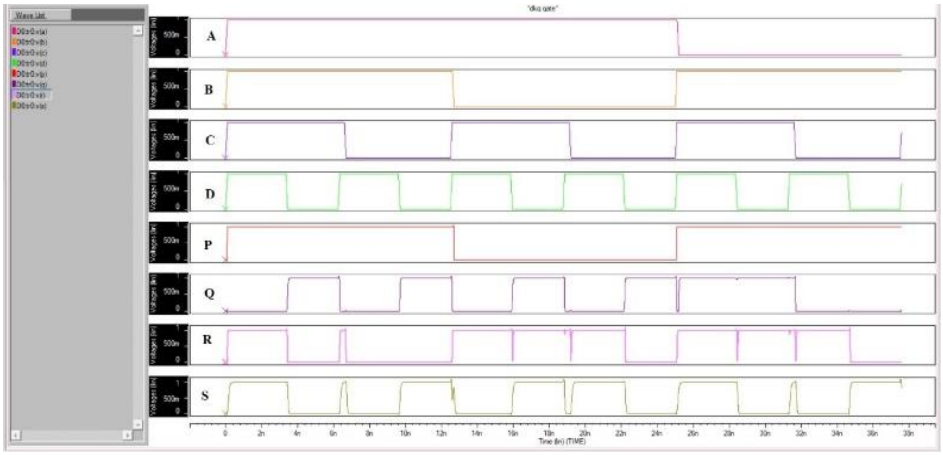


(e)



(f)

Fig. 7: Simulation waveforms for the **a** Feynman gate, **b** Fredkin gate, **c** Toffoli gate, **d** Peres gate, **e** Sayem gate, **f** DKGgate

5. PROPOSED SRAM CELLS

By observing comparison tables, we have got less delay for Feynman gate but Feynman gate can perform only hold operation. So, we require read and write operation also for this we have used Fredkin gate.
In power dissipation table Peres gate has consumed less power than any other gates. So, we have proposed two SRAM gates one is w.r.t delay (SRAM using Fredkin and Feynman gates) and other w.r.t power (SRAM using Peres gate).

6. BLOCK DIAGRAM OF EXISTING SRAM CELL USING FREDKIN AND FEYNMAN GATES

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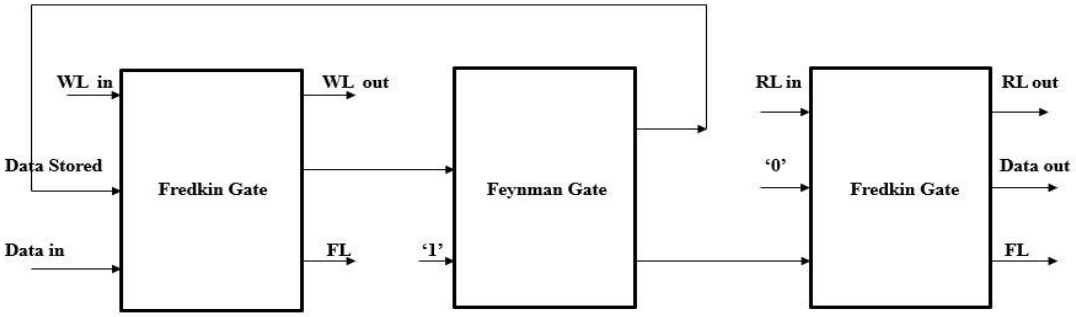
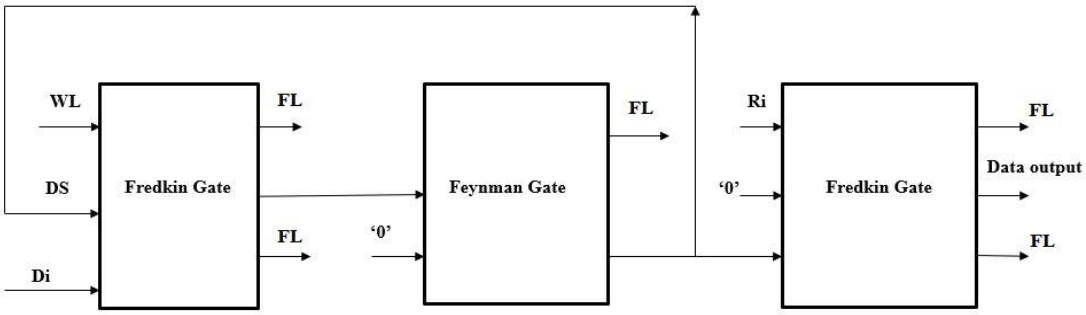
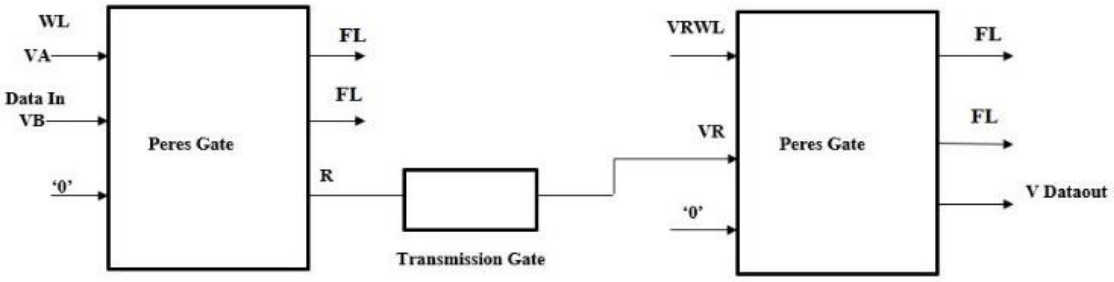


7. BLOCK DIAGRAM OF PROPOSED SRAM CELL USING FREDKIN AND FEYNMAN GATES



8. BLOCK DIAGRAM OF PROPOSED SRAM CELL USING PERES GATE



9. OPERATION OF EXISTING SRAM CELL USING FREDKIN AND FEYNMAN GATES

When WL=‘1’ and RL=‘0,’ the output of the frstFredkin gate is the same as that of the data input, which is stored in the bufer of the Feynman Gate, thus achieving the write operation. Thus, at WL=‘1,’ SRAM can be said to be in write mode. When WL=‘0’ and RL=‘1’ are fed as the input to the second Fredkin gate, the inverse of the data is stored in the Feynman gate. This Fredkin gate gives the same input as the data output. Thus, at RL=’1,’ SRAM can be said to be in read mode. When WL=‘0’ and RL=‘0,’ SRAM is said to be in hold mode. Previously stored data are held in the SRAM.

10.OPERATION OF PROPOSED SRAM CELL USING FREDKIN AND FEYNMAN GATES

When WL= ‘1’ and RL= ‘0’ the output of the first Fredkin gate is the same as that of the data input, which is stored in the buffer of the Feynman Gate, thus achieving the write operation. Thus, at WL= ‘1’ SRAM can be said to be in write mode. When WL= ‘0’ and RL= ‘1’ are fed as the input to the second Fredkin gate, the inverse of the data is stored in the Feynman gate. This Fredkin gate gives the same input as the data

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output. Thus, at RL= '1' SRAM can be said to be in read mode. When WL= '0' and RL= '0' SRAM is said to be in hold mode. Previously stored data are held in the SRAM.

11.OPERATION OF PROPOSED SRAMUSING PERES GATE

When WL= '1' and RL= '0' the output of the first Peres gate is the same as that of the data input, which is stored in the transmission gate, thus achieving the write operation. Thus, at WL= '1' SRAM can be said to be in write mode. When WL= '0' and RL= '1' are fed as the input to the second Peres gate, the inverse of the data is stored in the transmission gate. This Peres gate gives the same input as the data output. Thus, at RL= '1' SRAM can be said to be in read mode. When WL= '0' and RL= '0' SRAM is said to be in hold mode.Previously stored data are held in the SRAM.

12. RESULTS

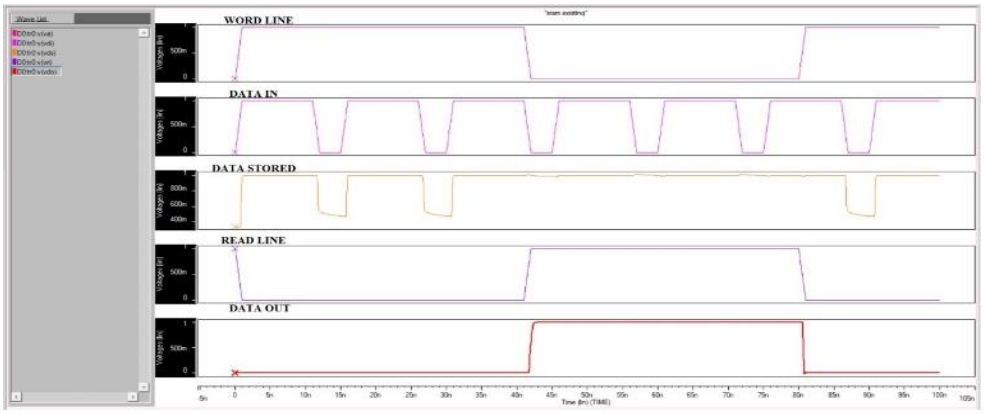

Fig. 8: Transiant analysis of Existing SRAM cell using Fredkin and Feynman gates

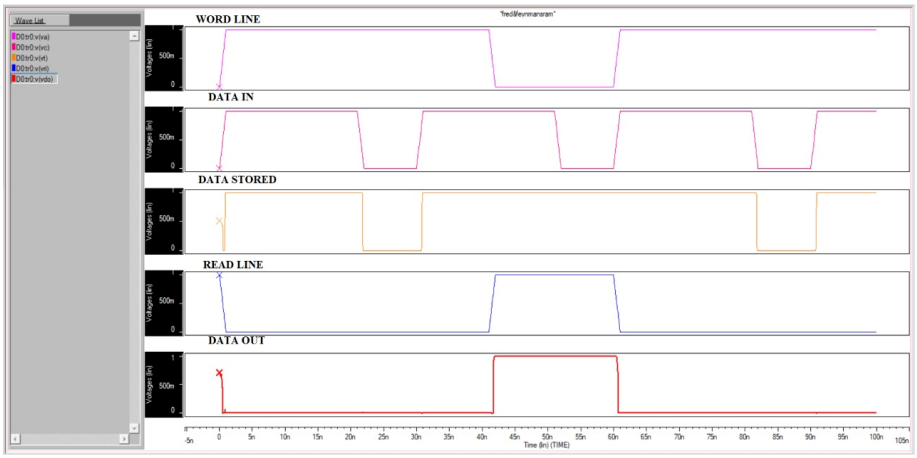

Fig. 9: Transiant analysis of Proposed SRAM cell using Fredkin and Feynman gates

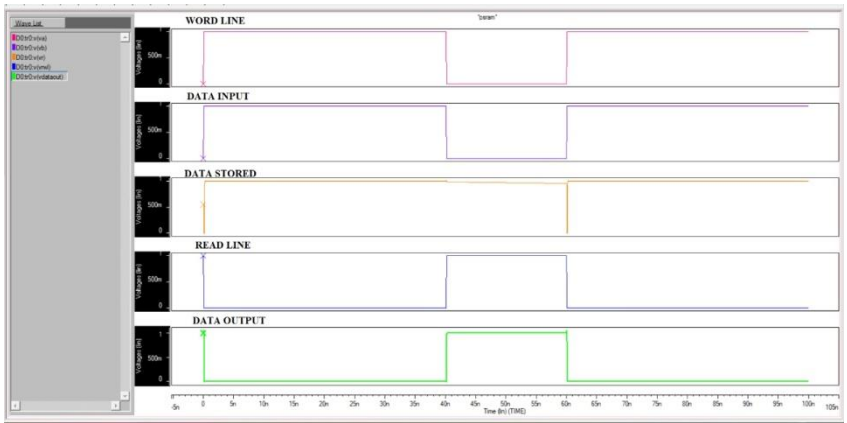

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Fig. 10: Transiant analysis of Proposed SRAM cell using Peres gate

13. COMPARISON OF POWER DELAY PRODUCT(FJ) OF WRITE OPERATION

SRAM	0.7V	0.8V	0.9V	1.0V	Average
Existing SRAM cell using Fredkin and Feynman Gates	0.475	0.377	1.252	0.436	0.635
Proposed SRAM cell using Fredkin and Feynman Gates	0.131	0.179	0.311	0.542	0.290
Proposed SRAM cell using Peres Gate	0.407	0.522	0.623	0.777	0.582

14. COMPARISON OF POWER DELAY PRODUCT(FJ) OF READ OPERATION

SRAM	0.7V	0.8V	0.9V	1.0V	Average
Existing SRAM cell using Fredkin & Feynman Gates	0.169	0.108	0.197	0.335	0.202
Proposed SRAM cell using Fredkin & Feynman Gates	0.609	0.096	0.085	0.118	0.092
Proposed SRAM cell using Peres Gate	0.340	0.455	0.464	0.512	0.442

CONCLUSION

Reversible logic gates such as Feynman Gate, Fredkin Gate, Toffoli Gate, Peres Gate, Sayem Gate, DKG Gate were implemented using Hspice. By comparing all the parameters like delay and power dissipation it is observed that Fredkin and Feynman having less delay and Peres has low power. So, a SRAM cell using Fredkin and Feynman Gates and SRAM cell using Peres Gate was proposed. The proposed SRAM cell using Fredkin and Feynman Gates and SRAM cell using Peres Gate has shown better results compared to the existing SRAM cell.

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