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DESIGN AND IMPLEMENTATION OF KOGGE-STONE PARALLEL PREFIX ADDER ARCHITECTURE USING LABVIEW

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ABSTRACT

In recent technologies of Electronics applications, Adder is an important source of any devices such as DSP, VLSI applications. For which, many electronics application devices used the high-speed adders namely Parallel Prefix Adder (PPA). Generally, PP Adders have less delay due to its less waiting time of carry for next addition. This paper is to design 16-kogge stone adder. Kogge stone adder is one of the parallel prefix adder. Kogge stone adder is a parallel prefix form carry look ahead adder. It generates carry in O (logn) time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In Kogge stone adder, carries are computed fast by computing them in parallel.

Keywords: *parallel prefix adder, carry look ahead adder, carry propagation delay.*

I. INTRODUCTION

The fundamental operations involved in any Digital systems are addition and multiplication. Addition is an indispensable operation in any Digital, Analog, or Control system. Fast and accurate operation of digital system depends on the performance of adders. The main function of adder is to speed up the addition of partial products generated during multiplication operation. Hence improving the speed by reduction in area is the main area of research in VLSI system design. Over the last decade many types of adder architectures were studied, such as carry ripple adders, carry skip adder, carry look ahead adder, parallel prefix tree adders etc. In tree adders, carries are generated in parallel and fast computation is obtained at the expense of increased area and power. The main advantage of the design is that the carry tree reduces the number of logic levels (N) by essentially generating the carries in parallel. The parallel-prefix tree adders are more favorable in terms of speed due to the complexity O(log2N) delay through the carry path compared to that of other adders. The prominent parallel prefix tree adders are Kogge-Stone, Brent-Kung, Han-Carlson, and Sklansky.

Out of these, it was found from the literature that Kogge-stone adder is the fastest adder when compared to other adders. The adder priority in terms of worst-case delay is found to be Ripple-Carry, Carry-Look Ahead, Carry-Select and Kogge-Stone. This is due to the number of “Reduced stages”. Kogge Stone adder implementation is the most straightforward, and it has one of the shortest critical paths of all tree adders. The drawback with the Kogge-Stone adder implementation is the large area consumed and the more complex routing (Fan-Out) of interconnects.

In Very Large-Scale Integration (VLSI) designs, Parallel prefix adders (PPA) have the better delay performance. A parallel prefix adder involves the execution of the operation in parallel which can be obtained by segmentation into smaller pieces. The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research continues increasing the adder’s delay performance.

The Kogge-Stone adder concept was described by two American computer engineers and scientists Peter M. Kogge and Harold S. Stone in their paper "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations" in 1973.In computer systems and technologies, the Kogge-

Stone adder is a parallel prefix form carry look-ahead adder. Other parallel prefix adders are the Brent-Kung adder, the Han- Carlson adder and the fastest known variation, the Lynch- Swartzlander spanning tree adder. The Kogge-Stone adders need more area to be implemented than the Brent-Kung adders, but have a lower fan-out at each stage, which increases performance for typical CMOS process nodes (the main advantage). However, wiring congestion is often a problem for Kogge-Stone adders. It is one of the parallel adder & used to add two binary numbers in parallel form. A parallel adder is a combinational circuit & has fast speed compared to serial adder. The addition process is carried out simultaneously that implies all bits sum up simultaneously.

II. LITERATURE REVIEW

The most objective of this paper is Quantum dot cellular automata (QCA) is used to get economical styles for the ripple carry adder (RCA) and varied prefix adders. The amount of majority gates for n-bit RCA and n-bit Brent-Kung can sure on adders. Signal integrity and strength studies show that the planned Brent-Kung adder is fairly well-suited to changes in time. It's going to undergone varied method steps of design rule, simulation engine, layout level implementation and study of signal integrity with reference to time. Thought of primitives in QCA and developed several results concerning majority logic optimization. It will perform the operation on add current bits once carry generation from previous bits solely. This paper uses the strategy as use of Brent- Kung Adders in QCA.

In carry select adders (CSLAs). employing a single ripple carry adder and a primary zero finders (FZF) circuit rather than twin ripple carry adder. It's a powerful impact on reduction of range of transistors then power consumption of adder. A 64-bit static adder with structure of hybrid CLA/CSLA is conferred that operates with low power and space compared to standard CSLA. This circuit is enforced in TSMC 0.18μm CMOS technology at one.8V power provide. Essential path delay of this adder decreased to 592ps, comparable to seven.6 FO4 (fanout-of-4) electrical converter delays. It will perform the operation by assumptive carry is one or zero addition is preprocessed. This paper uses the strategy of static hybrid carry-look ahead/carry- choose adder.

In Binary addition ripple carry adders square measure replaced by the parallel prefix adder to decrease the delay. Parallel prefix adder could be a technique for raising the speed of the addition. They provide an honest theoretical basis to create a good vary of style tradeoffs and it's a lot of fitted to adders with wider word lengths. Han-Carlson Adder is introduced that uses completely different stages of Brent -Kung and Kogge-Stone adders. The proposed style reduces of prefix operation by victimization a lot of number of Brent-Kung stages that reduces the quality, semiconductor space and power consumption significantly. The operation undergone during this technique is that once high operation speed is required. tree structures like parallel-prefix adders square measure used. The strategy employed in this technique is Parallel Prefix Adder in Associate in Nursing FPGA.

Perform computation that any previous state can perpetually be reconstructed given an outline of the present state. Simulation results of forward & backward computation of 4*4 reversible TSG & Fred kin gate. The gate is then wont to design four bit Carry Skip Adder block. The adder design designed victimization TSG & Fredkin gate square measure abundant optimized as compared to existing four bit Carry Skip Adder in terms of low power dissipation. Methodology used for coming up with reversible gate is Tanner Tool Version 13 & technology file zero.35 micron. The operation that undergone is that the method of carry- skip adder (also familiar as a carry-bypass adder) is adder implementation that improves on the delay of a ripple-carry adder. The strategy employed in this method is Carry skip adder victimization TSG &amp, Fred kin reversible gate.

Reversible logic is gaining important thought because the potential logic style for implementation in fashionable engineering and quantum computing. They are implemented with marginal impact on physical entropy. a unique programmable reversible computer circuit is conferred verified and its implementation within the style of a reversible ALU is incontestable. Implementations of the Kogge-

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Stone adder with sparsity-4, eight and sixteen were designed, verified, and compared. The improved sparsity 4.

Kogge-Stone adder with ripple-carry adders was selected and it's enforced within the design of a 32-bit ALU is incontestable. Like the carry-skip adder. however, computes generate signals additionally as cluster propagate signals to avoid looking ahead to a ripple to see if the cluster generates a carry. The strategy used is increased carry look-ahead adder for novel reversible ALU.

III. PROPOSED SYSTEM

3.1. PARALLEL PREFIX ADDERS

Parallel Prefix Adders can be built in many ways based on the number of levels of the logic, number of logic gates involved, number of the fanout from each gate and the number of wirings between the levels. The three fundamental Tree adders are Brent-Kung, Sklansky and Kogge Stone architectures. The most commonly used Tree (Parallel Prefix) Adders are.

1. Brent Kung
2. Sklansky
3. Kogge Stone
4. Han Carlson
5. Knowles
6. Ladner-Fische

The steps illustrated above are as shown in Fig 1.

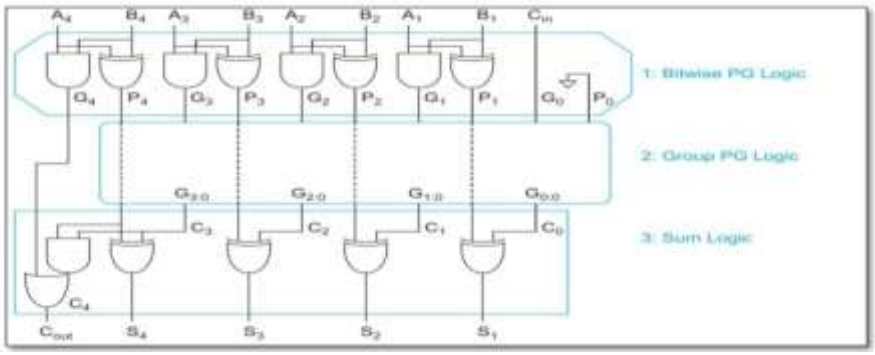

Fig 1. Parallel Prefix Adder Stages

3.2. BACKGROUND INFORMATION OF KSA

The Kogge-Stone adder is a parallel prefix form of carry look-ahead adder. It generates the carry signals in O(log2N) time and is widely considered as the fastest adder design possible. It is the most common architecture for high-performance adders in industry. The Kogge-Stone adder concept was first developed by Peter M. Kogge and Harold S. Stone. In Kogge-stone adder, carries are generated fast by computing them in parallel at the cost of increased area. The Kogge Stone Adder (KSA) has regular layout which makes them favoured adder in the electronic technology. Another reason the KSA is the favoured adder is because of its minimum fan-out or minimum logic depth. As a result of that, the KSA becomes a fast adder but has a large area. The delay of KSA is equal to log2n which is the number of stages for the "o" operator. The KSA has the area (number of "o" operators) of (n*log2n)-n+1 where n is the number of input bits.

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3.3. ARCHITECTURE OF KSA

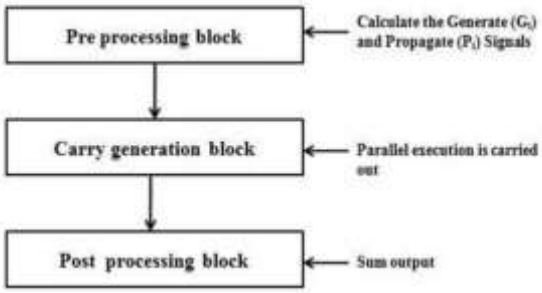

Fig 2. Architecture of KSA

3.4 THREE STAGES OF KOGGE STONE ADDER

The complete functioning of KSA can be easily comprehended by analysing it in terms of three distinct parts:

Pre processing

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \cdot B_i$$

2. Carry look ahead network

This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equation below:

$$G_i = (P_i \cdot G_i^*) + G_i$$
$$P_i = (P_i \cdot P_i^*)$$

3. Post processing

This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

$$C_i = G_i$$
$$S_i = P_i \oplus C_{i-1}$$

3.5 SCHEMATIC OF KSA

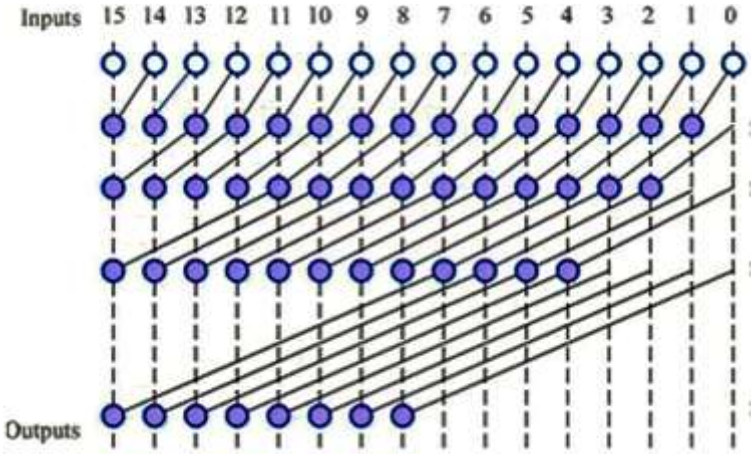

Fig 3.Schematic of KSA

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IV. EXPERIMENTAL RESULTS

Primitive Component	Delay(ns)	Area	Power (W)
4-bit carry ripple adder	72.1	160	0.8745784
8-bit carry ripple adder	72.1	160	0.8745784
16-bit carry ripple adder	72.1	160	0.8745784
4-bit carry look-ahead adder	93.54	288	1.049
8-bit carry look-ahead adder	118.9	302	1.1627
16-bit carry look-ahead adder	124.3	310	1.1757
2-level 8-bit carry look-ahead adder	31.57	434	1.348
4-bit carry select adder	24.72	422.5	1.6351
8-bit carry select adder	20.48	394.5	1.5757
16-bit carry select adder	26	356.5	1.4792
16-bit Brent-Kung prefix adder	26.94	290	1.15
16-bit Han-Carlson prefix adder	25.43	326	1.2758
16-bit Kogge-Stone prefix adder	25.59	428	1.5546

STIMULATION RESULTS

A=1001100110011001
B=0101010101010101
Cin=0

A=1001100110011001
B=0101010101010101
Cin=1

A=111110011001100
B=1111110101010101
Cin=0

A=1111100110011001
B=1111110101010101
Cin=1

V. CONCLUSION

This paper presents a 16-bit KSA was verified using LabVIEW. Power analysis was carried out and was compared with the classical 16-bit ripple carry adder and the results were very impressive. It was found out that KSA has better power optimization than the ripple adder but there is a trade off with the area as the KSA consumed large amount of chip area. The number of stages consumed by KSA is very impressive as it just uses 3 stages as compared to the ripple adder which uses 7 stages. Hence the delay is reduced. The speed of computation is very high in KSA compared to the ripple adder. The 16-bit KSA was also verified using LabVIEW output observed with a particular example.

This differs from the results, where the parallel-prefix adders, including the Kogge-Stone adder, always exhibited inferior performance compared with the RCA. Kogge Stone Adder is the fastest adder which focuses on design time and is said to be a good alternative for high performance applications. The speedy nature of Kogge Stone Adder is because of minimum logic depth and restricted fan-out. In KSA, parallel advance will give scope to generate fast carry for intermediate stages.

For future work, the design can be further enhanced for 32-bit as well 64-bit. Even other design variants can also be tried for even better analysis. In fact, by combining the various tree adders as well as the technology used to implement them, a very suitable adder with significant less delay can be achieved.

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