Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

ANALYSIS OF 16-BIT COUNTER USING GDI TECHNIQUE WITH CLOCK GATING

P.NAGA SAILAJA PG Student, Dept of ECE, SITS, Kadapa.
N.NAGA MALLIKARJUNA Associate Professor, Dept of ECE, SITS, Kadapa.
R.L.B.R.PRASAD REDDY Associate Professor, Dept of ECE, SITS, Kadapa.

Abstract –

This project presents the simulation of a 16-Bit Counter using CMOS logic and GDI technique.Gate diffusion input logic is a technique to design low power digital circuits that is used to reduce transistor count and power delay product of the digital circuits. The 16-bit counter is designed by using master-slave flip-flop based on GDI technique. In this approach conventional CMOS counter and GDI based counter has been analyzed in terms of delay, power consumption and power delay product. All these parametric analyses had been carried out using Tanner CAD tool with varying supply voltage from 0.8V to 1.8V. The analysis showed that GDI based counter is more suitable for low power application as a counter.

I. INTRODUCTION

A Flip-Flop itself a circuit that gives either zero or one as a stable state of the Flip-Flop. It is widely used for storing the information. In sequential logic, Flip-Flop is used as a basic storage element. Scaling circuit is an electronic device that stores the number of times that the process or event has occurred in relation with the clock signal. It is used for counting the number of pulses coming at the input line in a specific time period. The design which consumes lesser power with maximum reliability is almost important especially when it uses clock. Thus, the power of the circuit is minimized by decreasing the dissipation of power in the clock. In Complementary Metal-Oxide Semiconductor VLSI design, the basic classification of counters is synchronous and asynchronous counter and this classification depends on clock triggering.

Counting is the most commonly used operation in real time DSP applications. The counter is designed with the help of flip flop circuits. The energy consumption of flip flops plays an important role in sequential design. The important factors for designing sequential circuits are energy consumption and delay. The energy consumption of counter is improved by using GDI technique. In this chapter the design of low power counter using GDI technique is focused. GDI based counter circuits are analyzed and compared to select the suitable sequential circuits for low power applications. The GDI technique is based on the use of a simple cell as shown in figure. The GDI cell contains three inputs- G (gate input is common for both PMOS and NMOS, P (Input to the source/drain of PMOS), and N (Input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P, so it can be arbitrarily biased in contrast to CMOS inverter.

II. DESIGN METHODOLOGY

The Flip-Flop is designed using the method of True Single Phase Clock. The main objective of using TSPCL is to perform the operation of the required Flip-Flop that consumes minimum power and also operates with maximum speed.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

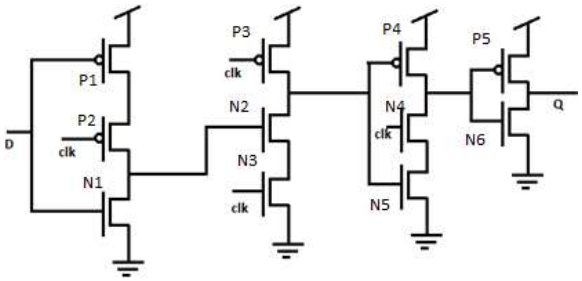

Figure: D Flip-Flop Design using TSPCL

Fig gives the design of D Flip-Flop with TSPCL. Consider when D is 0 and CLK is low, the transistor P1 andP2 is active which in turn activates the transistor N2 of the next stage. Here P3 of this stage is active and gives 1 which is inverted and gives 0. Similarly the given input of D gets inverted in every stage and it produces the output same as the input.

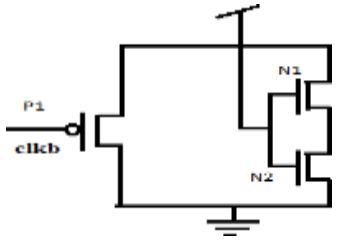

Figure: Upper SVL Design

The upper SVL consists of two NMOS connected in series with a parallel PMOS. The gate of the two NMOS connected to the supply and the input clock bar is given to PMOS. When the clk is 1, clkb becomes 0 and PMOS gets ON. Thus the PMOS starts conducting and the supply voltage 1 can pass through hit. When the clk is 0, clk b becomes 1 then the two NMOS starts conducting and are connected to the ground. By connecting the NMOS in series the leakage power can be reduced while the circuit is in off condition Figure gives the design of Upper SVL.

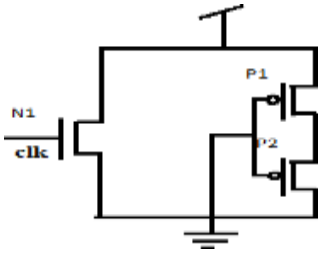

Figure: Lower SVL Design.

The lower SVL consists of two PMOS connected in series with a parallel NMOS. The gate of the two PMOS connected to the ground and the gate of the NMOS is connected to the input clock. When the clk becomes 1 and NMOS gets OFF. Thus the PMOS starts conducting and they are connected to the ground. When the clk becomes 0the two NMOS starts conducting and the supply voltage 1can pass through it. When PMOS are connected in series it makes the circuit to reverse bias that causes the standby mode leakage current to be reduced. Figure gives the design of Lower SVL. A recital CMOS D Flip-Flop circuit which is comprehensively used in analog and digital systems. In CMOS technology leakage power is primary significance. To reduce power dissipation and to increase the battery lifetime, the supply voltage should be reduced when the circuit is in off state. Modified SVL technique is applied to CMOS D Flip-Flop circuit, which suppresses the signals and reduces power dissipation because of leakage currents. The consumption of dynamic power is also reduced as minimum number of transistors is used in the modified design.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

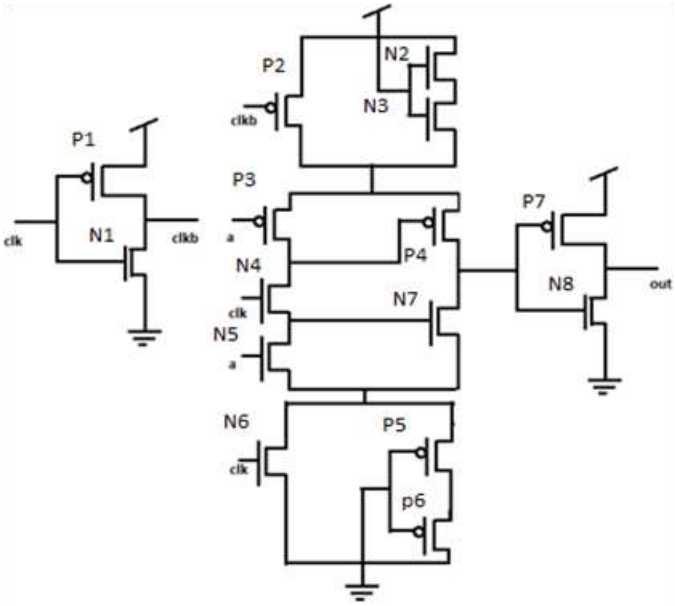

Figure: Design of D Flip-Flop with Modified SVL.

P1 is ON, N2 is ON, P2, P3 are OFF, N1 and N2 are inactive. In order to perform the normal D Flip-Flop operation, it is connected to supply and GND. When a is inactive, P1, N1, N3 are active and P2, N2 are inactive so that out becomes inactive. When a is 1, which makes P1, N3to in active state while makes N1, N2 and P2 active state, that is out becomes one. P1, N3 are in OFF state i.e. open circuits. N1, N2 are active but as the supply voltage it gives Vdd-Vth because they acts as a pull-up network. When the NMOS transistors reconnected in series it reduces the static power. P2, P3 are active but they gives finite positive voltage as a replacement of GND because they acts as a pull down network. As the NMOS transistors are used in series it reduces supply voltage and also reduces leakage current during standby mode. The reduction of leakage power is very much concerned as it is proportional to the current and supply voltage. This designal so has an advantage of increasing the operational speed of the circuit and also reduces the consumption of dynamic.

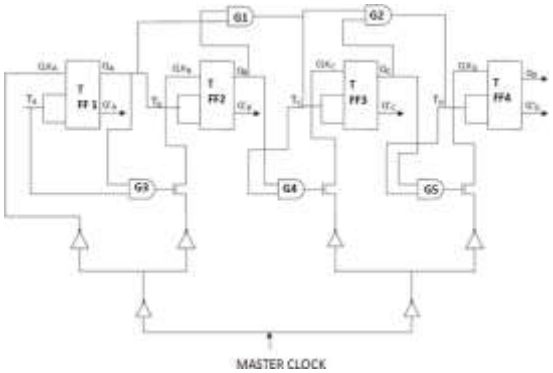

Figure: Block diagram of 4-Bit Existing Binary Up Counter

This design is applicable for wide range of bits. The Flip-Flop receives the clock signal from the clock network. This network consists of repeaters in series and eliminates clock skew. The circuit has a benefit of minimum power consumption in the clock network by introducing a combinational logic that mastery the clock based on the Flip-Flop activity. So, by avoiding the unwanted activity of clock at the inactive Flip-Flop, the power could be optimized. Fig gives the design of 4-Bit Existing Binary Up Counter.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

Research Method of Flip-Flop and Counter Design

The proposed design uses the positive edge triggered Flip-Flop. In comparison with the conventional Flip-Flop this TSPCL combined with SVL technique consumes less power.

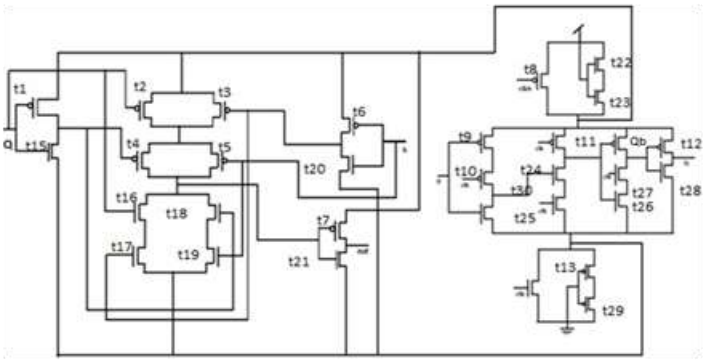

Figure: Design of Proposed T Flip-Flop with Combined SVL.

Fig represents the design of projected T Flip-Flop design with combined SVL. P1 is ON, N2 is ON, P2, P3 are OFF, N1 and N2 are inactive. In order to perform the normal D Flip-Flop operation, it is connected to supply and GND. When a is inactive, P1, N1, N3 are active and P2, N2 are inactive so that out becomes inactive. When a is1, which makes P1, N3to inactive state while makes N1, N2and P2 active state, that is out becomes one. P1, N3 are in OFF state i.e. open circuits. N1, N2 are active but as thesupply voltage it gives Vdd-Vth because they acts as a pull-up network. When the NMOS transistors re connected in series it reduces the static power. P2, P3 are active but they gives finite positive voltage as are placement of GND because they acts as a pull down network. As the NMOS transistors are used in series it reduces supply voltage and also reduces leakage current during standby mode. TSPCL consists off our stages of inverter. The input gets inverted in each stage and the final output of the TSPCL is same as that of the input. The operation of the TSPCL functions according to the clock signal.

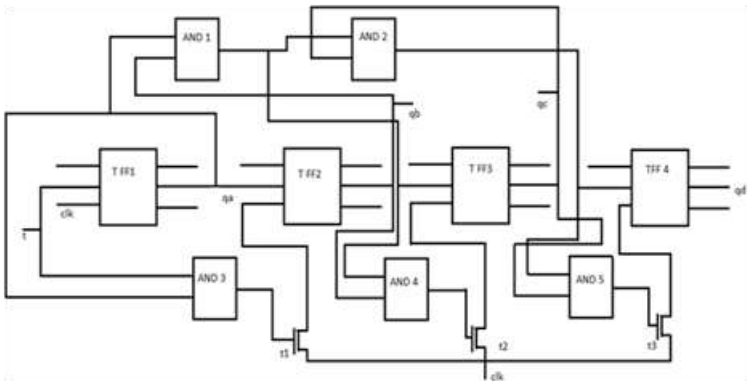

Figure: Proposed Counter Design using modified Flip-Flop.

A cascade T Flip-Flop structure is used in this system. The reason for using T Flip-Flop is it concerns for the changing activity of next state. It eliminates the clock transition when the input of T Flip-Flop is zero. When the clock is zero it does not affect the output of the circuit and in turn maintains the previous state output whereas the output gets toggled when the clock is one. So, it is evident that the clock acts as a control signal for the counter. The block diagram of proposed counter is shown in Figure.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

III. RESULTS

All the designs are simulated using 250nm CMOS technology library in Tanner EDA TOOL at various supply level voltages.

Existing waveforms:


```
General options:
         search =                    threads = 2

 Device and node counts:
              MOSFETs -      140
    MOSFET geometries -        3
      Voltage sources -        3
          Subcircuits -       16
    Model Definitions -        6
      Computed Models -        2
    Independent nodes -       84
       Boundary nodes -        4
          Total nodes -       88
*** 1 WARNING MESSAGE GENERATED DURING SETUP


Power Results

VV1 from time 0 to 1.8e-007
Average power consumed -> 1.081279e-007 watts
Max power 2.845913e-004 at time 1.35812e-007
Min power 0.000000e+000 at time 0

VV2 from time 0 to 1.8e-007
Average power consumed -> 1.832177e-005 watts
Max power 6.581973e-003 at time 1.00916e-008
Min power 0.000000e+000 at time 0
```

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

Proposed waveforms:


```
General options:
         search =                    threads = 2

 Device and node counts:
              MOSFETs -      234
    MOSFET geometries -        7
      Voltage sources -        3
          Subcircuits -       31
    Model Definitions -        6
      Computed Models -        2
    Independent nodes -      113
       Boundary nodes -        4
          Total nodes -      117
*** 1 WARNING MESSAGE GENERATED DURING SETUP
```

```
Power Results

VV1 from time 0 to 1.7e-007
Average power consumed -> 3.548171e-006 watts
Max power 1.908272e-002 at time 4.25e-011
Min power 0.000000e+000 at time 0

VV2 from time 0 to 1.7e-007
Average power consumed -> 2.987520e-005 watts
Max power 8.093225e-003 at time 1.551e-007
Min power 0.000000e+000 at time 0
```

CONCLUSION

The consumption of power in the counter is minimized by using the proposed T Flip-Flop with clock gating technique. The T Flip-Flop is proposed by combining TSPCL and SVLtechnique.TheproposedTFlip-Flopusesonly0.34microwatt power which is 30% less than the existing T Flip-Flop design. The proposed counter design consumes 27%less power compared to the existing counter design. The projected T Flip-Flop and counter is designed and simulated using the Tanner Tool which employs 250nm CMOS technology. The proposed counter reduces power consumption and chip area which maximizes the battery life and performance of the system. Thus, it is witnessed that the combination of TSPCL, Upper and Lower SVL can be used to design the low power consuming Flip-Flop used in the construction of counters. The design is proposed only for 4bit up-counter, the work can also be extended for the design of low power consumed wide bit counters. This project gives only the power comparison result of Flip-Flop and counter design, area analysis and delay analysis of Flip-Flop and counter design at different Supply Voltage can also be done. Comparing to existing counter, the projected counter design utilizes 27% less power. The future work is to further minimize the power consumption of counter comparing to the proposed power of counter design.

REFERENCES

[1] Adler, V. and E.G. Friedman, 1997.Delay and power expressions for a CMOS inverter driving a resistive-capacitive load. Analog Integrate. Circuits Signal Process, vol.14, pp. 29–39.

[2] Chang, C. H., J. Gu and M. Zhang, 2005. A review of 0.18um full adder performance for tree structured arithmetic circuits, In: IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.13, No. 6, pp.686-695.

[3] Hu, J., X. Yu and J. Chen, 2011.New Low–leakage Flip-flops with Power-gating scheme for Ultra-low power Systems, Information Technology Journal, 10:2161-2167.

[4] Kang, S.M.S., 2003. Elements of low power design for integrated systems. Proceedings of the International Symposium on Low Power Electronics and Design, August 25-27, ACM, New York, USA. 2003, pp: 205-210.

[5] Markovic, D., B. Nokolic and R.W. Brodersen, 2001. Analysis and design of low-energy flip-flops. In: International Symposium on Low Power Electronics and Design, August 6-7, 2001, Huntington Beach, CA. USA., pp. 52-55.

[6] Marimuthu, C.N. and P. Thangaraj, 2010. Low power multiplier design using latches and flip-flops. In:J.Comput. Sci., 6: 1117-1122.
[7] Morgenshtein.A., A. Fish, I.A. Wagner, 2002.Gate-Diffusion Input (GDI) – A Power Efficient Method for Digital Combinatorial Circuits. In: IEEE Trans. VLSI, 10(6): 566-581.
[8] Sakurai, T., 1993. Closed form expressions for interconnection delay, coupling and crosstalk in VLSI. IEEE Trans. Electron Devices, vol. 40: 118–124.
[9] Weste.N and K. Eshraghian., 1993.2nd Edition Principles of CMOS digital design. Reading, MA: Addison-Wesley, pp. 304–307.
[10]Callaway, T & Swartzlander, E 1996, 'Low Power Arithmetic Components', IEEE in Low Power Design methodologies',Norwell,MA: Kluwer,pp.161-201.
[11]Lee, PM, Hsu, CH &Hung,YH 2007, 'Novel 10T full adders realizedby GDI technique', IEEE International Symposium on Integrated Circuits , pp.115-118.