Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

Design of Low Quiescent LDO with OTA for Portable Device Applications

A SATHVIK, K PRABHU

Abstract— Power management integrated circuits (ICs) are essential in modern electronic systems to ensure a stable, regulated voltage supply across various load conditions, free from any irregularities.

Biomedical devices, in particular, have stringent and reliable power requirements due to their sensitivity to external noise. Additionally, portable devices powered by batteries face constraints in terms of available energy. As a result, the primary objective of this thesis is to design a low-quiescent current, low-dropout voltage regulator (<10 µA) that can handle up to 1 mA of load current, ensuring reliable operation under all conditions. This is achieved by employing a combination of three current mirror operational transconductance amplifiers (OTAs) and an additional buffer stage to minimize quiescent current consumption.

Index Terms—Low dropout regulator, Output Transconductance Amplifier, Power management IC.

I. INTRODUCTION

A. VOLTAGE REGULATORS

An essential part of a power management system is a voltage regulator. They serve to maintain a steady and steady voltage regardless of variations in line voltage and load demands. The raw line voltage is restless, noisy, and fluctuates in magnitude and frequency by nature. In a similar vein, an amplifier's load requirement and that of a digital signal processor differ. Therefore, conditioning the power supply is necessary for a device to work properly supplying clean and steady output to the load.

Bio medical signals generated from human body are very minute and more susceptible to noise. therefore, electronic devices designed for bio-medical applications need to be robust and noise free. Nowadays majority of bio-medical devices are designed for portability for used in implantable applications. Which monitor vitals entire day.[1]

Performance of portable devices majorly depends upon power management modules which is deciding factor its lifetime, noise resistant nature. To obtain a strictly regulated noise free clean voltage a LDO is employed[2]. to design a low dropout regulator defining of specifications based upon input signal bandwidth, noise resistant capabilities, operating voltage range should be narrowed down. We can decide specifications by overviewing characteristics of LDO from [3].

The core circuitry for LDO is an error amplifier which defines overall performance. here we implement widely used 3 current mirror OTA [5] as error amplifier as it is simple to stabilize due to its single dominant pole.

As we aim to design LDO for portable devices [8] which have limited power supply through battery, quiescent current [9] must be as low as possible to prevent current leak in idle mode.

Based to previous research works [10], LDO can be classified as output capacitor-based, Cap-less based LDO. Here we opt external capacitor based LDO which demands large capacitor at output node. We primarily focus on power saving techniques to minimize idle current as low as possible.

In previous research works two stage op-amp is used as error amplifier which acts as negative feedback to regulate transient changes of voltage according to current demands of load device. But it omits stability issues as it employs two stages resulting in extra pole which deteriorates phase margin of circuit. To overcome this, we utilize alternate topology using output transconductance amplifier.

Main advantage of OTA is that it contains less nodes than op-amp which cuts out unnecessary current branch nodes. The OTA offers high output impedance which is not feasible to drive Pass device therefore additional buffer circuitry is introduced.

B. LDO ARCHITECTURE

LDOs are linear regulators that can effectively control the input voltage with a substantially smaller voltage differential between the input and output. A standard LDO regulator structure is made up of a resistor feedback network, an error amplifier and a pass element. When the output is at its nominal value, the feedback network's resistive voltage divider provides a scaled output voltage equal to the reference voltage. The reference voltage and the voltage coming from the voltage divider are continuously compared by the error amplifier. To maintain the output voltage level at the required level, this discrepancy is amplified and the error amplifier's output

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

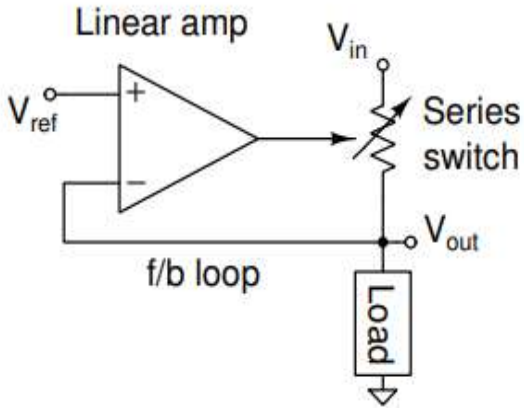

fig 1: basic LDO architecture powers the pass element.

1) The Voltage Reference

A voltage reference establishes the operating point of the error amplifier, making it the foundation for all regulators. Typically, this voltage reference is of the band-gap variety, as it can function effectively at low supply voltages, and its accuracy and stability across different temperatures are adequate for designing linear regulators.

2) The Error Amplifier

The differential input amplifier which constantly compares slacked off error signal with a reference voltage it is core circuit of entire LDO which determines overall performance. But contrarily the architecture of error amplifier needs to be as simple for decent stability under all load conditions. Additionally, as to guarantee the output's accuracy, the amplifier's bandwidth should be sufficient to respond quickly to changes in input voltages and load circumstances.

The biasing current and the error amplifier's performance (bandwidth, slew rate, etc.) are traded off in our attempt to minimize the quiescent current. As pass transistor occupy major portion in design it omits large capacitance due to its size to shift pole away from dominant pole, we design error amplifier op resistance as low as possible implying buffers if needed. To guarantee output accuracy, the DC open loop gain needs to be high under all load circumstances.

3) The Feedback Network

As output voltage is high, we extract only tiny portion of it to compare with reference. To setup voltage output required for load the divider ratio of R2/R1 is the design factor because of the constant VREF.

The quiescent current of the voltage regulator is affected by the current flowing through the divider. To minimize power consumption, the resistor values must be carefully selected to balance the load current and the current drawn by the error amplifier. For example, using resistors in the hundreds of kΩ range will produce a current in the microampere range when the error amplifier consumes 50 µA. To achieve lower quiescent current in such a case, the resistances would need to be in the megaohm range if the error amplifier's current draw is in the microampere range.

4) The Series-pass Element

In a feedback loop, the error amplifier drives the pass element, which transfers high currents from the input to the load. Although there are many different pass element topologies, only MOSFET pass elements will be discussed because the study is primarily concerned with the construction of an LDO in CMOS technology.

Since the PMOS pass element voltage VGS is connected to the regulator's Vdd supply rail, the minimum voltage needed for the pass transistor to remain in the saturation area and regulate correctly is provided by the minimum drain source voltage Vds. This equation defines the PMOS dropout voltage:

$$V_{dropout,PMOS} = V_{out} + V_{dsat,PASS} \quad [V]$$

If the pass transistor functions in the linear zone, the system's open-loop gain degrades, and regulator is deactivated if the input voltage drops below the dropout voltage, the precision of linear voltage regulators drops. The pass transistor's gate cannot be pulled below ground level, so for high output currents, either the pass device must be very large or the LDO's input voltage must be raised. In the end, the PMOS pass element gate voltage is moving toward ground as the load current increases.

5) *Output Capacitor*

During load transients, the output capacitor makes sure that the current is given to the load right away until the error amplifier catches up. Because it forms a low frequency pole and a zero at higher frequencies, it also plays a crucial part

in the system's stability.

The capacitor's Equivalent Series Resistance (ESR), which is represented as a resistance in series with a capacitor, is correlated with the zero. we use 1 uF capacitor's specified ESR range is 10 mΩ to 300 mΩ. This limits our options to using solely ESR capacitors in this range.

II. LDO DESIGN METHODOLOGY

The designing can be started from maximum and minimum load requirements as pass transistor need to handle worst case load current scenarios.

A. Feedback Voltage Divider

As the reference voltage from Bandgap circuit is fixed to 1.2V which is reference voltage to error amplifier. We need to extract portion of error signal from LDO output. This can be performed by simple voltager divider circuit. The GPDK90 library offers wide range of MOSFET acting as resistor in linear region. feedback factor can be determined by

$$\beta_{FB} = \frac{V_FB}{V_O} = \frac{1.2}{1.5} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = 0.8$$

Although the resistor ratio is known, the resistor values need to be chosen so that they consume less current and also plays a role in stability of entire circuit. We need to make sure resistance offered is high to ensure it draws low current.

B. Pass Element Design

We can determine that the maximum dropout voltage is 200 mV based on the input voltage range of 1.7 V to 2 V and the output voltage standard of 1.5 V. There are two pass devices available to us: PMOS and NMOS. Since the PMOS's saturation voltage VDS,sat is the only source of the minimum voltage required to maintain saturation, it has a far lower demand on the minimum input voltage. It might be feasible to employ NMOS if we so desired, but because to input voltage specifications, a charge pump would be required to increase the NMOS pass element's gate voltage to a level where it would be properly biased.

In addition to complicating our circuit, that would be inefficient in terms of power consumption because we have strict specifications about low quiescent current. Because of its low dropout voltage, the PMOS is ultimately the best option for our application.

We must now consider the maximum load current that will pass through our pass element since we have determined that it will be a PMOS device. According to the specification, the maximum load current is 1 mA with a 10% possible deviation, which adds up to 1.1 mA.

We will use the square-law equation for drain current to determine the minimal W/L ratio of the pass device since we want the pass transistor to remain in the saturation region under all load situations. Ignoring our channel length modulation

$$I_D = \frac{1}{2}\mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \Rightarrow \frac{W}{L} = \frac{I_D}{\frac{1}{2}\mu C_{ox} \cdot (V_{GS} - V_{TH})^2} \quad [A]$$

However, this value may vary significantly depending on temperature and process corners. The W/L ratio of pass device is made little large than calculated ratio for high load transients, if the ratio is too large then it affects stability due to large capacitance.

C. Buffer

Due to large pass transistor, it shows as capacitance. A significant parasitic capacitance Capacitive input protection (CIP) is added at the gate of the pass device due to the large gate area. Although the capacitance in this case is not high enough to create a slew-rate limitation, it still impacts system stability. This is because a high resistance ROE at the error amplifier's (AE) output node is necessary to achieve an adequate loop gain ALG .

The combination of ROE and CIP introduces a low-frequency pole, pOE , which can compromise system stability. To address this, a buffer amplifier AB is employed. For AB to effectively control the pass device, both turning it off and fully driving it under maximum load conditions, it must have a small capacitance at input, low impedance at output, and sufficient voltage swing at its output. As a solution, a PMOS source follower is chosen for the buffer amplifier.

However, because of how low its source-gate voltage can drop in relation to VIN, it may impede the PMOS pass device's dropout voltage.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

$$V_{DO} \propto \frac{1}{V_{SG,PASS}} = \frac{1}{V_{IN} - V_{O,BUF}} = \frac{1}{V_{IN} - (V_{SG,BUF} + V_{OE})} \quad [V]$$

where the input voltage is VIN, the buffer output voltage is VO,BUF, the dropout voltage is VDO, the pass transistor source-gate voltage is VSG, P ASS, the error amplifier output voltage is VOE, and the buffer source-gate voltage is VSG,BUG

D. Error Amplifier

As with the pass device and buffer, we must take into account all of the prior limitations and characteristics while selecting the best topology for the error amplifier.

Low quiescent current, appropriate bias under all load current and input voltage circumstances, and a high enough gain to offer adequate precision and PSR at the output—without being overly high so that the system stays stable—should be the objectives. Random and systematic input-referred offsets should also be minimal. The design of the error amplifier itself must also be taken into account in order for it to drive the buffer correctly.

1. Differential Pair

When choosing the differential amplifier topology, the reference voltage (vref) could be a limiting issue. Examining the PMOS differential pair, the least amount of headroom required above Vref is

$$V_{IN,min} = V_{ref} + V_{SD,sat} + V_{SG} = 2 \cdot V_{SD,sat} + V_{THP} + V_{ref} \quad [V]$$

where VT HP is the PMOS's threshold voltage, VSG is its source-gate voltage, VSD,sat is its saturation voltage, and VIN,min is its minimum input voltage.

The scenario is different for the NMOS differential pair. Vref determines sizes of input pair indirectly. The reference voltage must be high enough to bias the input pair as well as the MT.

$$V_{ref,min} = V_{GS} + V_{DS,sat} = 2 \cdot V_{DS,sat} + V_{THN} \quad [V]$$

Given that Vref is 1.2 V and the minimum input voltage is 1.7 V, we prefer PMOS pair due to its simple biasing and low headroom.

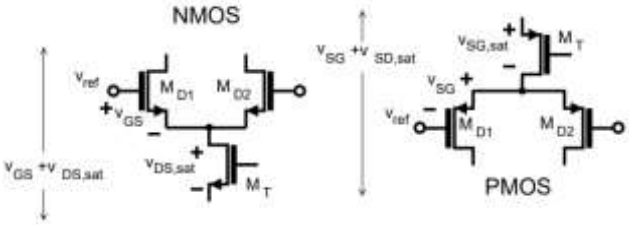

fig 2: input pair with tail MOSFET

2. Error Amplifier Topology

symmetrical operational transconductance amplifier (OTA) satisfies all specification criteria. The primary benefit of this topology is its huge output swing, but it also has two more current branches than a simple ota with differential pair, which results in a greater quiescent current. Only the saturation voltage of the two transistors limits the lowest and greatest voltage at its output. Thus, the NMOS saturation value is the lowest output voltage.

$$V_{OE,min} = V_{DS,sat} \quad [V]$$

Additionally, the output stage's PMOS saturation voltage is the highest.

$$V_{OE,max} = V_{IN} - V_{SD,sat} \quad [V]$$

This guarantees that under certain load current levels, the error amplifier may correctly drive the buffer and, consequently, the pass transistor.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

That is not a limiting factor because the OTA's GBW is sufficiently large in relation to the output dominant pole. The circuit is not entirely symmetrical in terms of PSR, and its derivation is more complicated than for a straightforward OTA with a single load current mirror.

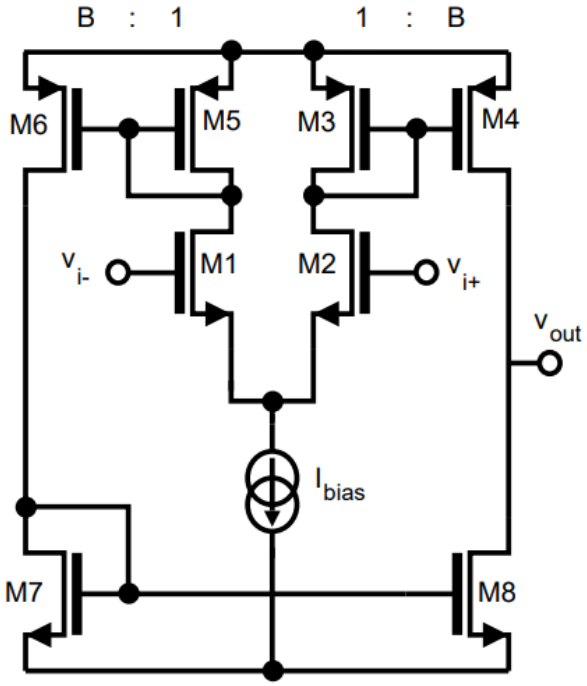

fig 3: three current mirror OTA

The PSR at the symmetrical OTA's output is determined by NMOS and PMOS type mirror PSR. Additionally, all of the OTA's nodes—aside from the output node—are gate-drain connected, meaning that their impedance is low because the impedance facing the gate is 1/gm. This lowers the internal node resistance to about 1/gm in the tiny signal scenario.

E. LDO TRANSISTOR SIZING

The MOSFET is a realiable only in saturation region because small signal current solely depends on small signal input.to achieve low quiescent we need to target lowest w/l values so that it does not draw excessive unwanted power. As error amplifier Major current demanding device we need to design with lesser nodes.

The goal is to improve the matching of components, which requires moving the current mirrors into the strong inversion region. However, this is complicated by the fact that small currents are involved. If the transistors are lengthened to achieve strong inversion, the output resistance at the nodes increases, which is undesirable. The objective is to minimize the gm/ID ratio without sacrificing the stability of the system. The biasing transistor M4 and the differential pair M1-M2 can remain in saturation at a voltage of 1.2 V, which is adequate for their operation.

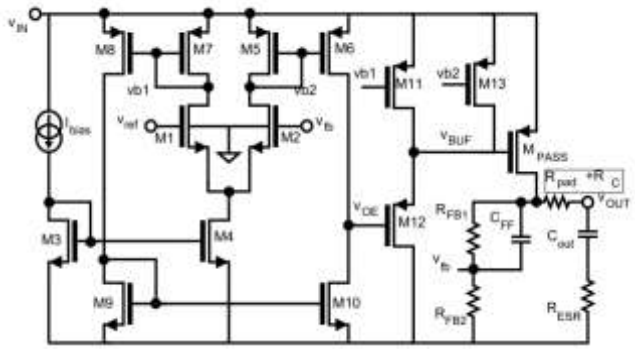

fig 4: final LDO design

Transistor name	Calculated ratio
M1 & M2	2/1
M3 & M4	8/1
M5 & M6	3/1

M7 & M8	6/1
M9 & M10	2/3
M11& M13	6/1
M12	10/0.6
M PASS	8(30/0.13)

table 1: MOSFET W/L ratios

The differential pair M1 and M2 operate with a low VDS,sat as they are designed for gain in weak inversion, and this doesn't affect the headroom available for the current mirrors involving transistors M5-M6 and M7-M8. The key saturation concern arises with the transistor M10 at the output of the error amplifier. To increase the current through the pass transistor as the load current rises, feedback must be used to raise the VSG of the pass transistor. Since this is simply a shifted voltage from the buffer output, both the voltage at the gate and the buffer output VBUF decrease, which causes the output of the error amplifier, VOE to drop as well.

III.RESULTS

A. DC ANALYSYS

1. DROPOUT VOLTAGE

The bandwidth at which the LDO supplies constant output irrespective of load. As required output voltage is 1.5V . when the regulator cannot maintain 1.5V Is goes to cutoff region. that implies that, the feedback loop cannot bear the output value.

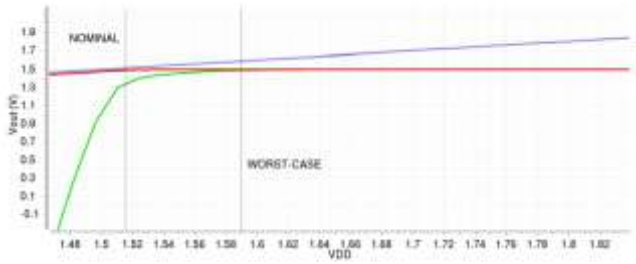

fig 5: voltage sweep regulation

2. LINE REGULATION

The slightest change of voltage output due to change in input voltage sweep is known as line regulation. It is essentially the regulator's constant DC power supply gain.

By sweeping along the input voltage range and determining change in output voltage we determine line regulation. in worst case corners, DC The findings are shown. As expected, the worst corner is for the highest output capacitor and the lowest bias current, which results in a reduced gain that is proportionate to the line regulation.

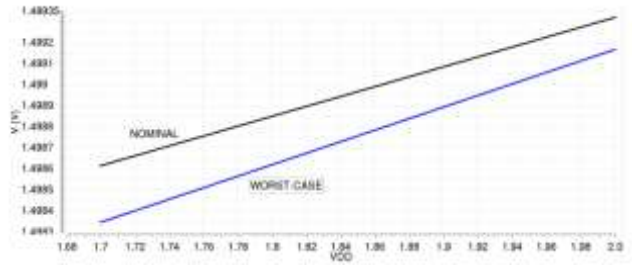

fig 6: line regulation

3. LOAD REGULATION

Load regulation is an additional steady state parameter. It derives how well the output voltage remains stable if the current drawn fluctuates. usually load regulation is limited by loop gain of error amplifier.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

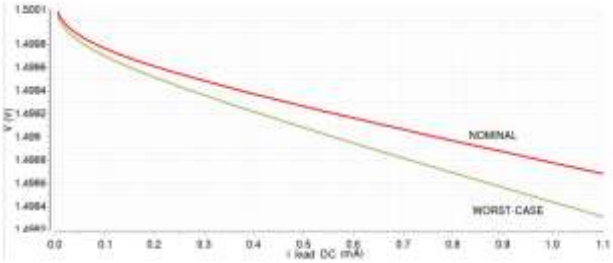

fig 7: load regulation

B. AC ANALYSYS

To determine phase margin and gain margin, it is crucial to measure the gain and phase by breaking feedback loop for open loop conditions. The circuit's ability to respond quickly to changes at the input or output is also defined by the unity gain bandwidth, or f0dB.

By giving step response as test signal, we can derive inputs and other conditions by open loop characteristics like phase margin. However as, stability is determined by phase and gain margin it is also the most crucial factor. Our goal is to have a phase margin in the worst corner of at least 45◦. moving of the zeros and other poles as a result of the altered bias circumstances, in addition to the shifting of the dominant pole that we previously discussed. The greatest noticeable divergence occurs when the dominating pole is at the lowest frequency and the load current is very low (9 uA).

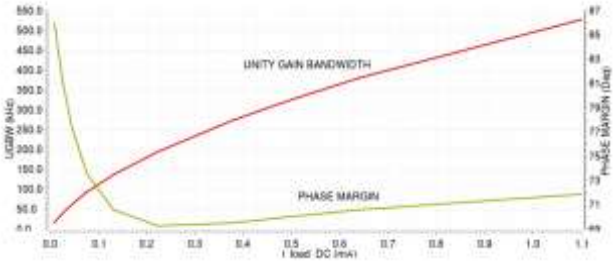

fig 8: UGBW / phase vs load current

The Power Supply Ripple Rejection, or PSRR for short, is a crucial metric. We are aware that it establishes the regulator's ability to effectively suppress fluctuating input voltage throughout a broad frequency range. Remember that in our design, the RC filter—which is made up of the pad's resistance and the output capacitor—affects the PSR at the LDO's very output. High frequency supply signals are first filtered slightly below the bandwidth of unity gain. The PSR would typically decrease in magnitude near unity gain bandwidth.

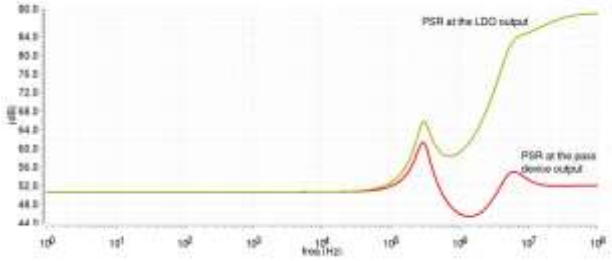

fig 9: PSRR

C. TRANSIENT ANALYSYS

As the load device current drawn fluctuates abruptly time to time, the LDO regulator need to coupe up with load demands.so the circuit working in action along with steady response on impulse change in transients can be determined. Load transient analysis and Line Transient analysis are deciding factors for circuit performance. For Good design for stability the circuit settles to nominal voltage without oscillations.

1. LOAD TRANSIENT

For the load transient response at 5 kHz to which is minimum expected time to settle. The system transitions maximum load current to minimum load current smoothly, due to high phase margin. during transition from minimal to maximum load little overshoot is observed.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 12, December : 2024

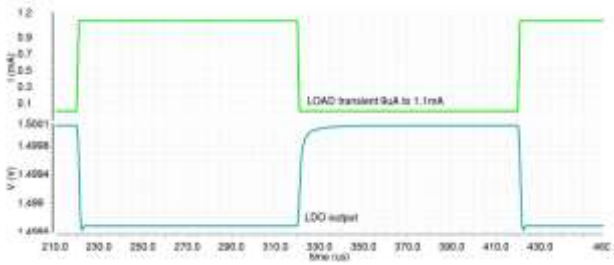

fig 10: load transient 9uA to 1mA in 5kHZ

Overshoot seen was primarily due to large capacitor which is trying to pump voltage from its storage before LDO reacts to change in transient. This turbulence is in order of few mV therefore it can be neglected.

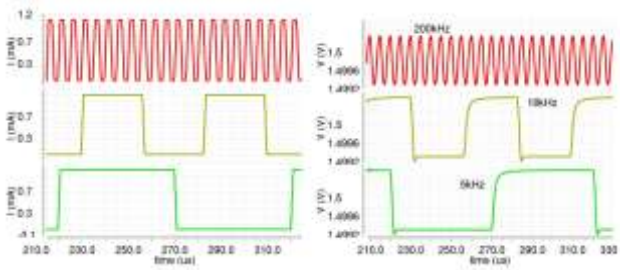

fig 11: load transient load transient 9uA to 1mA in 18kHz and 200kHz

Beyond the frequency limit the output cannot be regulated because of it was unable to read the fast change in transients so, the input fluctuates dramatically while LDO trying to regulate most recent changes. The regulation effect fades away with increase in transient frequency.

2. LINE TRANSIENT

The behaviour of the line transient differs significantly from that of the load transient. Ideally output voltage should be stable irrespective of input change in line transients but slight change in order of uV is seen due to power supply noise. High PSRR can increase line transients. here the line transient's overshoots contrarily, load transient's overshoots are opposite. Additionally, line transients for small and big load currents are of different scale.

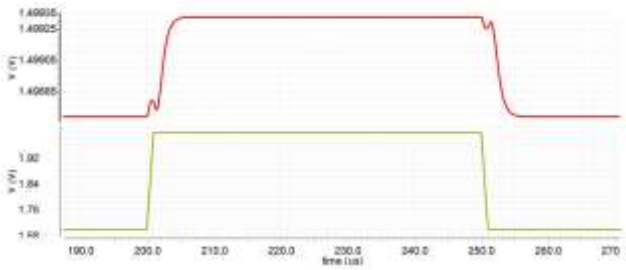

fig 12: line transient 1.7v to 2 v in 1.1mA ,5kHz

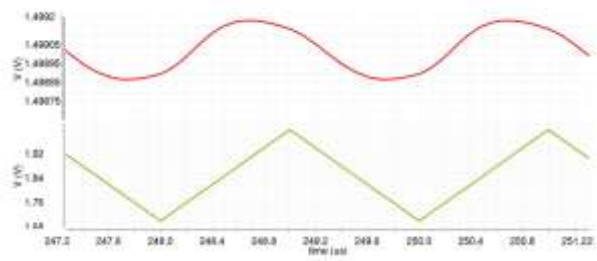

fig 13: line transient 1.7v to 2v in 1.1mA, 1MHZ

During downfall of line transient the capacitor supplies demanded voltage then loses only half of capacity until error amplifier picks up. When voltages increase, the capacitor is at full load so it responds quickly as it is at peak capacity.

At higher frequencies than the system's bandwidth, line transients behave unexpectedly as the error amplifier fails to

coupe up with error signal and fails to regulate with change in fast transients.

V. CONCLUSION

A conclusion section is not required. Although a conclusion may review the main points of the article, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions. In this thesis, design of low dropout regulator has been performed using GPDK90 PDK by cadence virtuoso EDA. During the design of LDO several iterations of optimization is done having low quiescent current as top priority which is under 10uA. Here error amplifier plays a crucial role deciding performance of LDO.in our case we choose classical 3 current mirror OTA Final design is stable in all conditions and are within desired specifications boundary however this LDO can be further improved by implementing various topologies for on chip SOC applications.

REFERENCES

[1] Yoo, HJ., van Hoof, C. (2011). "Introduction to Bio-Medical CMOS IC". In: Yoo, HJ., van Hoof, C. (eds) Bio-Medical CMOS ICs. Integrated Circuits and Systems. Springer, Boston, MA. https://doi.org/10.1007/978-1-4419-6597-4_1

[2] B. Razavi, "The low-dropout regulator," IEEE Solid-State Circuits Mag., vol. 11, no. 2, pp. 8–13, Spring 2019, doi: 10.1109/ MSSC.2019.2910952.

[3] Bang S. Lee," Understanding the Terms and Definitions of LDO Voltage Regulators" in Texas Instruments applications report, october 1999.

[4] B. Razavi, "The Design of An LDO Regulator [The Analog Mind]", in IEEE Solid-State Circuits Magazine, vol. 14, no. 2, pp. 7-17, Spring 2022, doi: 10.1109/MSSC.2022.3167308.

[5] Choi, J.; Kweon, S.-J.; Jeon, H. "Single-Stage CMOS Operational Transconductance Amplifiers (OTAs)": A Design Tutorial. Electronics 2023, 12, 3833. https://doi.org/10.3390/electronics12183833

[6] I. B. Attili and S. A. Mahmoud, "Examining the Performance of Low Power – Area Efficient OTA Designs that are Based on Different Current Shunting Techniques," 2018 30th International Conference on Microelectronics (ICM), Sousse, Tunisia, 2018, pp. 200-203, doi: 10.1109/ICM.2018.8704075.

[7] Sapna Kumari, C., Ramya, K., Puneet, J., Hemanth, S., Karkera, M. B., & Deekshith, T. K. (2022). "Design and simulation of low dropout voltage regulator using 180nm technology". International Journal of Health Sciences, 6(S4), 9904–9915. https://doi.org/10.53730/ijhs.v6nS4.10820

[8] Abhishek Sharma, Sudeep Singh Chhaukar, Karri Babu Ravi Teja, Kavindra Kandpal, "Design of Low Dropout Voltage Regulator for Battery Operated Devices", IEEE 2018.

[9] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," in IEEE Journal of Solid-State Circuits, vol. 33, no. 1, pp. 36-44, Jan. 1998, doi: 10.1109/4.654935.

[10] R. J. Milliken, J. Silva-Martinez and E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54, no. 9, pp. 1879-1890, Sept. 2007, doi: 10.1109/TCSI.2007.902615.

[11] He, L.; Li, X.; Xu, S.; Pan, G.; Xie, C.; Chen, H.; Song, Z. "A Fast-Transient-Response NMOS LDO with Wide Load-Capacitance Range for Cross-Point Memory". Sensors 2022, 22, 9367. https://doi.org/10.3390/s22239367

[12] Behzad Razavi., "Design of Analog CMOS Integrated Circuits" McGraw-Hill Higher Education, 22 Jan 2016 - Technology & Engineering

[13] Phillip E Allen and Douglas R Holberg. "Cmos analog circuit design". 2002.

[14] Paul R Gray, Paul J Hurst, Robert G Meyer, and Stephen H Lewis. "Analysis and design of analog integrated circuits". John Wiley & Sons, 2008.

[15] R Jacob Baker. "CMOS: circuit design, layout, and simulation", volume 1. John Wiley & Sons, 2008.

[16] Ke-Horng Chen "Power Management Techniques for Integrated Circuit Design", John Wiley & Sons Singapore pp 28-121