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A LOW-POWER HIGH-SPEED SENSE-AMPLIFIER-BASED FLIP-FLOP IN 55 NM MTCMOS

N. Tejaswini, PG Scholar, Dept. of ECE, K.S.R.M College of Engineering, Kadapa.
Dr. M. Venkatanarayana, Ph.D Professor & Dean, R&D, Dept. of ECE, K.S.R.M College of Engineering, Kadapa.

ABSTRACT

This low-power, high-speed sense-amplifier-based flip-flop (SAFF) is perfect for. By including a novel sense-amplifier stage and a novel single-ended latch stage, the flip-flop's power consumption and latency are significantly lowered. By using MTCMOS optimisation, the suggested SAFF is able to provide low voltage functioning. Compared to the current master-slave flip-flop (MSFF), the proposed SAFF has a shorter latency and uses less power by reducing the size of the suggested flip-flop and improving the power-delay-product compared to standard SAFF and MSFF, the proposed SAFF is able to offer robust operation even with low supply voltages. However, in our design, we utilize 45nm technology, which allows us to get the desired output with just 1LVT (low a threshold voltage).

1. INTRODUCTION

A circuit that increases the strength of its input signal is often referred to as an amplifier. Amplifier circuits are categorised based on their circuit designs and modes of operation; however, not all amplifier circuits are identical. One frequent device in the field of "Electronics" is the tiny signal amplifier, which can take a weak signal from a sensor like a photo-device and turn it into a stronger one that can power a relay, light, or speaker. From operational amplifiers and small signal amplifiers to large signal and power amplifiers, the term "amplifier" encompasses a wide range of electrical circuit types. A signal's magnitude, the amplifier's physical design, and the connection between the input signal and the load current all play a role in the amplifier's categorisation. The three primary characteristics of a perfect signal amplifier are input resistance (RIN), output resistance (ROUT), and amplification (A). A universal amplifier model may demonstrate the connection of these three features regardless of the complexity of an amplifier circuit. The term "gain" describes how much of an increase there is in the signal strength relative to the input and output signals. An amplifier's gain is a measure of its ability to "amplify" the signal applied to it. A gain of "50" would indicate that the amplifier is capable of producing an output voltage of 50 volts from an input voltage of 1 volt. Basically, the input signal has been amplified by a factor of fifty. Gain is the name given to this growth. The output-to-input ratio is the simplest way to describe amplifier gain. Gain is a ratio that does not have units, although it is usually represented in electronics by the letter "A" for amplification. A simple way to determine an amplifier's gain is to divide the output signal by the input signal.

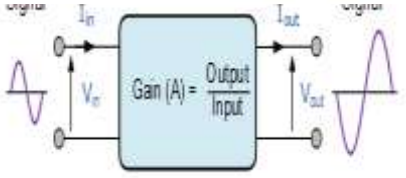
a) Amplifier Gain

One way to think about the connection between the input and output signals is as the foundation for the amplifier gain. Here are some examples of the three forms of amplifier gain that may be measured: voltage gain (Av), current gain (Ai), and power gain (AP). The kind of gain that is

applicable depends on the quantity being measured.

b) Voltage Amplifier Gain:

$$Voltage\,Gain\,(A_v) = \frac{Output\ Voltage}{Input\ Voltage} = \frac{Vout}{Vin}$$



Sense amplifier:

A sense amplifier is a component of an integrated circuit, which is a kind of semiconductor memory chip used in contemporary computers. The word "integrated circuit" has been used since the days of magnetic core memory. As part of the read circuitry, a sense amplifier is utilised to read data from memory. Its job is to detect the weak signals from a bit line, which stands for a data bit (1 or 0) stored in a memory cell, and to amplify the small voltage swing to discernible logic levels, allowing logic outside of the memory to interpret the data correctly. Two to six transistors, with four being the most common, make up a modern sense-amplifier circuit. In contrast, early core memory sense amplifiers might have thirteen transistors. Hundreds, if not thousands, of identical sense amplifiers typically comprise a contemporary memory chip, with one amplifier assigned to each column of memory cells. Thus, a computer's memory subsystem solely has sense amplifiers, which are analogue circuits.

2. LITERATURE SURVEY

[1]Jeong, H.; Oh, T.W.; Song, S.C.; Jung, S.-O. Sense-amplifier-based flip-flop with transition completion detection for low-voltage operation. 2018.

The SAFF-TCD is a low supply voltage (VDD) operating high-speed, very reliable flip-flop that uses a sensing amplifier for transition completion detection. When the SAFF-TCD detects that the sense-amplifier stage transition is complete, it uses its own detecting signal. In conclusion, this post has helped me think about the idea behind the present dispute and how to avoid SAFF issues.

[2]Jeong, H.; Park, J.; Song, S.C.; Jung, S.-O. Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time. IEEE J. Solid-state Circuits 2019.

We suggest a STPL, or self-timed pulsed latch, for use with low VDD. In STPL, the hold time issue of the typical pulsed latch is resolved by adaptively generating the transparency window by comparing the input and output. Hold time, setup time, and the usual pulsed latch issue have all been taken into account in this article.

[3]Kim, J.-C.; Jang, Y.-C.; Park, H.-J. CMOS sense amplifier-based flip-flop with two N-C2MOS output latches. Electron. Lett. 2000, 36, 498–500.

To further enhance the operational speed, Nikolic's flip-flop was suggested. A cross-coupled inverter latch with two inverting buffers were used to replace the NAND SR latch of [1]. But compared to the standard SAFF, the flip-flop's power consumption is much higher. Two NC2 MOS latches were used in lieu of the NAND SR latch in the new SAFF that was suggested in this study. Among the flip-flops tested in this study, the new SAFF had the quickest operating speed; nevertheless, its power consumption was somewhat higher than that of the traditional SAFF. A brief overview. I have taken into account what this

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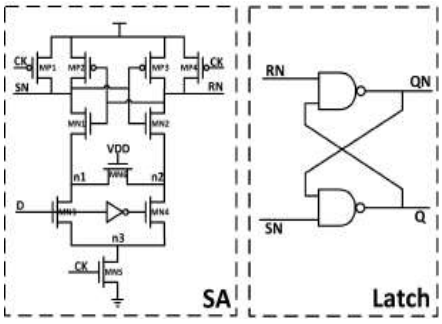
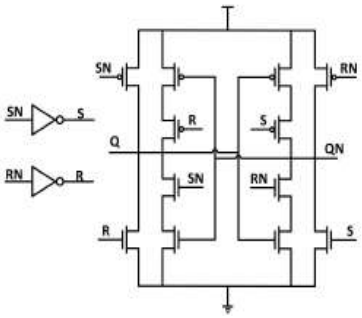
article says Boosts performance above a dynamic style circuit's flip-flop counterpart

3. EXISTING METHOD

The traditional SAFF, seen in Figure 2a, consists of a SA and an S-R latch that is based on NAND gates. The SAFF functions in the following way. While CK is low, the voltages of SN and RN are pre-charged to VDD, and the latch maintains the output data. The pre-charge transistors MP1 and MP4 are disabled and MN5 is enabled at the rising edge of CK. One of the pre-charge nodes (SN and RN) is set to VDD and the other is discharged to 0, based on the data that is entered. After then, the SA stage updates its data, and the latch records it. When CK is high, the SA's output is maintained by use of the always-on transistor MN6. At the rising edge of CK, for instance, SN is discharged to 0 in response to D = 1, and it must remain at 0 during the positive half cycle of CK. At this point in time, MN6 is functional, and because D could change to 0 during the positive half cycle, SN needs an alternate route to 0. The typical SAFF's major drawbacks are an imbalanced S-R latch delay and a very powerful pre-charge operation. In addition, the SAFF's resilience at low supply voltages is diminished by the always-on transistor.



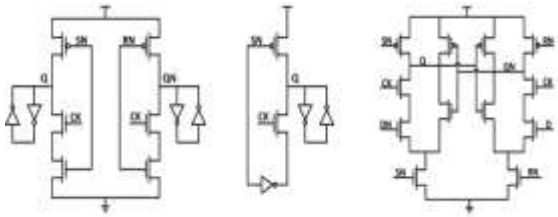
(a)



(b)

Figure 2. (**a**) Schematic of the conventional sense-amplifier-based flip-flop (SAFF)
(b) Schematic of the latch in Nikolic's SAFF

To reduce the SAFF's latency, Nikolic et al. suggested a latch for the SAFF that consisted of several complex logics, two inverters, and the elimination of the delay dependency between Q and QN in the traditional SAFF. In Figure 2b, you can see the latch's schematic. The four signals SN, RN, S, and R directly produce the outputs Q and QN, while the two inverters are used to invert SN and RN. Both the CK-to-Q latency and the reliance between Q and QN are eliminated. On the other hand, the SAFF's power consumption will rise due to a major glitch that occurs when both the output Q and the next data input are high. On top of that, the back-to-back inverters' current argument also leads to higher power usage.



(a) (b) (c)

Schematic of the latches in (**a**) Kim's SAFF; (**b**) Lin's SAFF; and (**c**) Strollo's SAFF

A hybrid SAFF combining conventional and Kim's SAFF was suggested by Strollo et al. in order to provide rapid and glitch-free

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functioning. Figure 3c displays the schematic of the latch in Strollo's SAFF.The always-on transistor in the SA stage causes the low voltage operation fault in all of the SAFFs mentioned above. To get around this issue, SAFFs use detecting signals to gate the always-on transistor, which is an improvement over earlier SAFFs. Figure 4 serves as a schematic of Jeong's SAFF. This SA stage changes the control signal of the always-on transistor to the detection signal. One major issue with Jeong's SAFF is that the FF's propagation time will be increased due to the transition completion detection algorithm.

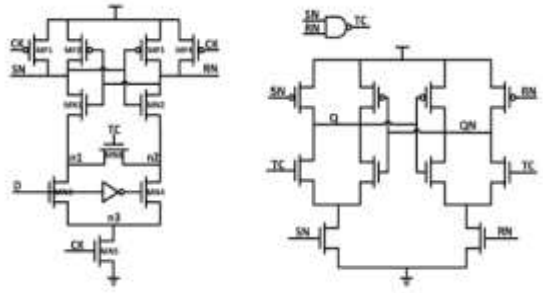

Figure 4. Schematic of Jeong's SAFF

Disadvantages:

The low voltage operating difficulty is experienced by all of the SAFFs mentioned before because of the always-on transistor in the SA stage. Other issues include delay, power consumption, and the current contention of the back-to-back inverters, which will lead to an increase in power consumption.

4. PROPOSED METHOD

Figure 5 shows the planned SAFF schematic. The SAFF, like its predecessors, consists of a SA stage and a slave latch, as seen in Figure 5. The SA stage may collect data immediately after the rising edge of CK, as mentioned before, and the output can be maintained throughout the negative half cycle of CK by using the slave latch.

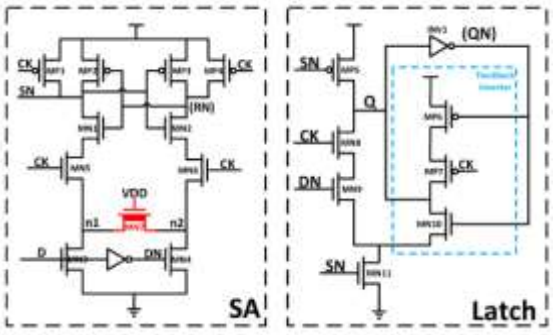

Figure 5. Schematic of the proposed SAFF.

Nodes n1, n2, and n3 in Figure 2a are discharged to VSS during the data-capturing process regardless of the input data, since the SA stage in the traditional SAFF requires to charge all the internal nodes during the pre-charge operation. The pre-charge action of the SA's n1, n2, and n3 is really electricity wasted and does nothing useful. Due to the high sizes of the transistors MN3 and MN4, which are used to reduce propagation delay, pre-charge operation of these nodes results in a significant waste of power as the voltages of n1, n2, and n3 are charged close to the power supply voltage. Figure 5 shows the new SA structure after the CK-controlled NMOS (MN5 in Figure 2) is divided into two halves (MN5 and MN6) and relocated to link directly to the back-to-back inverter (MN6 in Figure 5). By converting MN5 and MN6 to o_ when CK is low, the nodes associated with MN3 and MN4 are no longer required to charge during pre-charge operation. Figure 5 shows that the n1 and n2 voltages stay low for the whole procedure. As a result, the pre-charge operation's power is significantly diminished.

a) High-to-low transition:

The information that was entered Since DN is the inverse of D, it does low-to-high conversion simultaneously with D, which means that D completes high-to-low conversion before the rising edge of CK. When CK is in its negative half cycle, SN and RN are already charged to a

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high potential. When CK begins to rise, MN2, MN6, and MN4 release RN to a low level. SN stays high while MN8, MN9, and MN11 discharge the output Q to low.When QN completes the low-to-high conversion (or Q completes the high-to-low conversion), MP7 gates the feedback inverter. After QN becomes high, the feedback inverter can maintain a low Q voltage thanks to MN10 and MN11.

b) Low-to-high transition:

While DN completes high-to-low conversion, input data D concludes low-to-high conversion before the rising edge of CK. When CK is in its negative half cycle, SN and RN are already charged to a high potential. On the ascent of CK, SN is released into low via MN1, MN5, and MN3. The process is also contention-free since MN11 cuts off MN10 when SN is low and the output Q is charged to high via MP5. Throughout the positive half cycle of CK, MP5 maintains the output Q. In the negative CK cycle, MP5 is off and SN is pre-charged to high, while MP6 and MP7 keep the output Q constant.

Advantages:

Less power is used in comparison to the current design.
The circuit's latency is decreased.
The system's footprint is less as compared to the current layout.

5. RESULTS

The 45 nm technology is the basis for the planned SAFF's design. A number of other SAFFs including the conventional SAFF, Nikolic's SAFF, Lin's SAFF, and Jeong's SAFF have been developed using the same technology as the proposed SAFF so that its validity may be checked. All post-layout simulations are run using the same conditions to facilitate comparisons. The table below describes in detail the performance comparisons of the several flip-flops, including their area, power consumption, CK-to-Q latency, setup time, and hold time.

Table - 1: Power and delay comparison of Existing and Proposed SAFF

Type of SAFF	Power(mw)	Delay(ns)	Area
Nikolic's SAFF	7.3	30	28
Strollo's SAFF	1.2	30	24
Jeong's SAFF	1.9	40	26
Lin's SAFF	2.4	0.3	20
Proposed SAFF	0.04	0.4	22

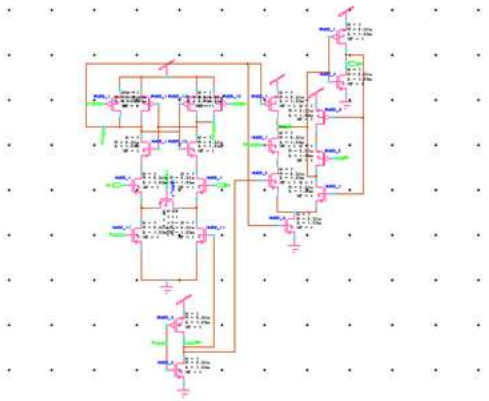

Figure -6: Schematic of the proposed SAFF is shown in the figure

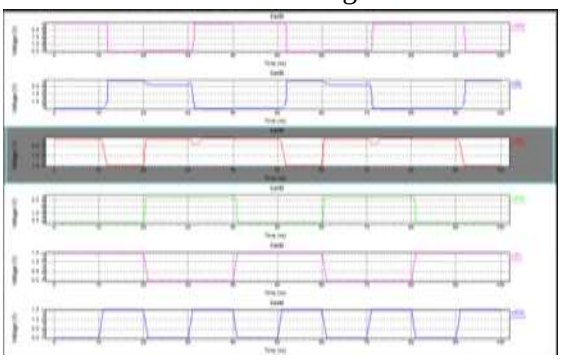

Figure – 7: Wave forms for proposed SAFF

Figure – 8: Area of the proposed SAFF Power of the proposed SAFF

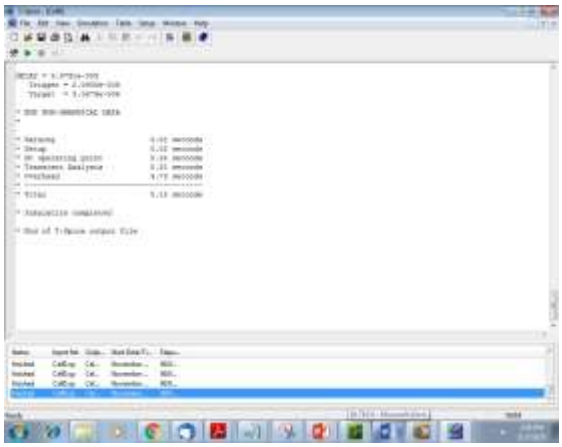

Figure – 9: Delay of the SAFF

6. CONCLUSION

Presented below is a proposal for a low-power, high-speed SAFF. It is suggested that the SA stage's 45nm technological structure be used to reduce the SAFF's pre-charge power. On top of that, we provide a single-ended latch that is both glitch-and contention-free. The SAFF's latency and power are optimised with the use of the single-ended latch and the new SA stage. A comparison between the power-delay-product of the standard SAFF and the suggested upgrade. Since the suggested SAFF is an upgrade over the MSFF, it might be a suitable replacement for MSFFs in digital systems that need low-power, high-speed operation.

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