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A NINE-LEVEL QUADRUPLE BOOST INVERTER TOPOLOGY FOR SMALL-SCALE SOLAR PV APPLICATIONS

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ABSTRACT

Renewable energy, particularly small-scale solar photovoltaics (PV), is making an increasing contribution to the energy sector. High gain DC-DC converters are commonly used as front-end converters to increase the low voltage of PV panels; additionally, DC-AC converters (multilevel inverters) are used for standalone AC loads or grid integration. This paper proposes a nine-level quadruple boost inverter topology for small-scale solar PV applications to avoid the front-end converter while meeting both objectives. The proposed topology uses a switched capacitor technique to boost voltage and has capacitor self-voltage balancing. This paper describes the detailed operation of the proposed nine-level inverter, as well as voltage stress calculations, loss analysis, and circuit parameter design. A high-gain generalised multilevel inverter (MLI) topology is also described. In addition, the proposed MLI is compared to competitive inverters from the recent literature. The proposed MLI topology has several advantages, including a low total standing voltage and a low component count; it can also generate bipolar voltage inherently. The proposed MLI topology's performance is validated using MATLAB-based simulations. Further, the simulation results are presented by considering load variations, modulation index variations, and output frequency variations. The simulation efficiency obtained is in the range of 96.2% to 92.8% for proposed 9-level inverter.

INTRODUCTION

The world's energy consumption is increasing on a daily basis. Large-scale renewable sources, particularly solar photovoltaic, are being integrated into conventional power generation to meet the increased load demand. Large amounts of photovoltaic energy generated in a single location and transmitted over long distances reduce system efficiency. Recently, distributed generation has been introduced to overcome this problem and increase system efficiency [1], and the percentage of PV generation through solar rooftop has increased significantly, accounting for approximately more than 20% of total PV generation capacity [2]. Small-scale solar PV systems for rooftop applications range in power from 0.5kw to 2kw, with voltage ratings ranging from 60V to 100V. To avoid bulky and expensive batteries, solar PV is generally preferred to operate in a grid-connected mode. Figure 1 shows the solar rooftop connected to a low voltage distribution network of 415V (3-8) and 230V (rms) for 1-8. High gain DC-DC converters [4] are used at the front end of the DC-AC converters to achieve compatibility between low DC voltage PV systems and AC grid voltage. There are numerous MLI topologies proposed in the literature for DC-AC conversion. The most well-known topologies are diode clamped [5, flying capacitor (FC), and cascaded H-bridge multilevel inverters. Unbalanced capacitor voltages plague diode clamped MLI and FC MLI, necessitating an additional voltage balancing circuit [6]. Cascaded H-bridge MLI is modular in structure, requiring more isolated DC sources [7]. Recently, various reduced switch nine-level inverter topologies have been presented in [8][11]. These topologies use fewer switches and diodes to get the same number of levels compared with the basic MLI topologies.

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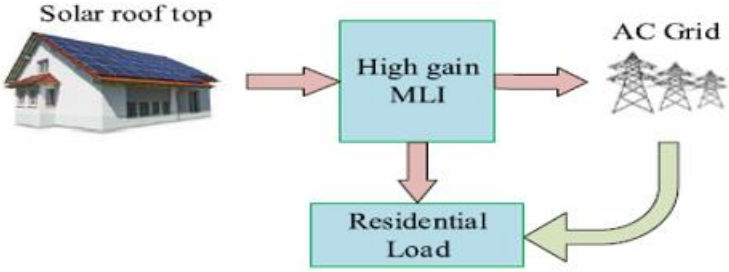

FIGURE 1. Solar rooftop PV application.

LITERATURE SURVEY

Operation and Control of a NineLevel Modified ANPC Inverter Topology with Reduced Part Count for Grid-Connected Applications,

This paper describes a nine-level active-neutral-point-clamped (ANPC) multilevel inverter (MLI) topology for grid-connected applications that only requires ten switches. The proposed structure is divided into two parts: a five-level ANPC unit and a two-level converter leg, the midpoint of which serves as another ac terminal. To ensure that the voltage across the flying capacitor is tightly balanced, an ad hoc switching state redundancy based modulation strategy is used, which is implemented using a look-up table, further simplifying the control complexity. Simulations and experimental tests are used to validate the performance and effectiveness of the proposed topology and its control scheme. Comparison with other MLIs is included to highlight the merits of the proposed topology. From the results, it will be shown that the proposed inverter requires the least part count as compared to other topologies with the same performance and output quality.

Implementation of Hybrid GSA SHE Technique in Hybrid Nine-Level Inverter Topology

The current trend in multilevel inverters (MLIs) is to produce a high-quality staircase ac voltage waveform while using the fewest switching devices possible. In this context, this article presents a topological and modulation scheme-based solution for optimum MLI performance. To reduce the number of switching devices, an adaptable dc voltage link in conjunction with a modified H-bridge unit is introduced. A hybrid gravitational search algorithm (GSA) selective harmonic elimination (SHE) technique is proposed and implemented on the newly developed MLI topology with symmetric dc sources to improve the quality of the voltage waveform and reduce switching losses in the proposed topology. Comparative analysis is performed with the conventional and existing hybrid cascaded MLI topologies, which exhibits the superiority of the proposed topology in terms of reduction in count of switching devices, count of components, and conduction losses. The efficacy of the proposed hybrid GSA SHE technique is shown in the simulated results. The feasibility of the proposed MLI topology and SHE technique is further verified by the experimental results of a nine-level inverter with both equal and unequal dc sources.

. “A Five-Level Boosting Inverter for PV Application

Because of their high efficiency and low cost, transformerless inverters (TIs) are widely used in grid-connected photovoltaic (PV) applications. However, the lack of galvanic isolation allows ground leakage current to flow due to PV parasitics, resulting in safety concerns and deteriorated power quality. A single-phase five-level TI topology with switched diodes and floating capacitors (FCs) is proposed in this article. In accordance with the VDE-4105 safety standard, the proposed topology employs fewer active power switches, has self-voltage-balancing of FCs, voltage boosting capability, and suppressed leakage current. A suitable modulation strategy is applied to the proposed TI in order to generate a common-mode voltage with a reduced number of voltage swings and transitions, resulting in suppressed leakage current. A prototype model with a power rating of 1 kW is created, and the experimental results are presented. In the simulation and experiments, leakage currents of 10 and 17 mA are obtained, respectively. To demonstrate the merits of the proposed TI, a detailed comparison with other similar topologies is presented.

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Step-up switched-capacitor module for cascaded MLI topologies

This study presents a new module for cascaded multilevel inverters (MLIs) based on the switched-capacitor technique. In the proposed switched-capacitor cell, the capacitors are charged in a self-balancing manner. Significant advantages of the proposed topology include the ability to boost voltage and generate bipolar voltage levels without the use of an end-side H-bridge inverter. As a result, its circuit employs lower-voltage semiconductors. The proposed topology reduces the number of circuit elements as well as total blocking voltage by switches when compared to traditional topologies and other recently introduced MLIs. Furthermore, the proposed inverter configuration and its operating principle are thoroughly investigated, as are capacitance and power loss calculations, as well as topology extension to achieve higher levels.

A Single DC Source Nine-Level SwitchedCapacitor Boost Inverter Topology with Reduced Switch Count

This paper describes a new boost inverter topology that employs a single dc source and two switched capacitors to generate a nine-level output voltage waveform. The capacitor voltages are self-balancing, so there are no sensors or auxiliary circuitry. The output voltage is twice as high as the input voltage, eliminating the need for an input dc boost converter, which is especially important when the inverter is powered by a renewable source. By comparing recent and conventional inverter topologies, the merits of the proposed topology in terms of device count and cost are highlighted. Furthermore, the proposed topology has a lower total voltage stress and a maximum efficiency of 98.25%. The operation and dynamic performance of the proposed topology have been simulated using PLECS software and are validated using an experimental setup considering a different dynamic operation.

PROPOSED TOPOLOGY

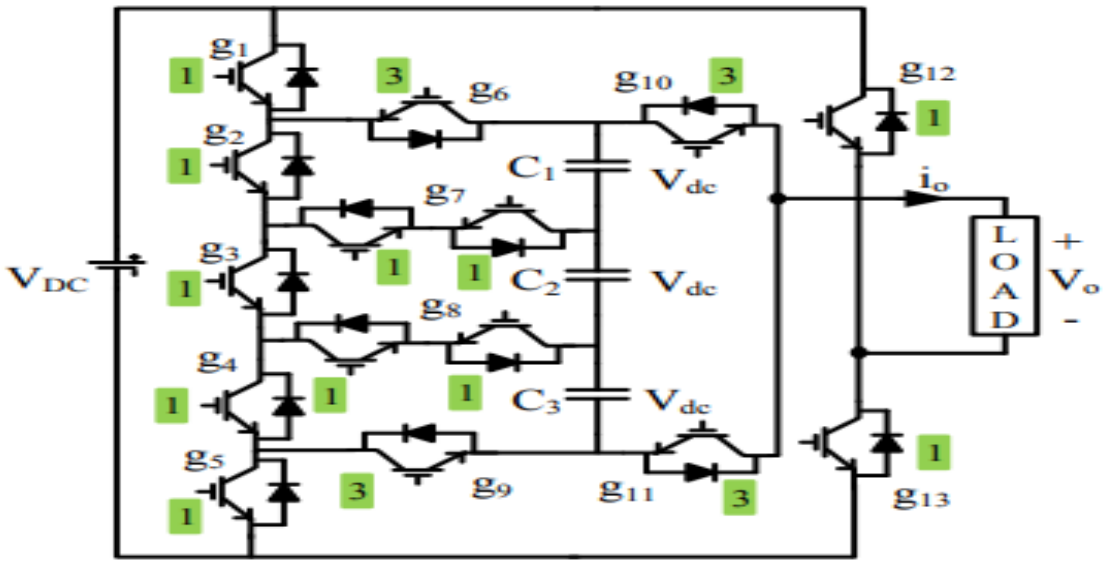

FIGURE 2. Proposed 9-level quadruple boost inverter (Proposed 1).

The proposed quadruple boost nine-level topology shown in Figure.2. It is structured with 1 DC source, 3 capacitors (C1, C2 & C3) and 13 switches in which 11 unidirectional switches (g1-g6 & g9-g13) and 2 bidirectional switches (g7 & g8). These switched capacitors are charged by using a series-parallel technique. Each capacitor is individually charged to Vdc and discharged to load by connecting in series with the DC source to obtain a high voltage gain. The output voltage of nine levels has ±4Vdc, ±3Vdc, ±2Vdc, ±Vdc, and zero levels. To avoid source and capacitor short circuit, switches pair (g12, g13) and (g10, g11), are operated complimentary. For each load voltage cycle, switches g10, g11, g12, and g13 have only two transitions (on to off and off to on). As a result, these switches operate at the load frequency (50Hz) and have low switching losses, improving the topology's overall efficiency. Switches (g1-g5) and (g12-g13) have a maximum blocking voltage (MBV) of Vdc, and because most of the

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switches have low voltage stress, the topology's total standing voltage (TSV) will be low. As shown in Figure 2, the voltage stress on each switch (g12-g13) is represented beside each switch in multiples of Vdc. where '1' denotes Vdc and '3' denotes 3Vdc. The proposed topology includes three capacitors, each of which is charged to Vdc. The three capacitors are designed to balance at Vdc by sequential charging and discharging during each load voltage cycle. Table I shows the gate signals for the switches in the proposed topology. The turn-on and turn-off states of the switches are shown as 1 and 0 in this table for each voltage level. The capacitors' charging, discharging, and floating states (without charging or discharging) are denoted .

B. PROPOSED GENERALIZED 2N+1 LEVEL MLI

Due to the requirement for higher grid voltages in grid integrated PV applications, the gain of the proposed quadruple boost 9-level inverter may not be compatible in some cases. For PV grid integration applications, a generalised topology with an extension circuit consisting of one unidirectional switch, one bidirectional switch, and a capacitor is proposed to achieve high gain with lower THD. The output voltage with '2x+9' levels and 'x+4' gain can be obtained by incorporating 'x' extension circuits into the proposed topology. Figure.3 depicts a generalised 2N+1 level with gain = N by extending the repeating unit highlighted in blue. N+7 unidirectional switches, N-2 bidirectional switches, N-1 capacitors, and one DC source comprise the generalised topology. The MBV of the proposed generalised topology is (N-1).

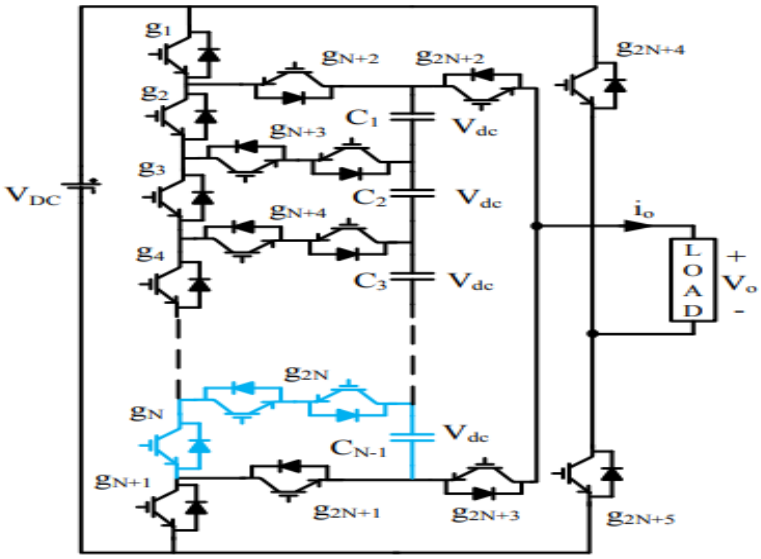

FIGURE 3. Proposed generalized MLI topology (Proposed 2)

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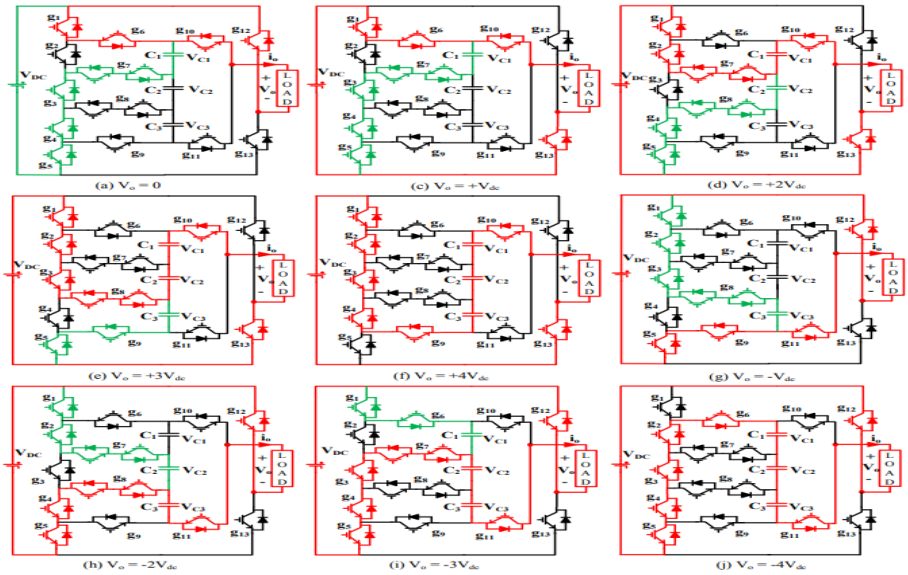
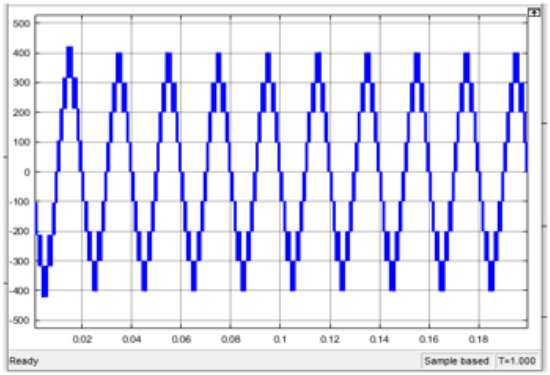


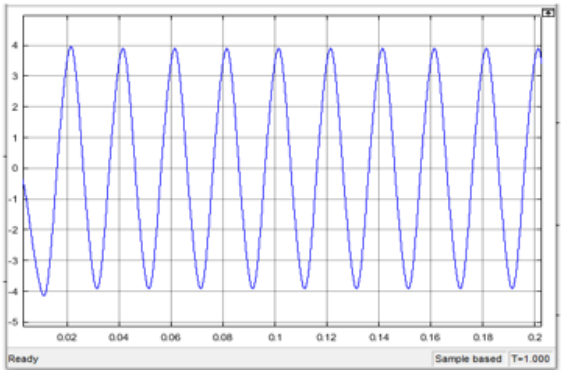
FIGURE 4. Operating modes of proposed topology (red indicates output voltage path and green indicates charging path).

SIMULATION RESULTS

In MATLAB/Simulink, the performance of the proposed topology is examined under various conditions. Vdc = 100V and C1 = C2 = C3 = 2200F are the ratings of the components used in the simulation. The load voltage, current, and balanced capacitor voltages of the proposed topology are shown in Figure.10 for the DC source voltage of 100V and the amplitude modulation index (Ma = 1). The output voltage has nine levels and a peak amplitude of 400V, with three capacitor voltages balanced at 100V.



(a) Vo



(b)I_L

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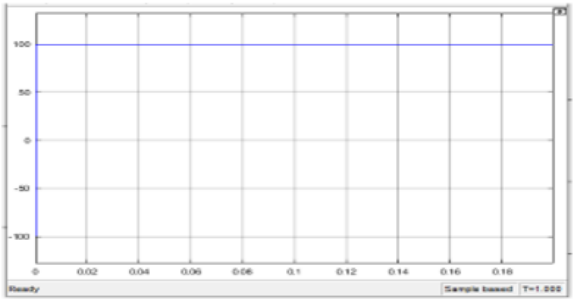
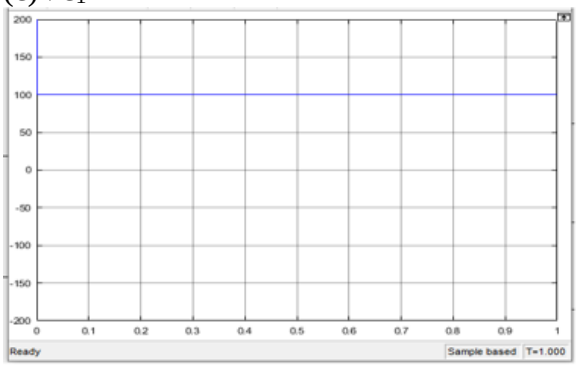
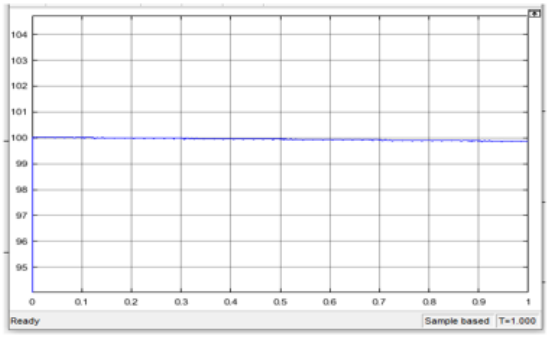


(c)Vc_1



(c)Vc_2



(c)Vc_3

FIGURE 5. Output voltage, current, and capacitor voltages at 100Ω+120mH.

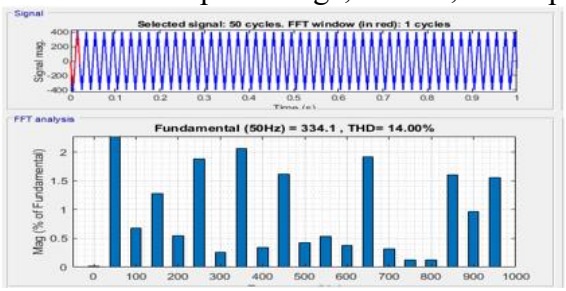
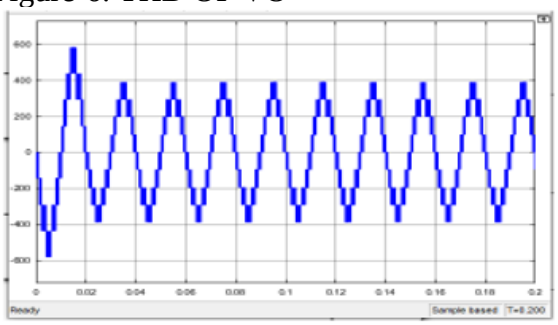


Figure-6: THD OF VO



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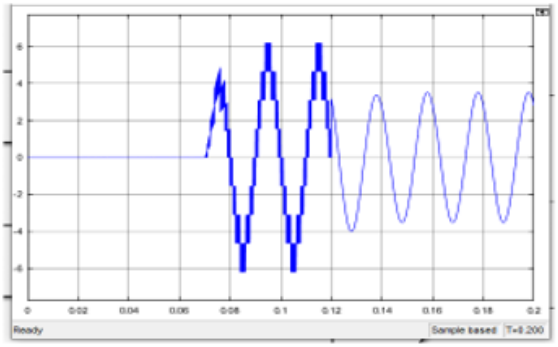

FIGURE 7. Output voltage, current for no load, 50Ω and 50 Ω +100Mh

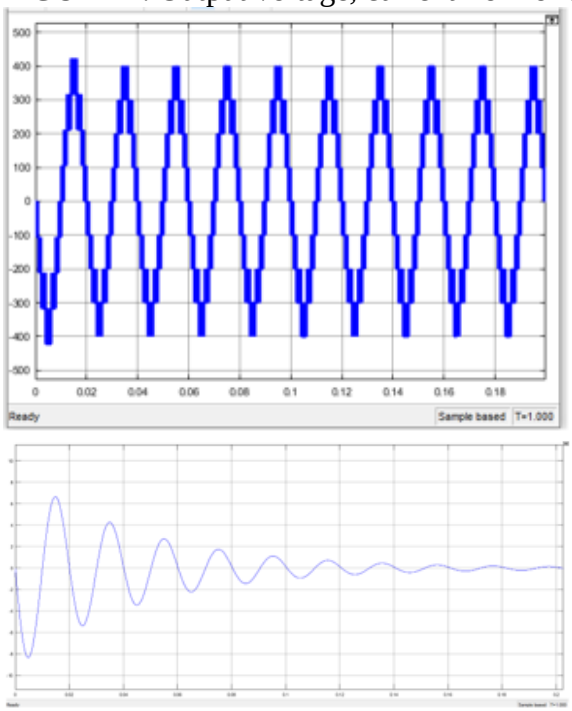

Figure 8. Output voltage and current for RL = 100 Ω +25mH, 100 Ω +75mH, 100 Ω +150mH.

CONCLUSION

For small scale solar PV applications, this paper proposes a high gain generalised MLI and quadruple boost nine-level inverter. It has the advantages of low switch stress and capacitor self-voltage balancing. A comparative study is carried out using recent literature. The proposed topology has been tested for various load variations, supply voltage variations, and load frequency variations, and it is appropriate for all types of loads. And, with different load variations, the capacitor's voltage ripples are within allowable limits. The topology is examined using the LSPWM technique for changes in amplitude and frequency modulation, as well as corresponding THD and fundamental component variations. The efficiency is examined in relation to load variations. Various simulation and testing methods are used to validate the effectiveness of the proposed topology.

REFERENCES

[1] N. Sandeep and U. R. Yaragatti, “Operation and Control of a NineLevel Modified ANPC Inverter Topology with Reduced Part Count for Grid-Connected Applications,” IEEE Trans. Ind. Electron., vol. 65, no. 6, pp. 4810–4818, 2018, doi: 10.1109/TIE.2017.2774723.

[2] C. Phanikumar, J. Roy, and V. Agarwal, “A Hybrid Nine-Level, 1- φ Grid Connected Multilevel Inverter with Low Switch Count and Innovative Voltage Regulation Techniques Across Auxiliary

Capacitor," IEEE Trans. Power Electron., vol. 34, no. 3, pp. 2159– 2170, 2019, doi: 10.1109/TPEL.2018.2846628.
[3] A. I. M. Ali, M. A. Sayed, E. E. M. Mohamed, and A. M. Azmy, "Advanced Single-Phase Nine-Level Converter for the Integration of Multiterminal DC Supplies," IEEE J. Emerg. Sel. Top. Power Electron., vol. 7, no. 3, pp. 1949–1958, 2019, doi: 10.1109/JESTPE.2018.2868734.
[4] P. Kala and S. Arora, "Implementation of Hybrid GSA SHE Technique in Hybrid Nine-Level Inverter Topology," IEEE J. Emerg. Sel. Top. Power Electron., vol. 9, no. 1, pp. 1064–1074, 2021, doi: 10.1109/JESTPE.2019.2963239.
[5] M. J. Sathik, N. Sandeep, D. J. Almakhles, and U. R. Yaragatti, "A Five-Level Boosting Inverter for PV Application," IEEE J. Emerg. Sel. Top. Power Electron., vol. 9, no. 4, pp. 5016–5025, 2021, doi: 10.1109/JESTPE.2020.3046786.
[6] M. Saeedian, S. M. Hosseini, and J. Adabi, "A five-level step-up module for multilevel inverters: Topology, modulation strategy, and implementation," IEEE J. Emerg. Sel. Top. Power Electron., vol. 6, no. 4, pp. 2215–2226, 2018, doi: 10.1109/JESTPE.2018.2819498.
[7] M. Saeedian, S. M. Hosseini, and J. Adabi, "Step-up switchedcapacitor module for cascaded MLI topologies," IET Power Electron., vol. 11, no. 7, pp. 1286–1296, 2018, doi: 10.1049/ietpel.2017.0478.
[8] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A Single DC Source Cascaded Seven-Level Inverter Integrating SwitchedCapacitor Techniques," IEEE Trans. Ind. Electron., vol. 63, no. 11, pp. 7184–7194, 2016, doi: 10.1109/TIE.2016.2557317. [16] S. S. Lee, "A Single-Phase Single-Source 7-Level Inverter with Triple Voltage Boosting Gain," IEEE Access, vol. 6, pp. 30005– 30011, 2018, doi: 10.1109/ACCESS.2018.2842182.
[9] J. Liu, J. Wu, and J. Zeng, "Symmetric/Asymmetric Hybrid Multilevel Inverters Integrating Switched-Capacitor Techniques," IEEE J. Emerg. Sel. Top. Power Electron., vol. 6, no. 3, pp. 1616–1626, 2018, doi: 10.1109/JESTPE.2018.2848675.
[10] M. D. Siddique et al., "Single-Phase Boost Switched-Capacitor Based Multilevel Inverter Topology with Reduced Switching Devices," IEEE J. Emerg. Sel. Top. Power Electron., vol. 6777, pp. 1–11, 2021, doi: 10.1109/JESTPE.2021.3129063.
[11] M. D. Siddique et al., "A Single DC Source Nine-Level SwitchedCapacitor Boost Inverter Topology with Reduced Switch Count," IEEE Access, vol. 8, pp. 5840–5851, 2020, doi: 10.1109/ACCESS.2019.2962706.
[12] M. D. Siddique, A. Iqbal, and A. Riyaz, "Single-Phase 9L Switched-Capacitor Boost Multilevel Inverter (9L-SC-BMLI) Topology," 9th IEEE Int. Conf. Power Electron. Drives Energy Syst. PEDES 2020, 2020, doi: 10.1109/PEDES49360.2020.9379779.
[13] M. D. Siddique et al., "Single-Phase Step-Up Switched-CapacitorBased," IEEE Trans. Ind. Appl., vol. 57, no. 3, pp. 3107–3119, 2021.
[14] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878–887, 2012, doi: 10.1109/TIE.2011.2158768.
[15] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "Analytical Determination of Conduction and Switching Power Losses in Flying-Capacitor-Based Active Neutral-Point-Clamped Multilevel Converter," IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5473– 5494, 2016, doi: 10.1109/TPEL.2015.2498107.
[16] Y. Ye, K. W. E. Cheng, S. Member, J. Liu, and K. Ding, "A StepUp Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 6672– 6680, 2014.
[17] R. S. Alishah, S. H. Hosseini, E. Babaei, M. Sabahi, and G. B. Gharehpetian, "New High Step-Up Multilevel Converter Topology with Self-Voltage Balancing Ability and Its Optimization Analysis," IEEE Trans. Ind. Electron., vol. 64, no. 9, pp. 7060–7070, 2017, doi: 10.1109/TIE.2017.2688968.

[18] J. Zeng, J. Wu, J. Liu, and H. Guo, "A Quasi-Resonant SwitchedCapacitor Multilevel Inverter with Self-Voltage Balancing for Single-Phase High-Frequency AC Microgrids," IEEE Trans. Ind. Informatics, vol. 13, no. 5, pp. 2669–2679, 2017, doi: 10.1109/TII.2017.2672733.
[19] A. Taghvaie and J. Adabi, "A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure," IEEE Trans. Power Electron., vol. 33, no. 1, pp. 199–209, 2018.
[20] M. Khenar, A. Taghvaie, J. Adabi, and M. Rezanejad, "Multilevel inverter with combined T-type and cross-connected modules," IET Power Electron., vol. 11, no. 8, pp. 1407–1415, 2018, doi: 10.1049/iet-pel.2017.0378.
[21] H. M. I. Featuring, "Switched-Capacitor-Based Single-Source Cascaded H-Bridge Multilevel Inverter Featuring Boosting Ability," IEEE Trans. Power Electron., vol. 34, no. 2, pp. 1113– 1124, 2019.
[22] S. S. Lee, K. B. Lee, I. M. Alsofyani, Y. Bak, and J. F. Wong, "Improved Switched-Capacitor Integrated Multilevel Inverter with a DC Source String," IEEE Trans. Ind. Appl., vol. 55, no. 6, pp. 7368–7376, 2019, doi: 10.1109/TIA.2019.2893850.