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DESIGN AND VALIDATION OF REDUCED SWING COMPLEMENTARY PASS-TRANSISTOR LOGIC FULL ADDER IN 16-NM CMOS TECHNOLOGY

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Abstract
Because of their unique internal logic structure and pass-transistor logic architecture, our innovative low-power full-adder cells significantly lower the power-delay product (PDP). We evaluated its speed, area, and power consumption in comparison to comparable full-adders that were said to have a low power consumption profile (PPD). A thorough test bench was used to track the current consumption from the full adders' inputs and the power supply current; all of the full adders were constructed utilizing a 16nm CMOS technology. The suggested full-adders achieve 80% average PDP advantage and 40% relative area advantage over its competitors in simulations.

Keywords: low power, reduced swing, Pass transistor, SR-CPL.

Introduction

Current CMOS (Complementary Metal-Oxide-Semiconductor) technology's power limitations and increasing integration density have made low-power design solutions essential. Using circuit-level techniques to decrease short-circuit power is one way to reduce the amount of power used by complementary metal-oxide semiconductor (CMOS) circuits, especially static logic gates operating at the 22 nm technology phase. Power dissipation due to short circuits occurs at the logic gate's transition phase when the p-channel and n-channel MOS transistors momentarily conduct electricity simultaneously. This conduction channel creates a direct current route between the power supply rails, which causes a brief increase in power consumption.Many approaches exist for reducing short-circuit power in 22-nm CMOS technology: One way to lessen the impact of short circuits on power usage is by using power gating. It entails disabling unused components of the circuit. This employs additional transistors to completely disable unused circuit components. Second, one way to avoid needless short circuits on current pathways is to utilize conditional pre-charging of nodes. To reduce the frequency of PMOS and NMOS transistors conducting at the same time, designers may use intelligent node pre-charging that occurs only when needed. Thirdly, rearranging circuit logic helps decrease power loss due to short circuits. Logic gate designers may reduce short-circuit power by rearranging the gates to eliminate direct PMOS and NMOS conduction paths during transitions. Scaling one efficient method of lowering short-circuit power is to increase the supply voltage.. Some examples of this include dynamic voltage scaling and the use of several voltage domains. Their role in lowering the voltage differential between transistors is responsible for this effect. Fifthly, improving the size and design of the transistors within the gates, as well as maximizing the overlap between the conduction of PMOS and NMOS transistors, may assist minimize short-circuit power.

Literature

One of the main goals of modern high-performance and/or portable electronics is energy efficiency. On the one hand, there's the ever-increasing need for portable electronics, which in turn requires components with low power consumption so that systems may operate for long periods of time on

batteries. On the other hand, modern high-performance processing applications need very fast circuits to keep up with the current tendency toward more complicated circuits and higher operating frequencies, both of which are necessary to fulfill the throughput demands of these applications. It is more accurate to use the power-delay product (PDP) meter to compare the optimizations of a module that have been tried and developed using various technologies, operating frequencies, and situations. The quantity of power required to do a specific job is measured by it.

The basic mathematical action of addition is essential to Many VLSI systems, which include microprocessors and designs for application-specific digital signal processing (DSP). This unit focuses on the four basic arithmetic operations: adding, subtraction, multiplying, and dividing. Addresses are also built there. The PDP of the full-adder, as I've already said, would impact the system's overall performance. Thus, creating full-adders with low power consumption and short propagation delay is crucial for current digital systems.

This article describes in depth the process of building and testing two full-adder cells with distinct internal logic designs. In order to achieve the SUM and CARRY results, the structure relies on multiplexing the Boolean operations XOR/ XNOR and AND/OR, correspondingly. are balanced. Power consumption in these cells is drastically reduced with the implementation of pass-transistor powerless/groundless logic types. The produced full-adders beat out other options for low-power arithmetic units in terms of latency and power consumption.

Existing Method

Method for Input-Controlled Leakage Restrictor Transistors:

A hypothetical block diagram for lowering leakage power, the input-controlled leakage restrainer transistor (ICLRT) approach is shown in Figure 4.1. This study describes a novel approach to lowering leakage power, predicated on the idea that a state with several cut-OFF transistors along a path from the supply voltage to ground is much lower than a state with a single cut-OFF transistor. The inclusion of one stack transistor with the main transistors ensures that the power supply signal that goes to ground for all possible input combinations has at least two cut-OFF transistors (PUN and PDN). By using this strategy, you may be certain that little electrical current will be lost. For this idea to work, a PMOS ICLRT is linked to the PUN, and for every feasible path from the supply voltage and ground to the output, an NMOS ICLRT is placed at the base of the PDN. Among the many noteworthy advantages of the proposed ICLRT method are: Operating at full swing produces high output levels because the input signals control the applied ICLRTs. A separate circuit for controlling sleep signals or substrate voltage is unnecessary with input-controlled ICLRTs because to their input power and small size.A single threshold voltage and inexpensive, industry-standard 22-nm CMOS technology are used in the proposed solution to eliminate unnecessary expense. PDN for each and every way that the input voltage, ground, and output might possibly go. There are many significant benefits to the proposed ICLRT method:

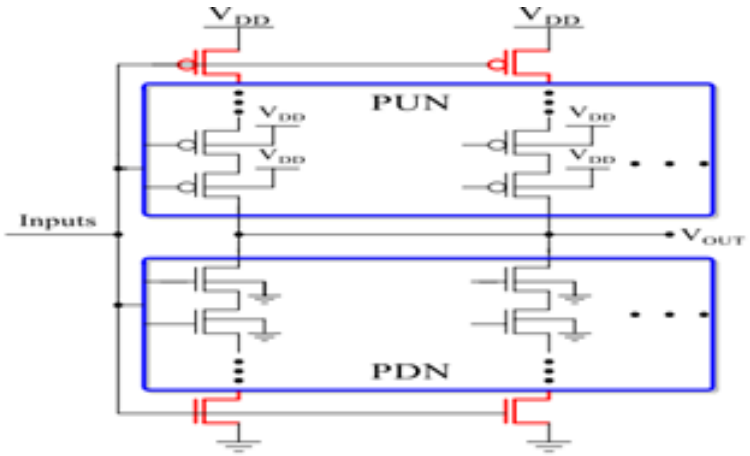

Figure.1: The suggested ICLRT method's conceptual block diagram

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When operated in full swing, the input signals control the applied ICLRTs, leading to high output levels. An extra circuit to manage sleep signals or substrate voltage is unnecessary with input-controlled ICLRTs since they are powered by input and are small. In order to reduce the system's propagation time, it employs the optimum amount of stack transistors. By using cheap, industry-standard The recommended approach eliminates wasteful cost by using 22-nm CMOS technology with a single threshold voltage. Of all the works of art listed above, not a single one has all of these qualities. By far the most popular gates constructed using the given approach are NOT, NAND, NOR, XOR, and XNOR (Figure 4.2). By meticulously including all of the previously specified components (Fig.4.2.a), the present work has been gifted with the following very desirable benefits: When IN = 0 (IN = 1), the sub-threshold current is drastically lowered when in standby mode. This happens when the gate-to-source voltage of MN (MP) becomes negative (positive) when the positive source potential VN > 0 (VP < VDD). Figure 4.2.a shows that when the PDN (PUN) turns on in active mode when IN = 1 (IN = 0), the gate-to-source voltage of MN (MP) drops below VDD due to VN > 0 (VP < VDD), therefore, the gate-oxide leakage current is greatly decreased. The extra ICLRTs reduce the gate-oxide leakage current by a stack effect, as shown in Figure 4.2.c.Saturation is approaching in both the MN and MP transistors as current flows short-circuit from the VDD rail to the ground rail at the switching point. Lower power and short-circuit current are shown by the MN and MP because to their smaller gate-to-source and higher threshold voltages.

Proposed Method

Existing method simulation results

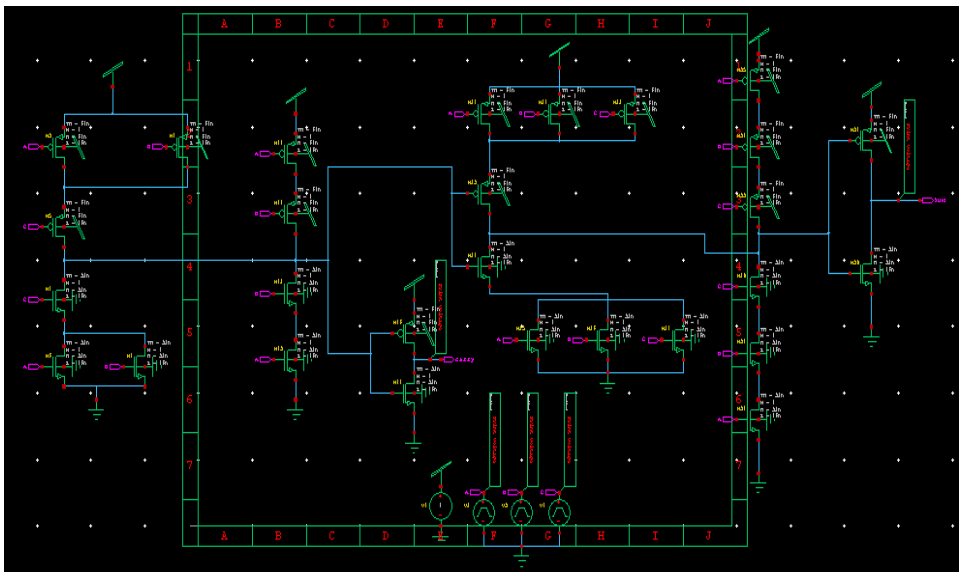

Figure 4.1 Simulation findings from current methods

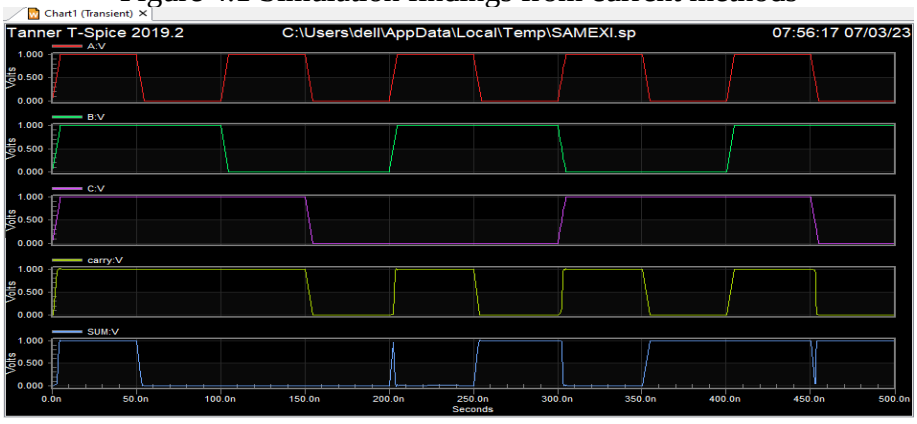

Figure 4.2 Simulation findings from current methods

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Current approach Analysis of power and delay

The power VV1 may be calculated by taking the transient tdealy trig v(A) and dividing it by the sum of all the variables. Then, with a value of 0.5.

```
Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 4.244984e-04 watts
Max power 5.454703e-04 at time 4e-09
Min power 2.508105e-04 at time 1.57384e-07


Measure information will be written to file "C:\Users\dell\AppData\Local\Temp\SAMEX

Measurement result summary
   tdealy          =  102.1650n
```

Existing Method Simulation

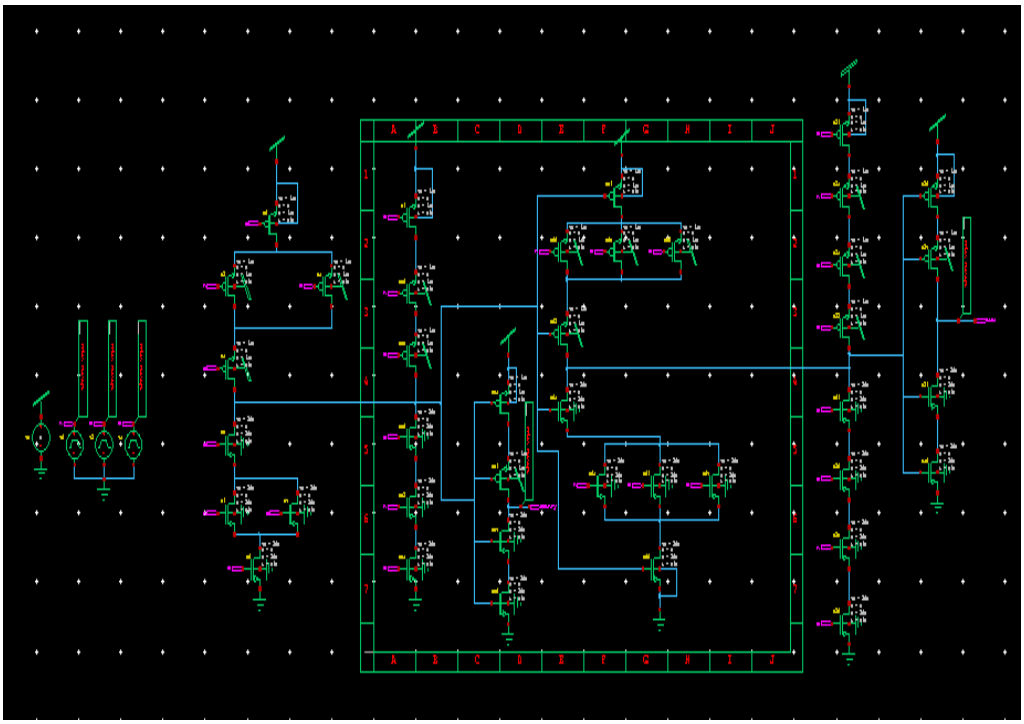

Figure 4.3 Simulation findings from current methods

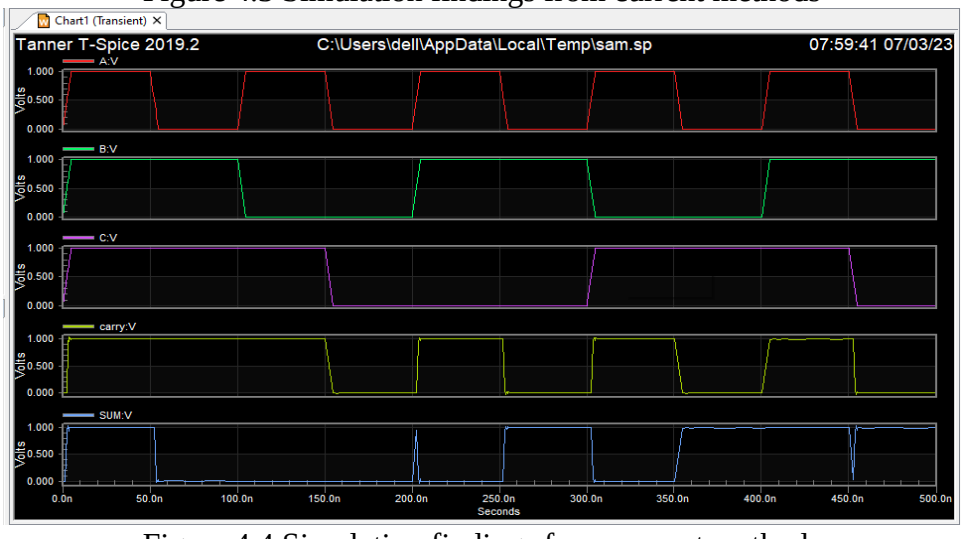

Figure 4.4 Simulation findings from current methods

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Existing Method Power And Delay Analysis

power VV1. The transfer function tdealy trig v(A) has a value of 0.5 and a fall of 0.5. The total variation targ v(SUM) also has a value of 0.5 and a fall of 0.5.

```
Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 3.749853e-05 watts
Max power 2.522633e-04 at time 2.80187e-09
Min power 2.587680e-05 at time 4.54606e-07
```

4.5 Proposed Sr-Cpl Method Simulation.

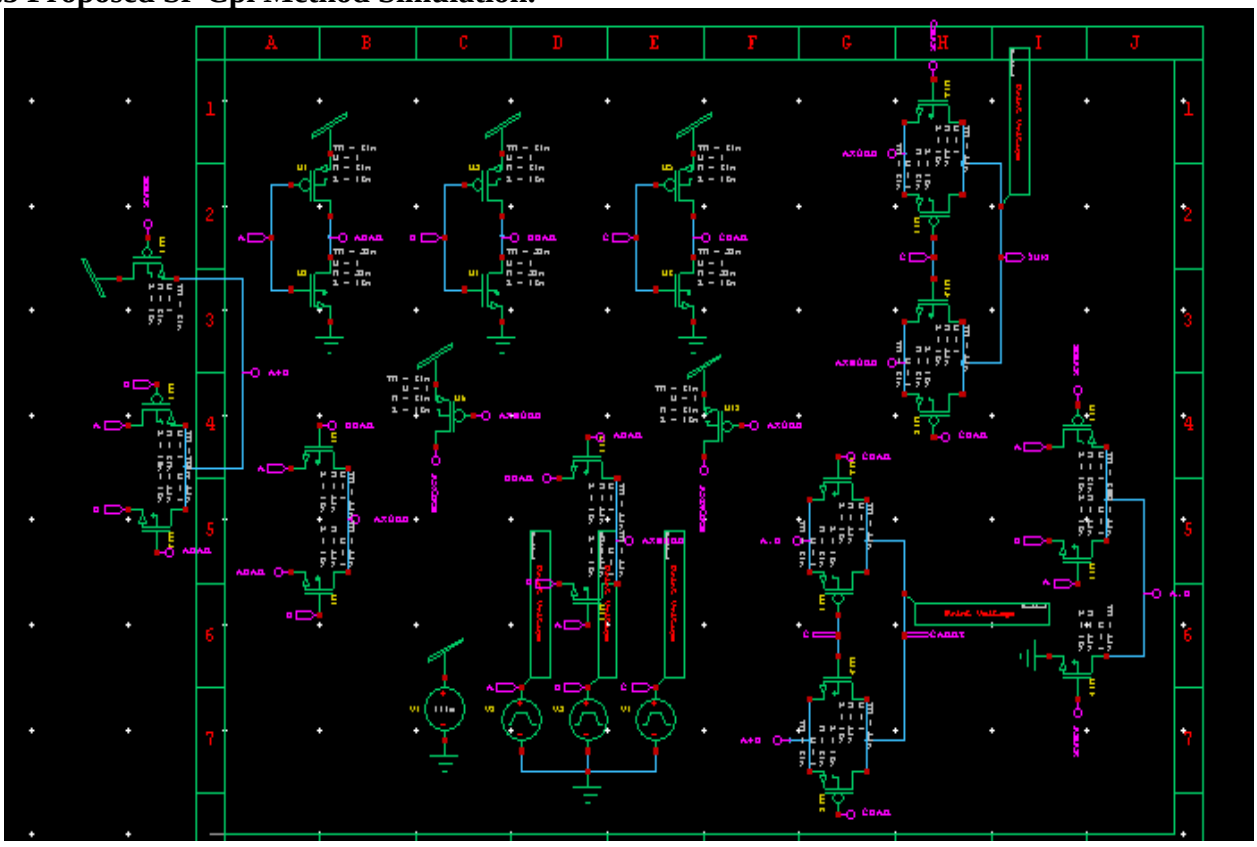

Figure 4.5 A full-adder that follows the suggested logic structure and uses the SR-CPL style of logic

The true-table of the full-adder is located in Table I. The output of So is equal to the value of A B when C is 0. C is also identical to A B when it equals 1. Thus, the same result may be achieved by use of a multiplexer, where the C input is used as the signal for selection. Similarly, when C=0, the Co output is A•B, and when C=1, it is A+B. When controlling a multiplexer, you may use C to choose the correct value for each condition. Figure 2 [13] shows an alternate logic approach for building a full-adder cell that involves joining two logic blocks. One block acquires the A B and A B signals, while the second block acquires the A • B and A + B signals. The So and Co outputs may be obtained by operating two multiplexers with the C input.The benefits and characteristics of it are detailed below.

The internal generation of signals to control the selection of output multiplexers is absent. Another option is to use the C input signal to control the multiplexers; this signal's complete voltage swing and absence of additional delay will lower propagation delays overall. Due to its reduced connection to individual transistor gates rather than the drain or source terminals—where the diffusion capacitance becomes quite high for sub-micrometer technology—the capacitive load on the C input has been decreased. Even if the C signal is on the critical route, bigger modules may still see a decrease in total latency.

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Having equal propagation delays at the outputs reduces the possibility of glitches in cascaded applications where the skew between incoming signals is critical for a proper functioning. Applications such as wave pipelining benefit from this. You may adjust the propagation delay of the So and Co outputs independently using the AND/OR and XOR/XNOR gates.

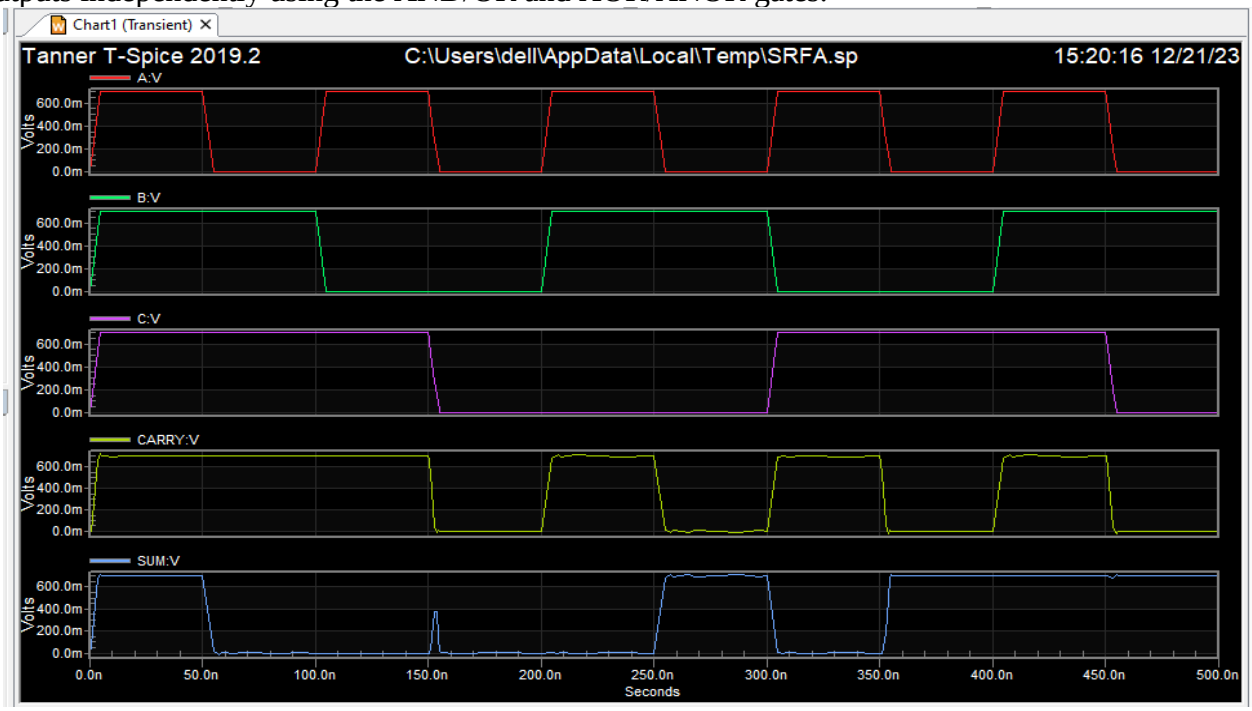

Figure 4.6 Full-adder designed with the proposed logic structure and a SR-CPL logic style

Applying a multiplexer to an input that is already configured to receive an XOR or XNOR signal or an AND or OR gate may improve performance for applications that are sensitive to load. Because of this, buffers may be inserted at the outputs of complete adders. Based on the findings in [13], the revised logic structure is shown in Figure 2. Plus, two brand new full-adders were created, one using the DPL type of logic and the other using the SR-CPL style. The So output is provided by a pass-transistor based multiplexer; Figure 3 illustrates a full-adder with XOR/XNOR gates created using DPL logic. The XOR/XNOR gates constructed using the SR-CPL logic approach are seen in Figure 4. To obtain the Co output, both examples employed a multiplexer based on pass-transistors; AND/OR gates were constructed using groundless and powerless pass-transistors, respectively.

Power And Delay Analysis

```
Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 2.179887e-07 watts
Max power 7.044140e-06 at time 1.53027e-07
Min power 2.545121e-09 at time 4.075e-07


Measure information will be written to file "C:'

Measurement result summary
   tdealy           =    51.1626p
```

Table 1. The Current Approach and the Suggested Alternative

S.no	Technology	Method	No.Trans	Power	Delay	PDP
1	22nm	Static CMOS	28	4.24 e-04	102.16n	4.32 e-11
2	22nm	ICLRT	40	3.74e-05	437.0443p	1.68 e-11
3	16nm	SR-CPL	26	0.021e-09	51.1626p	1.07 e-19

Application of the proposed method to one-bit full adders using swing-restored complementary pass-transistor logic produces the greatest results, as shown in the table. With smaller power consumption (0.021e-09 Nano watts), the proposed method decreases delay by 51.1626p seconds.

Conclusion

Using a pass-transistor logic approach and an alternative internal logic structure, we provide low-power, high-speed full-adder cells that reduce the power-delay product (PDP). We examined its speed, power consumption, and area to see how it compares to comparable low-PDP full-adders. The currents taken from the full-adders' inputs and the power supply were measured using a comprehensive test bench. All of the full-adders were built using 16nm CMOS technology. With a space need of only 40% and an average PDP benefit of 80%, Compared to their competitors, the suggested full-adders perform better.

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