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REPEATER INSERTION FOR TIMING OPTIMIZATION USING 28NM CMOS TECHNOLOGY

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Abstract
The research project on repeater insertion for timing optimization aims to enhance the timing performance of integrated circuits (ICs) during the physical design phase. Repeater elements are utilized to improve signal integrity and mitigate delays. Through the optimization of repeater placement, the goal of this project is to enhance signal quality, reduce delays, and meet timing constraints. Ultimately, the objective is to achieve timing closure by minimizing violations and enhancing overall circuit performance.

Keywords: Place & route, CTS, Signoff, Physical Verification.

Introduction
Very Large-Scale Integration (VLSI) involves the conversion of a logical circuit description into a physical layout that can be produced as an integrated circuit (IC). This transformation, known as physical design, encompasses a series of steps that focus on optimizing the layout for various factors including performance, power consumption, and area (PPA). The ultimate objective is to guarantee that the manufactured IC adheres to the specified design requirements and constraints, ensuring its functionality and efficiency. It is process to convert the gate level netlist into the manufacturable format (GDSII) which contains the physical information of the design.

28NM CMOS TECHNOLOGY:
The term CMOS stands for “Complementary metal oxide semiconductor”. CMOS technology is one of the most popular technology in the computer chip design industry and is broadly used today to form integrated circuits in numerous and varied applications.
The optimization of physical layout for integrated circuits (ICs) at the 28nm technology node, known as physical design, encompasses the implementation of diverse techniques within the realm of 28nm CMOS (Complementary Metal-Oxide-Semiconductor) technology. This intricate process plays a pivotal role in attaining the desired outcomes of enhanced performance, power efficiency, and effective utilization of space. The following diagrams are the CMOS implementations of the inverter.

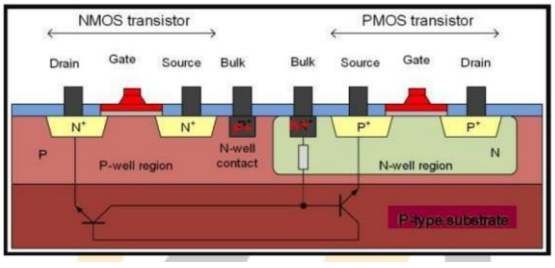

Figure 1: CMOS implementations of the inverter.

CMOS offers relatively high speed, low power dissipation, and high noise margins in both states and operates over a wide range of source and input voltages.

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Repeater Insertion & timing optimization:

Repeater insertion is a widely employed method in integrated circuits to mitigate the time delays caused by long wire lines. This approach entails dividing the lengthy wire into multiple shorter wires and subsequently incorporating a repeater between each pair of these newly formed shorter wires. By implementing this technique, the overall delay in the circuit is significantly reduced, leading to improved performance and efficiency.

The utilization of repeater insertion is a well-established strategy in integrated circuit design to address the time delays associated with long wire lines. This technique involves the segmentation of a lengthy wire into several shorter wires, followed by the insertion of a repeater between each pair of these newly created shorter wires. By employing repeaters at regular intervals, the signal propagation delay is effectively minimized, resulting in enhanced circuit performance and reduced power consumption. This approach is particularly beneficial in modern integrated circuits where long wire lines are prevalent, as it ensures efficient signal transmission and mitigates the adverse effects of wire length on circuit operation.

The process of timing optimization adheres to a 'top-down' methodology, where the focus is initially placed on analyzing and optimizing the scheduling level. Only after this step is completed, the optimization efforts are directed towards the code level, ensuring a systematic and efficient approach to enhancing timing performance.

In this we are using the block level implementation because in this we don’t need to use of the IO pads. But we are taking 2.0 space for IO pads in core to die of the Coreoffset. The distance between the core and the die boundary we called it as core offset.

Physical Design Flow:

The design flow is having some aspects of physical design in 28nm CMOS technology:

Partitioning:

The ASIC designs are generally very complex, so dividing the design into several small functional blocks can make other steps of the design flow much easier. The main goal of the partitioning phase is dividing the design into multiple blocks while minimizing the number of interconnections.

Floorplan & placement:

The floorplan is a crucial step in the design process as it involves determining the precise placement of each block within the overall layout. This selection of block placement is carefully optimized to ensure the best utilization of area, power, and performance. A poorly executed placement can significantly simplify the subsequent routing stage, but it can also lead to numerous complications during the routing phase. In a broader context, the floorplan encompasses both macro placement, which involves positioning larger blocks, and the subsequent placement of standard cells. Ultimately, floor planning plays a pivotal role in establishing the optimal block locations within a design.

Placement refers to the crucial task of determining the precise position of every individual cell within a given block. This intricate process is efficiently automated by the PnR tool, which employs advanced algorithms to streamline the placement procedure. The picture below shows as non-abutted placement, with gaps left between blocks for routing.

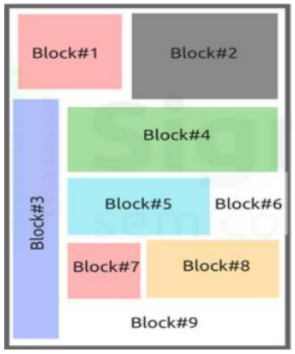

Figure 2: Floorplan & placement.

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Clock Tree Synthesis:

Prior to the clock tree synthesis process, the clock is considered to be ideal, meaning that there is no variation in timing between any two registers. However, during clock tree synthesis, the primary goal is to create an actual clock tree with the least amount of timing variation, known as skew. This reduction in skew is accomplished by inserting clock buffers in specific paths as needed. The accompanying images illustrate the clock tree before and after the clock tree synthesis process. It is evident that prior to CTS, the assumption is that the clock signal is distributed to all registers from a single source, whereas after CTS, a realistic clock tree is constructed, taking into account the actual timing variations.

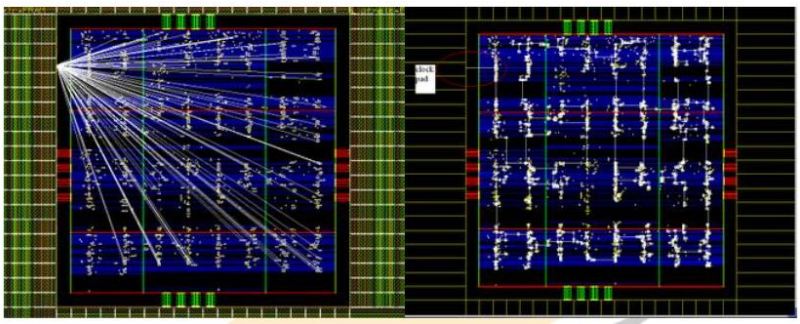

Figure 3: Clock Tree Synthesis.

Routing:

Once the placement and CTS (Clock Tree Synthesis) stages are finished, the subsequent step involves routing our design. Following CTS, the tool possesses precise information regarding the pin locations of the standard cells and macros, while the netlist provides the logical connectivity of the design along with the DRC (Design Rule Check) identification defined by the technology file. Taking into consideration all of these constraints, the tool proceeds to execute the most optimal routing strategy. The layout progress of our design throughout the PnR (Place and Route) process can be observed in the image below. It is evident that after the routing phase, all the blocks have been appropriately placed, the clock tree has been constructed, and all the necessary interconnections have been successfully established.

Physical verification:

The process of physical verification involves using EDA software tools to confirm the accuracy of an integrated circuit layout design. This verification ensures that the design functions correctly both electrically and logically, as well as being suitable for manufacturing. Various checks are performed during this process, including design rules check (DRC), layout versus schematic (LVS), XOR (exclusive OR), antenna checks, and electrical rule check (ERC). The design rule check (DRC) ensures that the current design adheres to all the rules specified in the technology file. Following this, the layout versus schematic (LVS) check is conducted to verify if the layout aligns with the netlist.

Signoff:

Before finalizing the design, a thorough evaluation is conducted to ensure that it fulfills all the necessary manufacturing, reliability, and functional requirements.

Once the design is finalized, the complete set of design data is transferred to the foundry for the manufacturing process to commence.

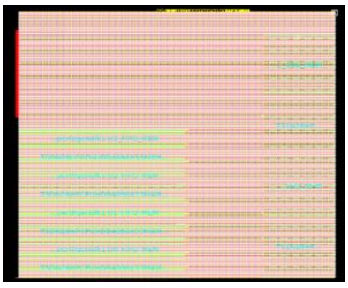

Figure 4: Final output from IC Design tool.

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IC Compiler II Tool:

IC Compiler II is a comprehensive system for implementing netlist-to-GDS II, offering a range of features and benefits. It encompasses various stages of the design process, starting from early exploration and prototyping to detailed planning, block implementation, chip assembly, and sign-off driven design closure. The foundation, architecture, and implementation of IC Compiler II are built upon innovative and patented technologies. The software itself has been developed using modern object-oriented languages and tools, ensuring efficiency and effectiveness.

One of the key advantages of IC Compiler II is its new hierarchical infrastructure, which enables massive parallelism. This means that multiple tasks can be executed simultaneously, leading to significant time savings and improved productivity. Additionally, IC Compiler II incorporates a high compact multi-mode (MMMC) architecture, which allows for efficient handling of multiple design modes. This is particularly beneficial in today's complex designs that often require support for various operating modes.

Another notable feature of IC Compiler II is its next-generation design planning capabilities. This includes advanced algorithms and techniques that aid in optimizing the design for performance, power, and area. The software also employs global, analytical, and scalable optimization techniques, ensuring that the design meets the desired specifications while minimizing resource utilization.

Figure 5: Synopsys IC Compiler II.

Furthermore, IC Compiler II offers global optimization approaches for clock synthesis. This ensures that the clock network is optimized for timing, power, and area, resulting in improved overall design performance. Additionally, IC Compiler II seamlessly integrates into existing design flows, thanks to its compatibility with industry-standard interfaces and file formats. This allows designers to easily incorporate IC Compiler II into their existing workflows without any major disruptions or compatibility issues.

In summary, IC Compiler II is a powerful and versatile netlist-to-GDS II implementation system. Its innovative features, such as the hierarchical infrastructure, MMMC architecture, advanced design planning, and global optimization techniques, make it a valuable tool for designers. With its compatibility with industry standards, IC Compiler II seamlessly integrates into existing design flows, providing a smooth and efficient design process.

Result & Conclusions:

1. The first objective of the project is to convert technology independent RTL (Register Transfer Level) designs into the manufacturing format of GDSII (Graphic Data System II). This conversion process is crucial for the fabrication of integrated circuits.
2. Another important aspect of the project is the optimization of power, area, and performance in VLSI (Very Large-Scale Integration) designs. By carefully analyzing and fine-tuning the design, the project aims to achieve the best possible balance between these three factors.
3. To reduce congestion and ensure efficient routing, the project will incorporate blockages and keep-

out margins. These measures will help prevent overcrowding and ensure smooth signal flow throughout the circuit.
4. To avoid crosstalk and electromigration issues, the project will utilize NDRs (Noise Density Ratio) in the design. These components will help minimize interference between signals and prevent the degradation of the circuit due to electromigration.
5. The project will also address any shorts and opens in the design. These issues can cause significant malfunctions in the circuit, and by fixing them, the project aims to ensure the reliability and functionality of the final product.
6. In addition to fixing shorts and opens, the project will also address setup and hold violations. These violations occur when the timing requirements of the circuit are not met, leading to potential data corruption. By resolving these violations, the project aims to improve the overall performance and stability of the design.
7. One of the key focuses of the project is to reduce power consumption in VLSI designs. By implementing various power optimization techniques, such as voltage scaling and power gating, the project aims to minimize power wastage and improve the energy efficiency of the circuit.
8. Another objective of the project is to enhance the circuit performance. This includes achieving higher speeds, lower latencies, and improved overall functionality. By carefully analyzing and optimizing the design, the project aims to push the boundaries of performance in VLSI circuits.
9. The project will also prioritize area optimization. By reducing the physical area occupied by the block, the project aims to maximize the utilization of the available space and improve the overall efficiency of the design.
10. Signal integrity is a critical aspect of VLSI designs, and the project will focus on improving it. By minimizing signal degradation and noise, the project aims to ensure robust and reliable communication between different components of the circuit.
11. Lastly, the project will adhere to industry standards and specifications. This ensures that the final design is compatible and interoperable with existing systems, making it easier.

Technology Node	28NM TSMC
Instant Count	62k
Frequency	400MHZ
Macros	6
Number of Clocks	1
Metal Layers	9
Description	Block level Implementation

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