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IMPLEMENTATION OF LOW VOLTAGE DIGITAL GATES USING BULK-DRIVEN TECHNIQUES

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Abstract
This paper evaluates the performance of a low-voltage bulk-driven quasi-floating gate (BD QFG) based on NAND and NOR digital gate circuits in comparison to bulk-driven (BD) and gate-driven (GD) digital gates. The findings show that the BD QFG NAND and NOR gates offer a propagation delay of 0.054 ns and 0.065 ns, power dissipation of 45.6 W and 28.5 W, and a power delay product (PDP) of 2.46×10^{-3} pJ and 1.86×10^{-3} pJ, respectively. The design has been simulated through PSpice simulation using a 0.5 V power supply in a 0.13 µm CMOS technology.

KEYWORDS: Bulk-Driven, Quasi-Floating Gate MOSFET, Logic Gates

1. INTRODUCTION

The primary approach for enhancing the performance of very Large-scale Integration (VLSI) circuits has historically involved the downscaling of complementary metal-oxide-semiconductor (CMOS) technology. However, recent indications suggest that the downsizing of Metal-Oxide-Semiconductor (MOS) transistors may be constrained by inherent limitations dictated by their operational principles. The bulk-driven technique has become prevalent to address this challenge and enhance the speed performance of sub-threshold circuits [1]. This strategy facilitates speed improvement and mitigates the impact of process and temperature variations, thereby preserving energy efficiency [1]. Much work has been done in the past on bulk-driven techniques such as bulk-driven differential CMOS Schmitt trigger and bulk-driven Winner-Takes-All (WTA) structure incorporating a voltage follower (VF) [2, 3]. A bulk-driven tunable transconductor topology employing six bulk-driven CMOS inverters was designed to achieve extremely low supply/consumption with a rail-to-rail input common-mode range [4, 5]. Integrating bulk-driven techniques with quasi-floating gate presents alternatives to extend the scalability of the bulk-driven MOS circuits. One such application is Differential Difference Current Conveyors (DDCCs), which employ both quasi-floating gate (QFG) and bulk-driven quasi-floating-gate (BD QFG) techniques [6]. Operational Transconductance Amplifiers (OTAs) utilize the bulk-driven technique [7, 8], while the OTA employing the bulk-driven floating-gate technique achieves low-power consumption for filter applications [9]. Furthermore, the OTA incorporates the Flipped Voltage Follower (FVF) configuration to reduce power consumption, and this OTA's linearity is enhanced by incorporating a bulk-driven technique with a floating gate [10].

Scaling down the supply voltage serves as an effective method for diminishing power consumption in integrated circuit designs. However, operating circuits with reduced voltage leads to a considerable decline in the speed of digital circuits [11]. To address this issue, digital designers employ strategies such as the bulk-driven technique, aiming to minimize circuit delays. By integrating the bulk-driven technique, CMOS designers maintain clock constraints even as the voltage supply decreases [12]. Universal gates, such as NAND and NOR, are fundamental building blocks of digital logic circuits. They possess the remarkable ability to emulate any other logic gate, making them indispensable in digital design. NAND and NOR gates hold significance in digital circuitry because they reduce the

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overall number of gates required in a circuit design. This reduction in gate count leads to minimized circuit area occupancy, consequently enhancing the circuit's efficiency by reducing propagation delays. Different techniques and styles are used to design these gates to improve their performance parameters [12-14]. By leveraging bulk-driven techniques, the performance of these universal gates can be further improved in terms of power efficiency, circuit simplicity, speed, and miniaturization.

2. BULK-DRIVEN TECHNIQUE

In bulk-driven technique a bias voltage is applied to the gate of the MOSFET, creating a channel between the source and drain. Unlike conventional MOSFETs, the signal is applied at the bulk contact, and the channel stays unchanged as long as the gate bias voltage is constant. This removes the threshold voltage restriction on the signal pathway and makes it possible to expand the range of low supply voltage applications for any analog circuit.

The threshold voltage of the BD MOSFET shown in Fig. 1 is given as:

$$V_{TH(VB'S)} = V_{tho} + \gamma\sqrt{2\phi_F + V_{BS}} - \gamma\sqrt{2\phi_F} \quad (1)$$

Having drain current can be expressed as:

$$i_D = k\frac{W}{L}\left(V_{GS} - V_{TH(VB'S)}\right)^2 \quad (2)$$

The transconductance of bulk-driven MOSFET is given by:

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} \quad (3)$$

Where γ is bulk threshold parameter and $2\phi_F$ is surface potential at strong inversion. g_{mb} represents the transconductance from the bulk input-node voltage V_{BS} to the output current i_D.

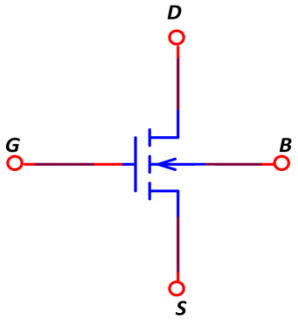

Figure 1. Symbol of BD MOSFET

The comparative transfer characteristics of BD MOSFET and conventional gate-driven MOSFET are shown in Figure 2(a). As evident from Figure 2(a) in BD MOSFETs, the threshold voltage is significantly lower than in conventional MOSFETs. This is because the channel in a BD MOSFET is formed in the bulk region, which is inherently more conductive than the lightly doped channel region in conventional MOSFETs. As a result, the transfer characteristic of a BD MOSFET is nonlinear, and the device can be turned on with lower gate voltages, which makes them more suitable for low-power applications. Figure 2(b) shows the drain characteristics of BD MOSFET, which shows the effect of bulk to source voltage upon the drain current. The figure shows I_D as a function of $V_{ds}$for different values of V_{bs} upto 0.4 V in steps of 0.1 V.

N-channel BD MOSFET shown in Figure 1 has been simulated by PSpice with 0.5 V supply voltage and the aspect ratio taken as 2.6 µm/0.13 µm for obtaining the transfer and drain characteristics.

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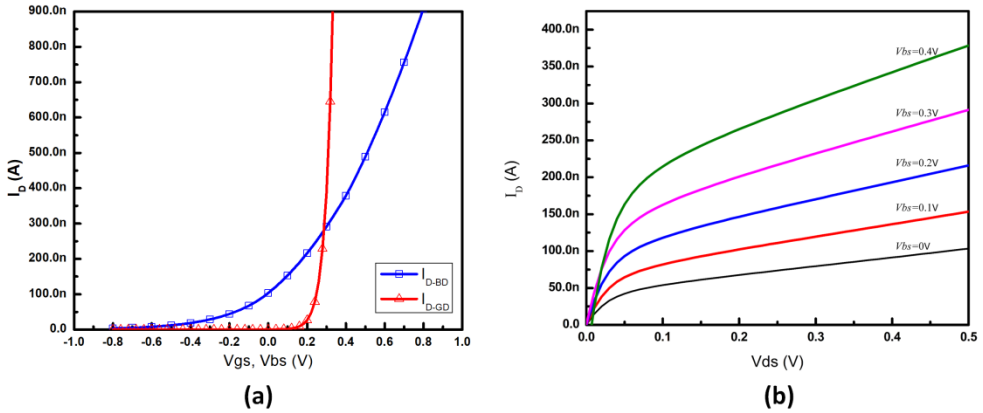

Figure 2. (a) Transfer characteristic (b) Output characteristic of BD MOSFET

2.1. Bulk-driven based NAND and NOR Gate

The design of the bulk-driven based NAND gate is similar to the conventional gate-driven NAND gate, except in this design, the signals are applied at the bulk terminal of the MOS, and the gate terminals are connected to a bias source, V_{bp} biased source is connected to the p-type MOS, and the gates of the n-type MOS are connected to V_{bn} biased source.

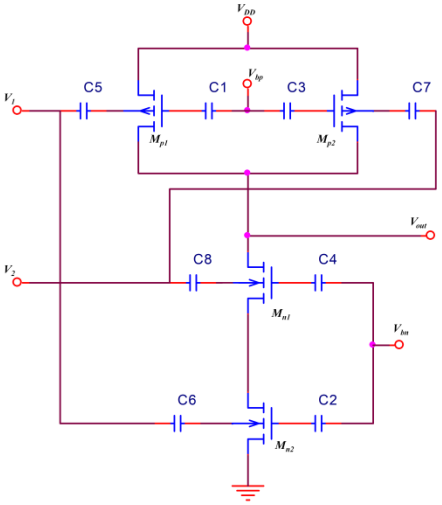

Figure 3. NAND gate using BD technique

The BD-based NAND gate circuit depicted in Figure 3 has been simulated to analyze the voltage transfer characteristics (VTC) across various bias voltages applied to both the p and n-channel BD MOS transistors. This analysis has been conducted by selecting specific aspect ratios for M_{p1} and M_{p2} as 26 µm/0.13 µm and for M_{n1} and M_{n2} as 13 µm/0.13 µm, utilizing a supply voltage of 0.5 V. The VTCs of the NAND gate using the BD technique are shown in Figure 4.

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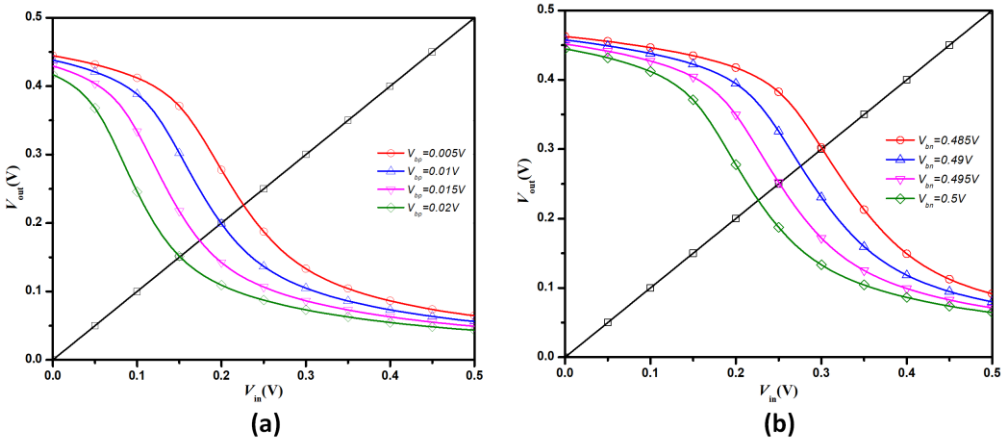

Figure 4. VTC of NAND gate using BD technique at different (a) V_{bp} and (b) V_{bn}

Table 1 showcases the calculated values for the switching threshold voltage (V_S) and noise margins (NM_H and NM_L), obtained from Figure 4(a) and (b) across varying V_{bp} and V_{bn} values.

Table 1 Noise margins of BD NAND gate at different Vbp and Vbn

V_{bp} (V)	V_S (V)	NM_H (V)	NM_L (V)	V_{bn} (V)	V_S (V)	NM_H (V)	NM_L (V)
0.005	0.22	0.28	0.22	0.485	0.30	0.20	0.30
0.01	0.20	0.30	0.20	0.49	0.27	0.23	0.27
0.015	0.17	0.33	0.17	0.495	0.25	0.25	0.25
0.02	0.15	0.35	0.15	0.5	0.22	0.28	0.22

These findings indicate that altering the bias voltages V_{bp} and V_{bn} modifies the voltage transfer characteristics of the BD NAND gate, leading to a reduced switching threshold voltage and amplified noise margins. In high-speed digital circuits, logic gates should introduce minimal delay when inputs transition. Minimizing propagation delay becomes crucial to enhance the NAND gate's speed. This has been achieved by implementing the BD technique, as shown in Figure 3. The circuit has transient response simulation at various V_{bp} and V_{bn} values. This simulation involved selecting the aspect ratio of M_{p1} and M_{p2} as 26 µm/0.13 µm and M_{n1} and M_{n2} as 13 µm/0.13 µm, with a supply voltage of 0.5 V. Figure 5 illustrates the transient characteristics of the NAND gate employing the BD technique across various values of V_{bp} and V_{bn}.

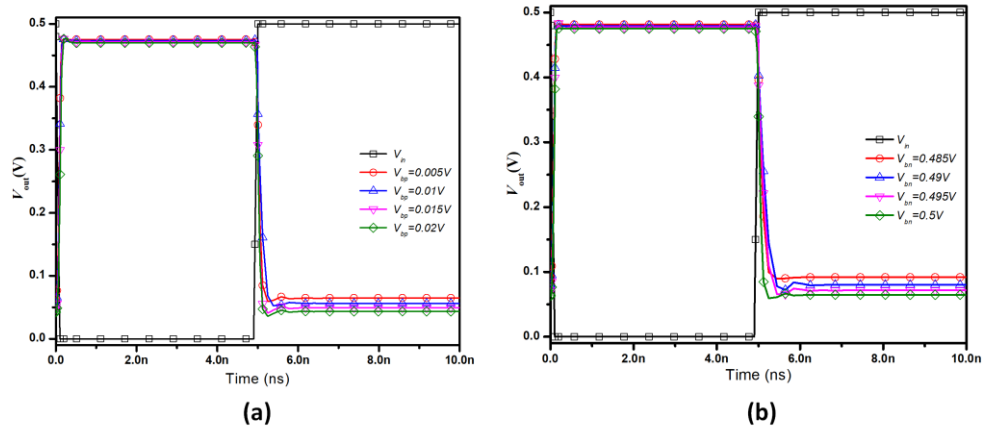

Figure 5. Transient response of BD technique NAND gate at various values of (a) V_{bp} and (b) V_{bn}

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Figure 5(a) exhibits the variation in the bias voltage (V_{bp}) of the p-channel BD MOS from 0.005 V to 0.2 V while maintaining a fixed bias voltage (V_{bn}) of the n-channel BD MOS at 0.5 V. Similarly, Figure 5(b) displays the variation of V_{bn} from 0.485 V to 0.5 V, with V_{bp} fixed at 0.005 V. Throughout these variations, the output voltage (V_{out}) is recorded over time. An observed trend indicates that the propagation delay correlates with the bias voltage.

From the transient responses depicted in Figure 5(a) and (b), the propagation delay calculation has been performed and is presented in Table 2.

Table 2 Propagation delay of BD NAND gate at different V_{bp} and V_{bn}

V_{bp} (Volts	Delay (ps)	V_{bn} (Volts)	Delay (ps)
0.005	58.0	0.485	75.5
0.01	58.9	0.49	67.0
0.015	60.0	0.495	62.0
0.02	60.7	0.5	58.7

The circuit design of the bulk-driven NOR gate technique is same as the BD NAND gate; the input signals are applied at the bulk terminals of the conventional gate-driven NOR gate, and the gate terminals are connected to a biased voltage V_{bp} and V_{bn}.

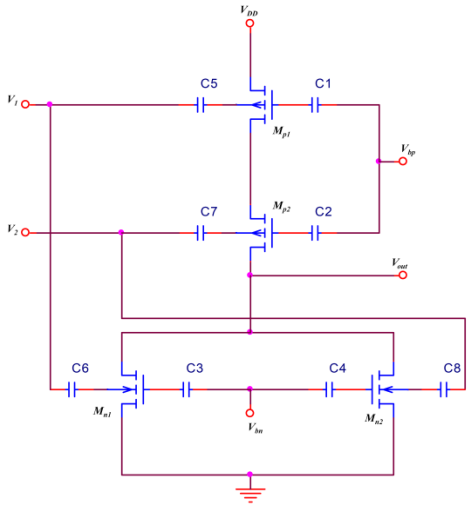

Figure 6. NOR gate using BD technique

Simulation of the circuit depicted in Figure 6 has been conducted to acquire the voltage transfer characteristics at different bias voltage values, as shown in Figure 7.

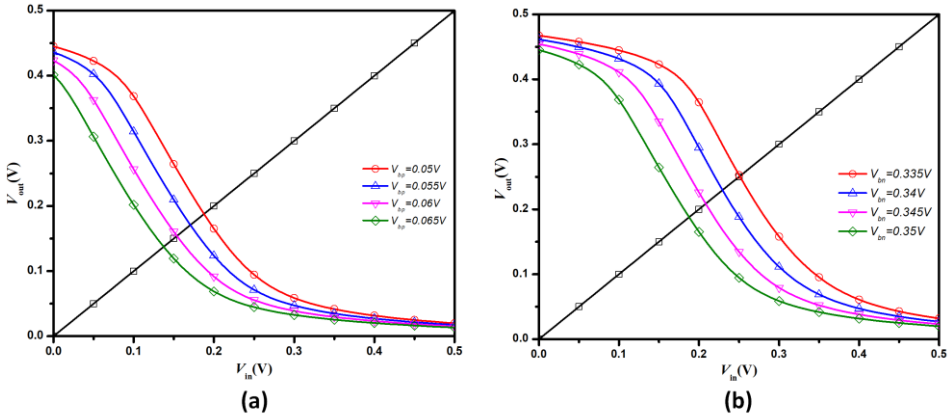

Figure 7 VTC of NOR gate using BD technique at different (a) V_{bp} and (b) V_{bn}

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Tables 3 present the calculated values for the switching threshold voltage (V_S), noise margins (NM_H and NM_L), obtained from Figures 7(a) and (b) across various V_{bp} and V_{bn} values.

Table 3 Noise margins of BD NOR gate at different Vbp and Vbn

V_{bp} (V)	V_S (V)	NM_H(V)	NM_L(V)	V_{bn} (V)	V_S (V)	NM_H(V)	NM(V)$_L$
0.05	0.18	0.32	0.18	0.335	0.25	0.25	0.25
0.055	0.17	0.33	0.17	0.34	0.23	0.27	0.23
0.06	0.15	0.35	0.15	0.345	0.20	0.30	0.20
0.065	0.13	0.37	0.13	0.35	0.18	0.32	0.18

Simulations were conducted to assess the transient behavior of the NOR gate utilizing the BD technique depicted in Figure 6. These simulations involved setting the aspect ratio of M_{p1} and M_{p2} as 26 µm/0.13 µm and M_{n1} and M_{n2} as 13 µm/0.13 µm, using a supply voltage of 0.5 V. The transient characteristics of the NOR gate for various V_{bp} and V_{bn} values are displayed in Figure 8.

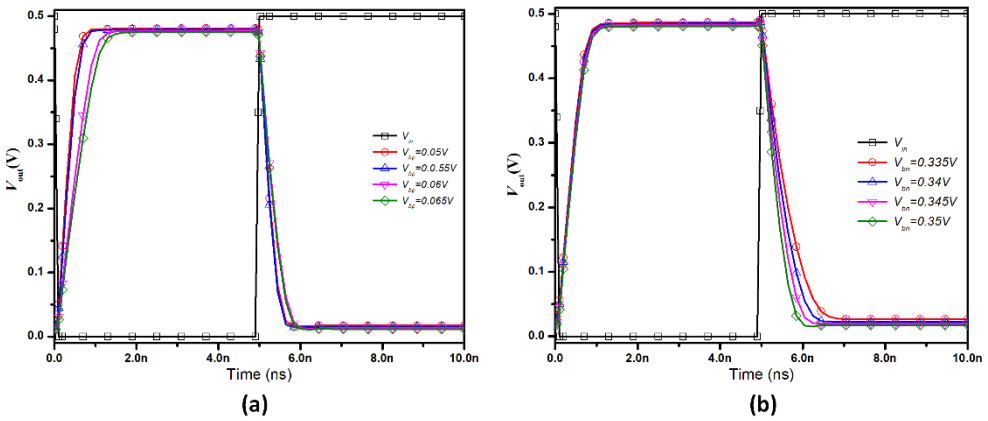

Figure 8. Transient response of BD technique NOR gate at different (a) V_{bp} and (b) V_{bn}

From the transient responses shown in Figure 8, we have calculated the propagation delay as listed in Table 4.

Table 4 Propagation of BD NOR gate at different V_{bp} and V_{bn}

V_{bp} (Volts	Delay (ns)	V_{bn} (Volts)	Delay (ns)
0.05	0.355	0.335	0.440
0.055	0.374	0.34	0.407
0.06	0.392	0.345	0.382
0.065	0.415	0.35	0.359

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2.2. Bulk-driven QFG based NAND and NOR Gate

The speed of the NAND gate can be further enhanced if we replace the BD device with BD QFG, which operates on a charge-sharing mechanism without complete isolation of the floating gate in its structure. The circuit of the NAND gate using BD QFG is shown in Figure 9.

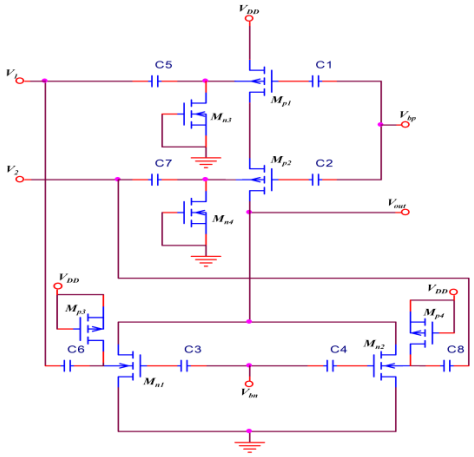

Figure 9. QFGMOS NOR gate using BD technique

The comparative transient characteristics and truth table (logic operation) of the NAND gate employing gate-driven, bulk-driven, and BDQFG approaches have been acquired. This was achieved by choosing the aspect ratio of p-channel MOS as 26 µm/0.13 µm and n-channel MOS as 13 µm/0.13 µm while utilizing a supply voltage of 0.5 V. These results are showcased in Figure 10. Upon analyzing the simulation outcomes, it has been noted that the NAND gate using BD QFG exhibits a propagation delay of 0.054 ns, which is notably lower when compared to the BD (0.075 ns) and gate-driven NAND gate (0.574 ns).

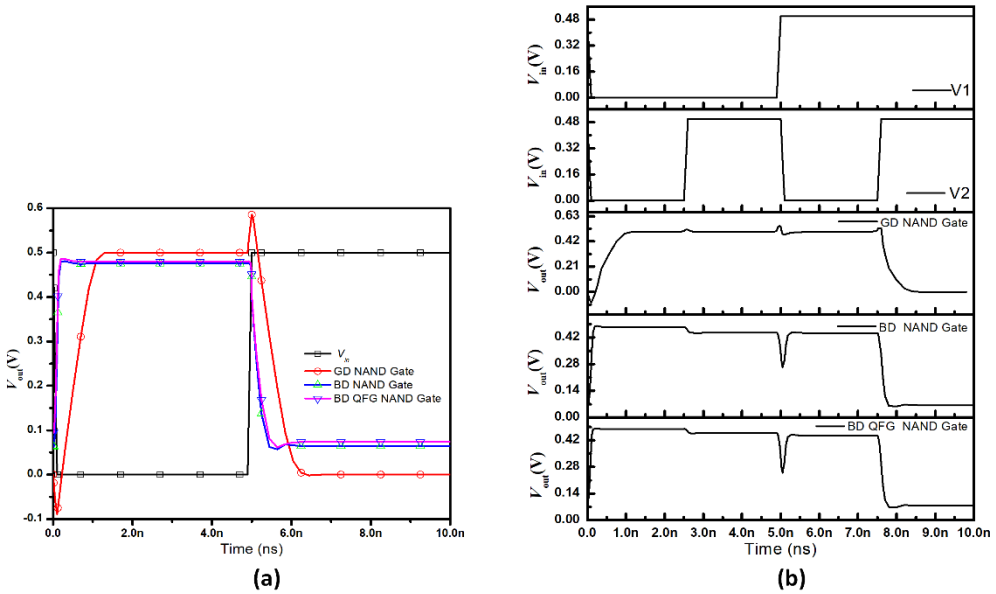

Figure 10. Comparative (a) transient response (b) logic operation of NAND gate

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Since the BDQFG NAND gate improves the performance of the BD NAND gate in terms of propagation delay, it is expected that the BDQFG-based NOR gate would exhibit better operating speed than its bulk-driven type. The BDQFG NOR circuit gate is shown in Figure 11.

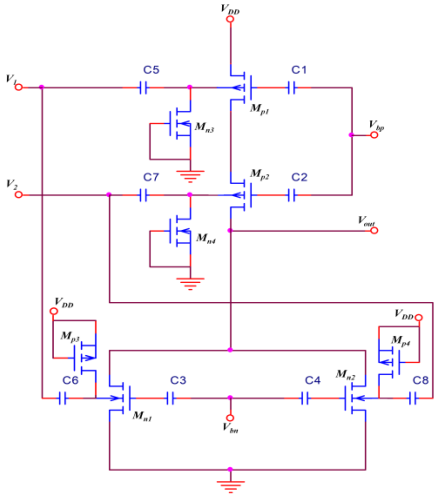

Figure 11. QFGMOS NOR gate using BD technique

The comparative transient characteristics and truth table (logic operation) of the NOR gate employing gate-driven, bulk-driven, and bulk-driven QFG methods have been derived. This was achieved by choosing the aspect ratio of the p-channel MOS as 26 µm/0.13 µm and the n-channel MOS as 13 µm/0.13 µm, with a supply voltage of 0.5 V. These results are depicted in Figure 12.

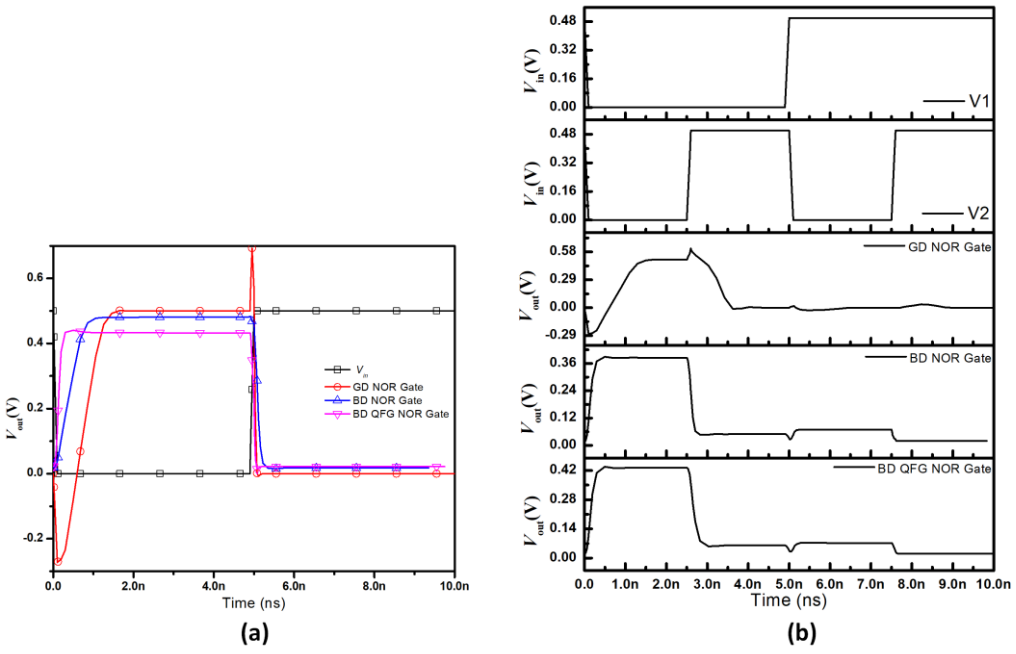

Figure 12. Comparative (a) transient response and (b) logic operation of NOR gate

Analysis of the simulation results reveals that the BD QFG NOR gate demonstrates a propagation delay of 0.065 ns. This value is notably lower compared to the BD's propagation delays (0.359 ns) and gate-driven NOR gate (0.467 ns). Table 5 summarized the performance parameters of NAND and NOR gate utilizing GD, BD, and BDQFG technique.

Table 5 the performance parameters of NAND and NOR gate utilizing GD, BD, and BDQFG technique

Parameters	Power (W)	Delay (ns)	PDP (pJ)
GD- NAND	9.24×10^{-11}	0.574	5.30×10^{-8}
BD- NAND	4.04×10^{-5}	0.074	2.98×10^{-3}
BDQFGD- NAND	4.56×10^{-5}	0.054	2.46×10^{-3}
GD-NOR	2.14×10^{-11}	0.467	1.00×10^{-8}
BD-NOR	2.57×10^{-5}	0.359	9.22×10^{-3}
BDQFGD- NOR	2.85×10^{-5}	0.065	1.86×10^{-3}

3. CONCLUSIONS

The pursuit of universal gate implementations through bulk-driven techniques represents a promising frontier in the field of digital electronics. The bulk-driven technique makes designing low-voltage gates with less propagation delay possible, which is further improved by combining it with QFG MOS in standard CMOS processes. The findings show that the BD QFG NAND and NOR gate offer a propagation delay of 0.054 ns and 0.065 ns, respectively, which is less than compared to their gate-driven counterparts (0.574 ns for NAND and 0.467 ns for NOR gate) at the expense of increased power dissipation (4.56×10^{-5} W for BDQFG NAND, 2.85×10^{-5} W for BDQFG NOR gate, 9.24×10^{-11} W for gate driven NAND gate and 2.14×10^{-11} W for gate driven NOR gate respectively). Thus, a proper heat-sinking mechanism must be incorporated to enhance the speed of digital circuits employing the BDQFG technique to expel the excess heat. The design has been simulated through simulation using a 0.5 V power supply in a 0.13 µm CMOS technology. All the circuits are verified by employing PSpice simulation software.

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