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GNRFET BASED DYNAMIC D FLIP FLOP DESIGN

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Abstract
The D flip-flop is an important memory component that is used in wireless communication devices. It offers enhanced power consumption and performance compared to other flip-flops. Researchers have offered the idea in order to improve energy efficiency as well as approaches for the generation of power. Computer systems also make use of flip-flop registers as a means of conserving energy and avoiding the wasteful dissipation of that energy. In this thesis, an alternative design for a D flip-flop is given to replace the Graphene Nano Ribbon Field Effect Transistor in the 22nm technology channel in order to accomplish efficient energy generation. The goal of this replacement is to reduce the size of the transistor. The suggested circuit has been shown to perform better in terms of mean power, time delay, and energy dissipation by means of the HSPIICE simulation. Flip-flops of the D kind are used in wireless sensor networks in order to lessen the amount of power that is consumed and to improve power management. GNRFETs have a voltage dissipation that is much better than that of bulk CMOS MOSFETs, which makes them a practical choice for the 22nm channel length technology.

Keywords- D flip flop; vlsi; nano technology

1. Introduction

There has been a significant increase in the need for conventional as well as specialist VLSI devices [1-4] as a direct result of the ever-increasing complexity of communication networks. Circuit integration is now more critical than it has ever been before in order to ensure the effective and practical deployment of SONET, SDH, and ATM networks in the future [5-6]. The relevance of these kinds of networks has been brought to light, in particular, as a result of the standardisation process. The goal of this chapter is to discuss the usual integrated circuit requirements that are present in the telecommunications sector. Designers of VLSI devices that operate in the telecommunications market face a range of challenges, and this chapter's focus is on how to overcome those challenges.
The mobile phone industry is expanding at a breakneck pace, and in the most recent years, in addition to traditional mobile phones, there has been a notable growth in the number of wearable information devices as well as gadgets related to healthcare [7-9]. This category includes many electronic devices that may be worn on the person, such as fitness trackers, smartwatches, and other devices. The preferences of customers are shifting towards ease of use and adaptability, which is made possible by contemporary technologies that enable the development of powerful computers that are able to show multimedia content. This shift in consumer preferences reflects an evolution in the nature of their shopping experiences. Portable applications that have a low consumption of battery power and a high throughput are becoming an increasingly crucial component in the effort that these organisations are making to meet their objectives. Tablet and smartphone computers, for example, are now undergoing development to provide computing capacity that is equivalent to that of desktop computers; this underscores the need for architectures that are tiny, low-power, and portable [10-12]. It is very vital to implement low-energy design solutions that have been carefully considered since the quantity of power that these devices consume is a crucial factor that defines the requirements for their weight and size.

Additionally, the higher clock rate in high-performance computer applications has led to a growth in clock jitter and clock skew, which are becoming increasingly significant variables in the whole clock cycle. This is because clock jitter and clock skew are caused by variations in the timing of the clock. This is due to the fact that fluctuations in the timing of the clock are the root cause of both clock jitter and clock skew.

Memory elements are used rather often in communication systems. Wireless Sensor Networks (WSNs) (14), in particular, make extensive use of the D flip-flop. It is often utilised in the creation of shift registers, which enable the efficient storing and retrieval of data by the cascade of a large number of D flip-flops [14]. Shift registers are commonly used in computer programming. By connecting the inverting output of one D flip-flop to the D input of the next D flip-flop, it is possible to create a circuit that divides by two. This enables state transitions to take place at a rate that is half that of the clock signal that is being received. By connecting it with extra external combinational logic gates [15], this arrangement may be further developed into a countdown timer.

A component such as the D flip-flop's primary function is to store state-related information by using a circuit that can exist in either of two stable states [16-18]. This is accomplished by employing a circuit that can be in either of the two states. It is a bi-stable device that has a range of behavioural qualities, and it is used widely in computers, digital electronics, and applications that are dependent on communication. Memory cells are the fundamental purpose of flip-flops; as such, they are responsible for storing data and delivering outputs that are time-synchronized with the clock signal. Flip-flops also play an important role in digital logic circuits. Flip-flops, and more particularly D flip-flops, are components that are used widely in computer systems for the purpose of storing data in registers. D flip-flops are exactly the kind of flip-flop that is employed. D flip-flops are differentiated from D latches by the fact that the output of a D flip-flop only reflects the state of the D input when the clock signal is on a positive edge. This is the primary difference between the two types of logic gates.

In order to achieve high transmission speeds through optical fibre, optical switches are a necessary component of the system. The processing of signals and the transmission of data across optical fibres are only two of the many roles that these switches are put to use for in a variety of contexts. In addition, the D flip-flop has a key role to play in the digital circuitry of today. Optical switches are becoming more important components of high-speed communication and networking systems as a result of the growing significance of optical technology in high-speed communication as well as the increasing speed and complexity of optical fibre networks. In optical communications, all-optical signal processing has a range of applications, and it is projected that in the future, it will play a significant role in the development of all-optical information networks. More than anything else, optical packet switching (OPS) systems need all-optical memory components in order to address the challenges brought on by congestion in the packet transport layer. On the other hand, the costs associated with purchasing these components are among the highest that can be found anywhere else on the market. Optical memory and tunable optical delay lines (TODLs) are the fundamental elements that go into the construction of sophisticated photonic integrated circuits (PICs). Modulation, amplification, and switching are all functions that may be carried out by a single device thanks to the combination of these components.

2. Implementation

Previous research has identified a number of high-performance D flip-flops, one of which, known as the TSPC (True Single-Phase Clock) D flip-flop, stands out as a particularly notable example [1]. Other high-performance D flip-flops have also been discovered. By shortening one critical route's latency and doing away with the device that generates pulses, the TSPC D flip-flop is able to demonstrate significant improvements in both its speed and its power consumption. The overall performance of the flip-flop is improved as a result of these two modifications. As a crucial component of our investigation, the TSPC D flip-flop has been the focus of further analysis and has been improved as a result of our efforts. Because of advancements in technology, leaky power dissipation has taken

on a greater significance as a fraction of total power dissipation. As a consequence, unique solutions to the issue of power loss have had to be developed in order to address this challenge. A promising new technology known as the Graphene Nano Ribbon Field Effect Transistor (GNRFET) has just emerged and is now being manufactured by a number of the industry's most prominent chip manufacturers.

The D flip-flop is an essential element of sequential circuit logic and is used in a broad range of electronic devices, such as microprocessors, microcontrollers, storage devices, delay devices, and very large scale integrated circuits (VLSI). It is also an essential part of sequential circuit logic. The TSPC notion, also known as a pre-settable True Single-Phase Clock based D flip-flop, is a method for constructing a circuit that performs well in the 180nm technology [1]. This method is also known as the pre-settable True Single-Phase Clock based D flip-flop. If we compare the performance of this dynamic flip-flop variant to that of static D flip-flops, we discover that the dynamic flip-flop variety is superior. This is because dynamic flip-flops use more current than static D flip-flops. In addition, a modified TSPC-based D flip-flop has the capability of resolving some of the issues that are typical of ordinary D flip-flops. The TSPC-based D flip-flop has been designed with a suppressed toggling node route included into it. As a result, this helps to cut down on the overall amount of errors that may take place throughout the circuitry[1].

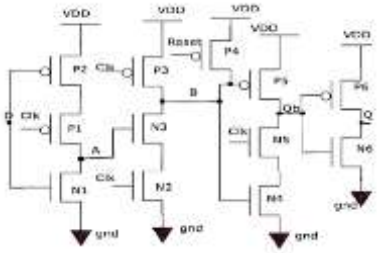

Figure 1: TSPC based D Flip Flop

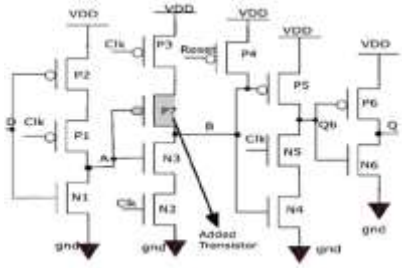

Figure 2: Modified TSPC based D Flip Flop

The research offers Figures 1 and 2's circuits, which are modified versions of the ordinary D flip-flop, as an attempt to remedy the shortcomings in that design. The operation of a D flip-flop is similar to that of a D latch, with the notable difference that the state of the D input is delayed by one clock cycle whenever the output of the D flip-flop experiences a positive clock edge (or a negative edge for an active low clock input). Because of this property, the phrase "delay flip-flop" or "delay line" is often used when referring to it. The value of the D input pin is recorded by the flip-flop whenever a clock event takes place, and all future changes to the value of that pin are disregarded until the next time a clock event takes place. The output of a level-clocked device may vary regardless of whether the clock is high or low, in contrast to the output of an edge-triggered flip-flop, which can only be altered when the clock is either rising or falling at an edge. The difference between edge triggering and level clocking is that edge triggering only permits one modification to the output per clock cycle, whereas level clocking permits numerous changes during each clock half cycle.

The D flip-flop has the simplest design of all the many types of flip-flops. On the other hand, latches are often referred to be level-sensitive devices since their output follows their inputs for as long as they are enabled. This is the case regardless of whether or not they are enabled. As long as the enable signal is present, latches will continue to be inactive and will not make any changes to their output. When

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certain conditions are met, it is desirable to make changes to the output only when the enable signal goes up or down. This enable signal typically performs the function of the principal clock control signal, making it possible for any modifications to be synchronised with the rising or falling edge of the clock.

GNRFETs, which have superior electrical properties (PDP) compared to ordinary MOSFETs, may be used to build high-performance dynamic TSPC D flip-flops. These flip-flops can be produced using GNRFETs. Due to the better properties of GNRFETs, switching from standard operation (SO)-mode GNRFETs to planar MOSFETs in the TSPC D flip-flop results in a considerable reduction in the amount of time needed for power delay. It has been suggested that further optimisation utilising a modified TSPC architecture with MOSFETs akin to GNRFETs should be done in order to decrease PDP and boost space utilisation. According to the findings of the simulations, the redesigned TSPC D flip-flop decreases PDP while only marginally increasing the number of transistors.

To create the GNRFET 22nm design, which will be utilised for simulating the TSPC-based D flip-flop shown in Figure 2, HSPICE simulation will be carried out. Figure 3 depicts the upgraded GNRFET circuit, while Figure 4 depicts the Sleep Mode circuit. Both of these figures may be seen below.

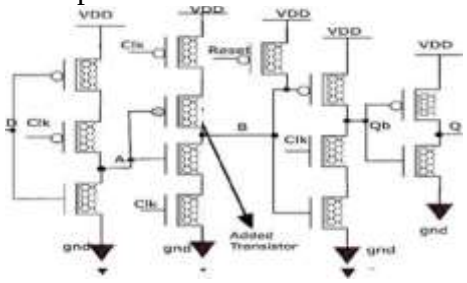

Figure 3: DFF TSPC GNRFET 22nm

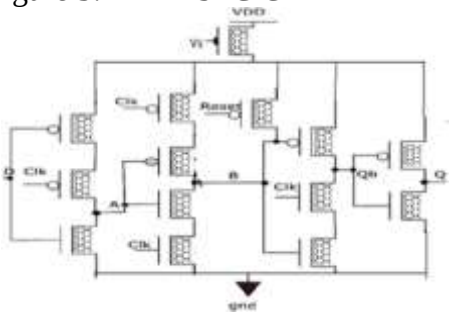

Figure 4: Proposed DFF GNRFET 22nm

3.Results

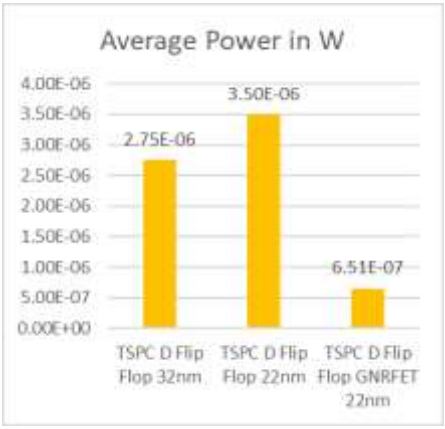

Figure 5: Average Power Result TSPC DFF MOS and GNR

Figure 5 shows that the TSPC DFF GNR based average power is lowest and 22nm MOS highest, which are the short channel consequences.

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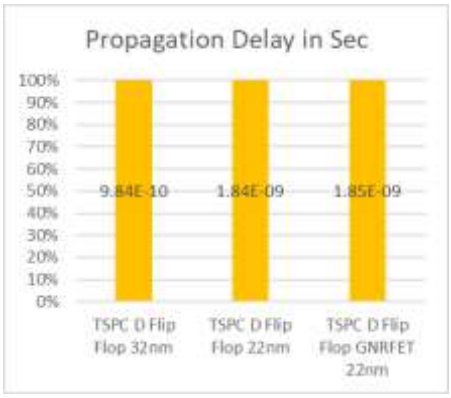

Figure 6: Delay Result TSPC DFF MOS and GNR

The delay case of GNRFET 22nm is considered to be the lowest on a single TSPC circuit in figure 6.

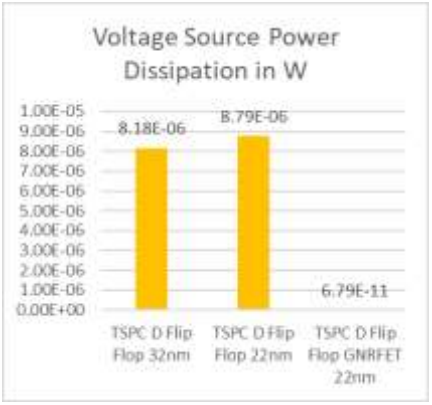

Figure 7: Power Dissipation Result TSPC DFF MOS and GNR

In Figure 7, the dynamic TSPC circuit based on GNRFET shows the lowest voltage power dissipation..

Figure 8: PDP Result TSPC DFF MOS and GNR

Figure 8 shows the PDP in DFF TSPC GNR as lowest and in MOS TSPC 22nm as highest..

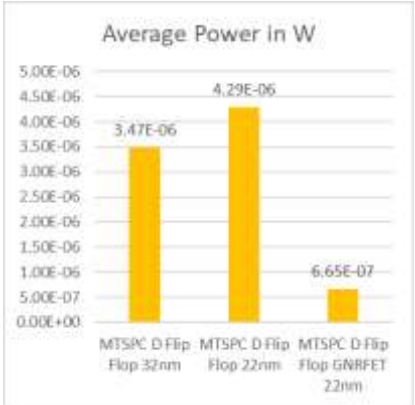

Figure 9: Average Power M TSPC DFF MOS and GNR

In the case of the upgraded TSPC D flip flop 22nm setup the average power and delay is also low in figures 9.

Conclusion

A favourable discovery was made about the use of GNRFET-based circuits, which demonstrated roughly the same voltage source power dissipation. This finding is supported by the results of simulations run using both HSPICE and Avanwaves. While there has been a 97.9% rise in both time and power dissipation, there has been a 99.9% increase in the amount of power that has been used. In addition, the voltage source PDP has been subjected to a substantial transformation of around 90% when compared to the version that came before it. This suggests that the Dynamic D Flip Flop circuit, when combined with GNRFET technology, has the potential to provide low power consumption as well as high-speed optimisation.

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